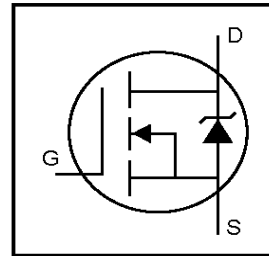


IRFBC40S/LPbF

HEXFET® Power MOSFET

- Surface Mount (IRFBC40S)
- Low-profile through-hole (IRFBC40L)
- Available in Tape & Reel (IRFBC40S)
- Dynamic dv/dt Rating
- 150°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Lead-Free



$$V_{DS} = 600V$$

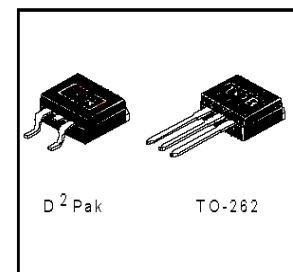
$$R_{DS(on)} = 1.2\Omega$$

$$I_D = 6.2A$$

Description

Third generation HEXFETs from international Rectifier provide the designer with the best combination of fastswitching, ruggedized device design, low on-resistance and cost-effectiveness.

The D²Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application. The through-hole version (IRFBC40L) is available for low-profile applications.



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ⑤	6.2	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ⑤	3.9	
I_{DM}	Pulsed Drain Current ① ⑤	25	
$P_D @ T_A = 25^\circ C$	Power Dissipation	3.1	W
$P_D @ T_C = 25^\circ C$	Power Dissipation	130	W
	Linear Derating Factor	1.0	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ② ⑤	570	mJ
I_{AR}	Avalanche Current ①	6.2	A
E_{AR}	Repetitive Avalanche Energy ①	13	mJ
dv/dt	Peak Diode Recovery dv/dt ③ ⑤	3.0	V/ns
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

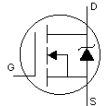
Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	---	1.0	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted, steady-state)**	---	40	

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	600	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.70	—	$V/^\circ C$	Reference to $25^\circ C, I_D = 1mA$ ⑤
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	1.2	Ω	$V_{GS} = 10V, I_D = 3.7A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Transconductance	4.7	—	—	S	$V_{DS} = 100V, I_D = 3.7A$ ⑤
I_{DSS}	Drain-to-Source Leakage Current	—	—	100	μA	$V_{DS} = 600V, V_{GS} = 0V$
		—	—	500		$V_{DS} = 480V, V_{GS} = 0V, T_J = 125^\circ C$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
Q_g	Total Gate Charge	—	—	60	nC	$I_D = 6.2A$
Q_{gs}	Gate-to-Source Charge	—	—	8.3		$V_{DS} = 3600V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	30		$V_{GS} = 10V$, See Fig. 6 and 13 ④⑤
$t_{d(on)}$	Turn-On Delay Time	—	13	—	ns	$V_{DD} = 300V$
t_r	Rise Time	—	18	—		$I_D = 6.2A$
$t_{d(off)}$	Turn-Off Delay Time	—	55	—		$R_G = 9.1\Omega$
t_f	Fall Time	—	20	—		$R_D = 47\Omega$, See Fig. 10 ④⑤
L_S	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
C_{iss}	Input Capacitance	—	1300	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	160	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	30	—		$f = 1.0MHz$, See Fig. 5⑤

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	6.2	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	25		
V_{SD}	Diode Forward Voltage	—	—	1.5	V	$T_J = 25^\circ C, I_S = 6.2A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	450	940	ns	$T_J = 25^\circ C, I_F = 6.2A$
Q_{rr}	Reverse Recovery Charge	—	3.8	7.9	μC	$di/dt = 100A/\mu s$ ④⑤
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② $V_{DD} = 50V$, starting $T_J = 25^\circ C$, $L = 27mH$
 $R_G = 25\Omega$, $I_{AS} = 6.2A$. (See Figure 11)
- ③ $I_{SD} \leq 6.2A$, $di/dt \leq 80A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 150^\circ C$
- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ⑤ Uses IRFBC40 data and test conditions

** When mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to application note #AN-994.

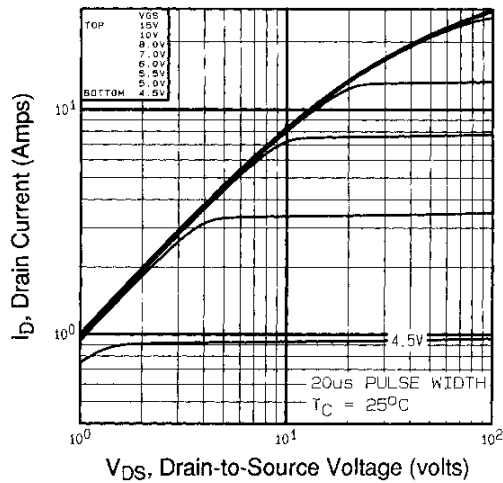


Fig 1. Typical Output Characteristics,

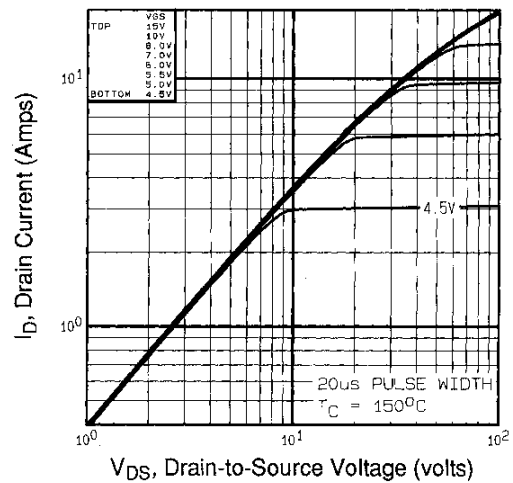


Fig 2. Typical Output Characteristics,

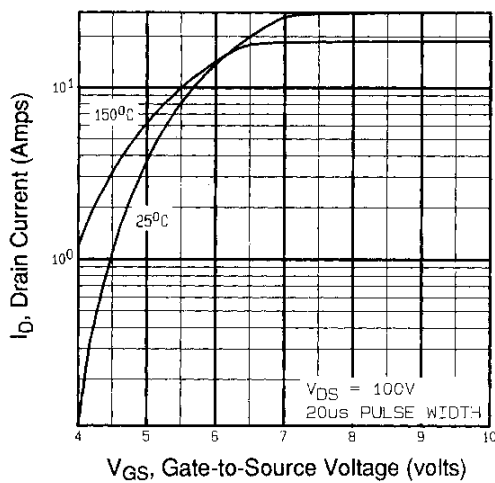


Fig 3. Typical Transfer Characteristics

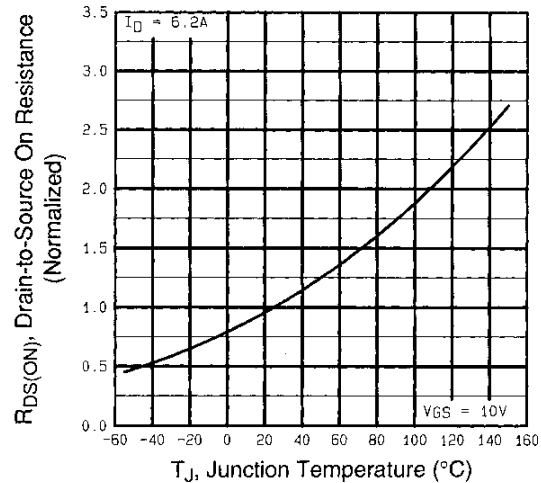


Fig 4. Normalized On-Resistance
Vs. Temperature

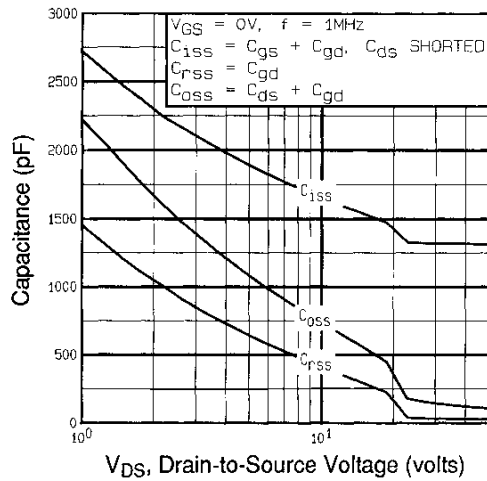


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

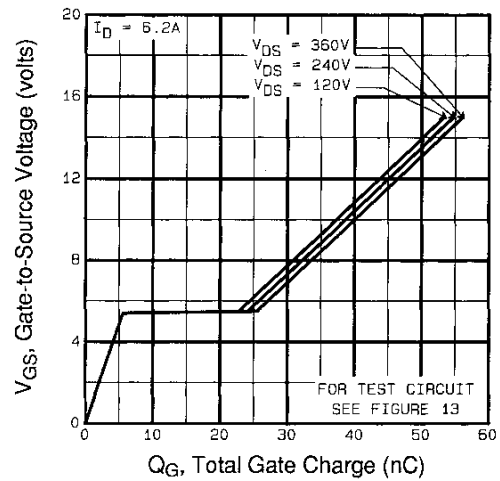


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

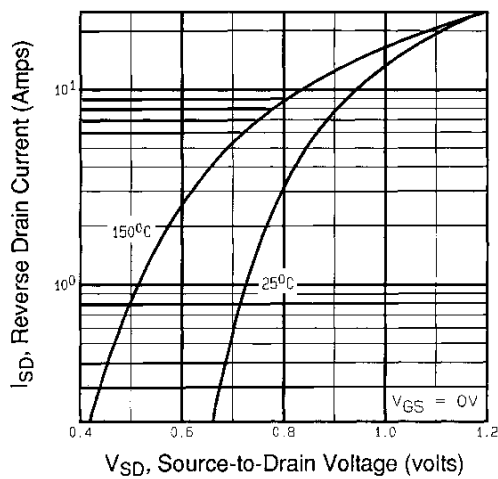


Fig 7. Typical Source-Drain Diode Forward Voltage

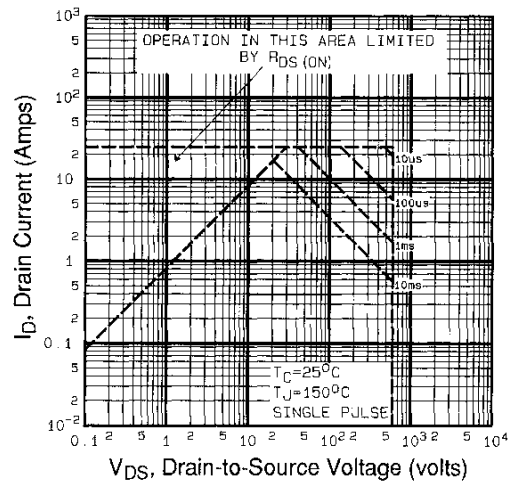


Fig 8. Maximum Safe Operating Area

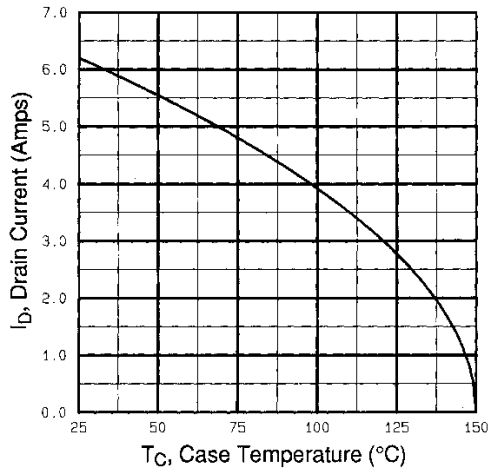


Fig 9. Maximum Drain Current Vs. Case Temperature

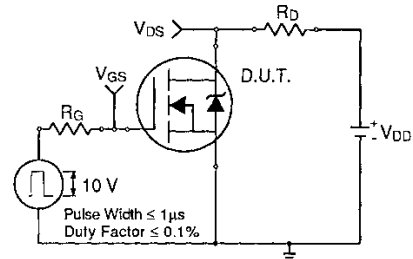


Fig 10a. Switching Time Test Circuit

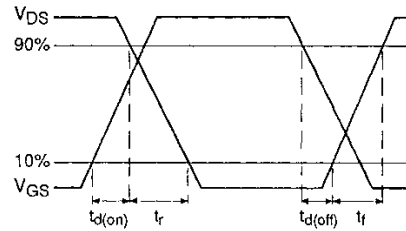


Fig 10b. Switching Time Waveforms

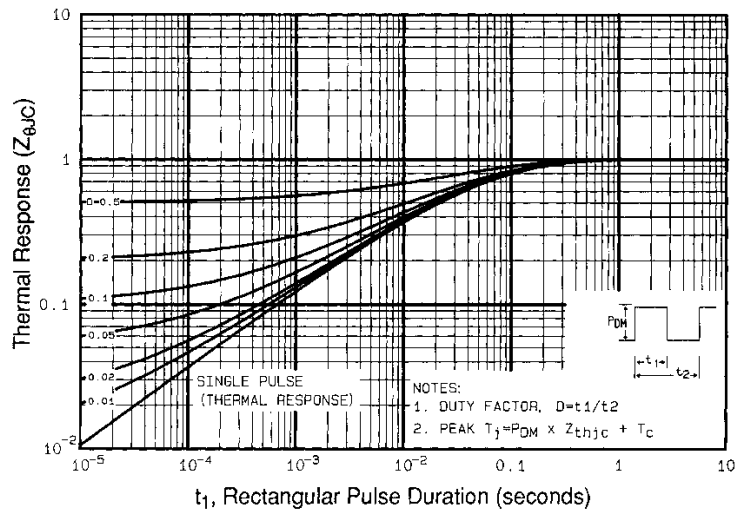


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

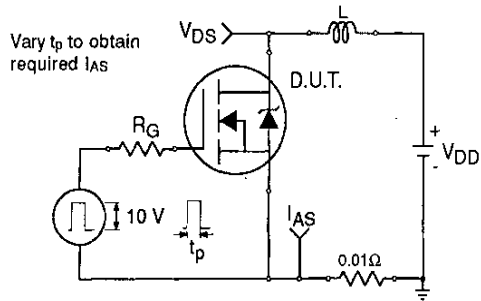


Fig 12a. Unclamped Inductive Test Circuit

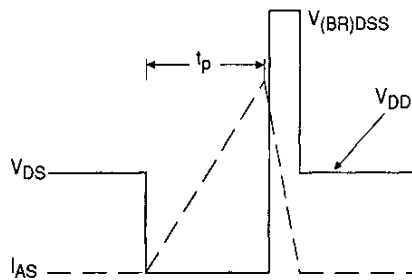


Fig 12b. Unclamped Inductive Waveforms

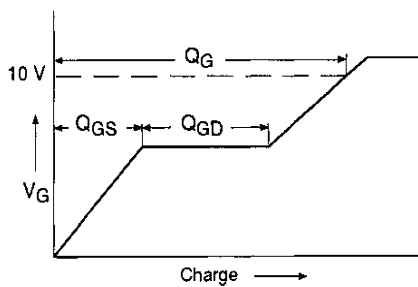


Fig 13a. Basic Gate Charge Waveform

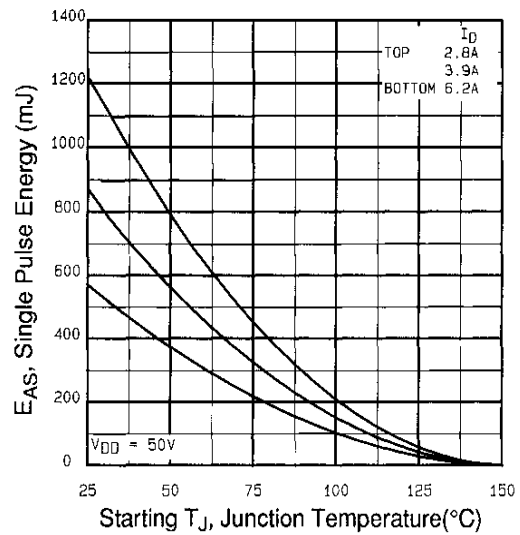


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

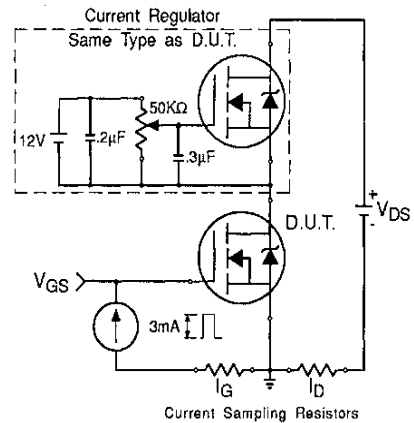
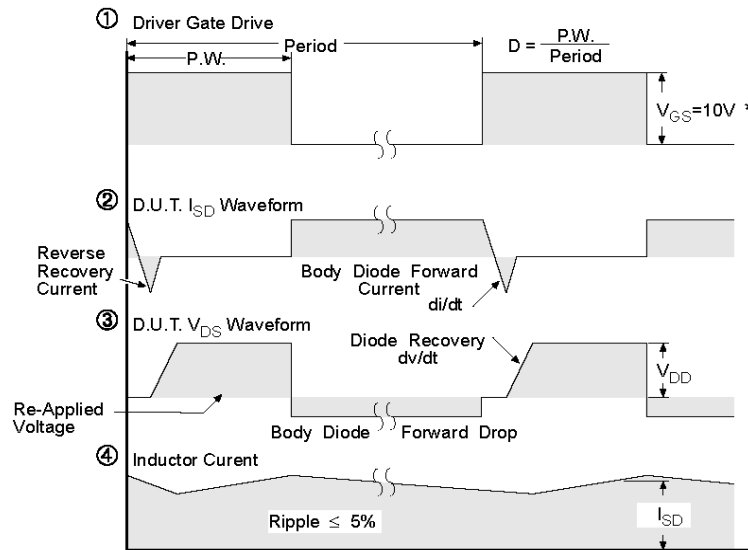
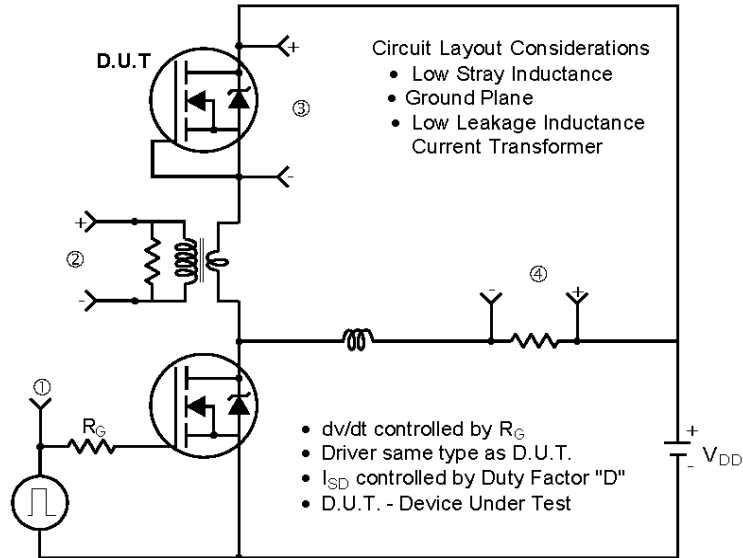


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit

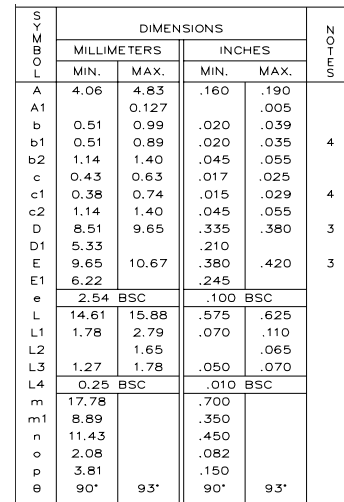


* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFETS

International
IOR Rectifier

Dimensions are shown in millimeters (inches)



HEXFET	IGBTs, CoPACK	DIODES
1.- GATE	1.- GATE	1.- ANODE *
2.- DRAIN	2.- COLLECTOR	2.- CATHODE
3.- SOURCE	3.- EMITTER	3.- ANODE

- PART DEPENDENT.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION: INCH.

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line position indicates "Lead-Free"

A diagram of a 530S integrated circuit package. The package is rectangular with a central notch. The text "F 530S" is printed at the top, "002L" is printed to the right of the center, "80" is printed at the bottom left, and "24" is printed at the bottom right. Two arrows point to the package: one to the left side and one to the bottom left corner. Below the package, there are two pins shown in cross-section.

PART NUMBER

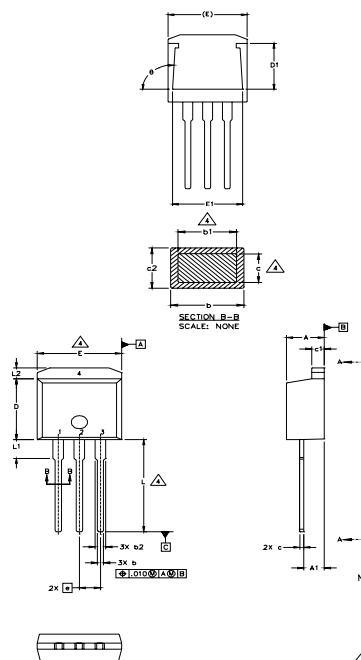
DATE CODE
YEAR 0 = 2000
WEEK 02
LINE L

OR

F 530S
ICR P002A
 80 24

PART NUMBER
 DATE CODE
 P = DESIGNATES LEAD-FREE
 PRODUCT (OPTIONAL)
 YEAR 0 = 2000
 WEEK 02
 A = ASSEMBLY SITE CODE

TO-262 Package Outline



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	4
A1	2.03	2.92	.080	.115	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.40	.045	.055	4
c	0.38	0.63	.015	.025	
c1	1.14	1.40	.045	.055	3
c2	0.43	.063	.017	.029	
D	8.51	9.65	.335	.380	
D1	5.33		.210		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	13.46	14.09	.530	.555	
L1	3.56	3.71	.140	.146	
L2		1.65		.065	

LEAD ASSIGNMENTS

HEXFET

- 1. - GATE
- 2. - DRAIN
- 3. - SOURCE
- 4. - DRAIN

IGBT

- 1 - GATE
- 2 - COLLECTOR
- 3 - EMITTER

NOTES:

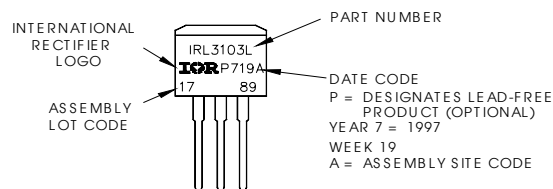
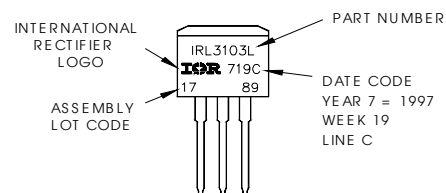
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION: INCH.

TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead-Free"

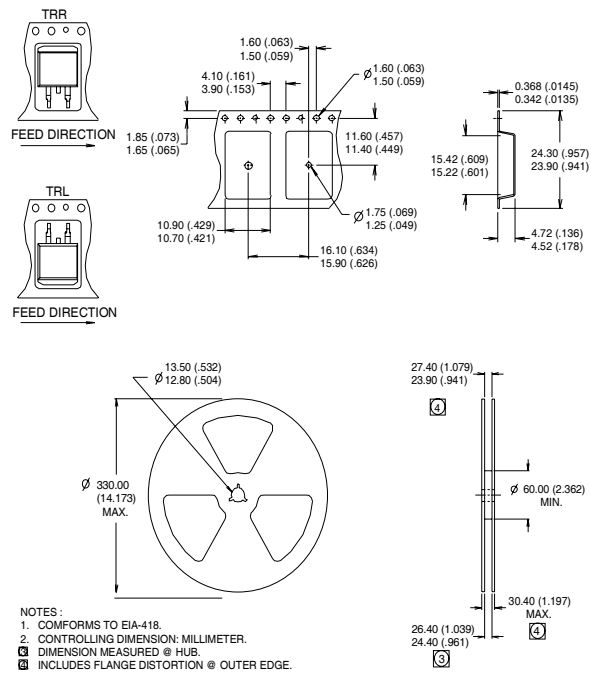
OR



IRFBC40S/LPbF

International
IOR Rectifier

D²Pak Tape & Reel Information



Data and specifications subject to change without notice.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105

TAC Fax: (310) 252-7903

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