# ZM7100 Series Digital Power Manager
# Data Sheet

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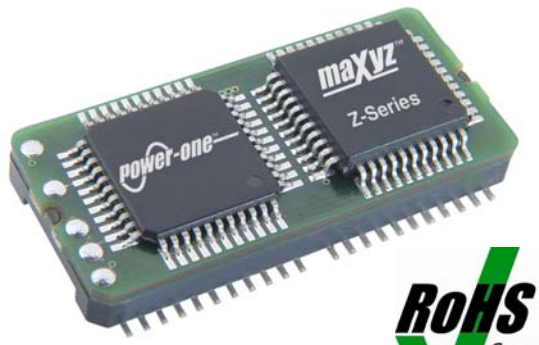
Changing the Shape of Power

## Member of the maXyz Family




RoHS Compliant

### Applications

- Low voltage, high density systems utilizing Z-One™ Digital Intermediate Bus Architectures
- Broadband, networking, optical, and communications systems
- Desktops, servers, and portable computing

### Benefits

- Eliminates the need for external power management components
- Communicates with the customer system via the industry standard $I^2C$ communication bus
- Reduces board space, system cost, complexity, and time to market

### Features

- RoHS lead-free and lead-solder-exempt products are available
- Programs, controls, and manages up to 32 independent Z-series POL converters
- Programs output voltage, protections, optimal voltage positioning, turn-on and turn-off delays and slew rates, switching frequency, interleave, and feedback loop compensation of the Z-POL converters
- User friendly GUI interface for programming, monitoring, and performance simulation
- Intermediate bus voltage monitoring and protection
- AC Fail input
- Up to four programmable interrupt inputs
- Ring buffer with programmable refresh rate to store real time voltage, current, and temperature measurements for up to 32 Z-POL converters
- Non-volatile memory to store system configuration information and status data
- 1 Kbytes of user accessible non-volatile memory
- Control of industry standard DC-DC front ends
- Crowbar output for optional crowbar protection
- Four independent OK lines for flexible fault management and fast fault propagation
- Small footprint horizontal SMT package: 32x16mm
- Low profile of 6.25mm
- Compatible with conventional pick-and-place equipment
- Wide operating temperature range

### Description

Power-One's point-of-load converters are recommended for use with regulated bus converters in an Intermediate Bus Architecture (IBA). The ZM7100 is a fully programmable digital power manager that utilizes the industry-standard $I^2C$ communication bus interface to control, manage, program and monitor up to 32 Z-series POL converters. The ZM7100 completely eliminates the need for external components for power management and POL converters programming, monitoring, and reporting. Parameters of the ZM7100 are programmable via the $I^2C$ bus and can be changed by a user at any time during product development and service.

### Selection Chart

| Part Number | Number of Z-series POLs that can be controlled | Active POL Addresses | Number of POL Groups | Number of Interrupts | Number of Parallel Buses |
|---|---|---|---|---|---|
| ZM7108 | 8 | 00…07 | 2 | 2 | 4 |
| ZM7116 | 16 | 00…15 | 3 | 3 | 4 |
| ZM7132 | 32 | 00…31 | 4 | 4 | 8 |

## 1. Reference Documents

- ZY7xxx Point of Load Regulator. Data Sheet
- ZM7100 Digital Power Manager. Programming Manual
- Z-OneTM Graphical User Interface

## 2. Ordering Information

| ZM | 71 | xx | G | – | yyyyy | Y | – | zz |
|---|---|---|---|---|---|---|---|---|
| **Product family:** Z-One Power Management Devices | **Series:** Digital Power Manager | **Total number of Z-One™ POLs that can be controlled:** **08** – 8 POLs **16** – 16 POLs **32** – 32 POLs | **RoHS compliance:** **No suffix** - RoHS compliant with Pb solder exemption[1] **G** - RoHS compliant for all six substances | | 5-digit identifier assigned by Power-One for each unique configuration file | **Optional:** Letter identifying configuration file revision level[2] | | **Packaging Option[3]:** **T1** – 500pcs T&R **T2** – 100pcs T&R **T3** – 50pcs T&R **R1** – 24pcs Tray **Q1** – 1pc sample for evaluation only |

[1] The solder exemption refers to all the restricted materials except lead in solder. These materials are Cadmium (Cd), Hexavalent chromium (Cr6+), Mercury (Hg), Polybrominated biphenyls (PBB), Polybrominated diphenylethers (PBDE), and Lead (Pb) used anywhere except in solder.

[2] Revision level identifier is optional and included for convenience of users. It is users' responsibility to order appropriate revision level. If no revision level identifier is added to the part number, the DPM will be programmed with the latest revision of the configuration file stored in the Power-One's database

[3] Packaging option is used only for ordering and not included in the part number printed on the DPM label.

Example: **ZM7116G-12345A-T1**: A 500-piece reel of 16-node RoHS-compliant DPMs with preloaded configuration file code 12345, revision A. Each DPM is labeled ZM7116G-12345A

## 3. Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings may cause performance degradation, adversely affect long-term reliability and cause permanent damage to the device.

| Parameter | Conditions/Description | Min | Max | Units |
|---|---|---|---|---|
| Ambient Temperature Range | | -40 | 85 | °C |
| Storage Temperature (Ts) | | -40 | 100 | °C |
| Input Voltage | IBV and IBV_S pins | 0 | 14.0 | VDC |
| Input Voltage | 3V3 pin | 0 | 3.8 | VDC |

## 4. Mechanical Specifications

| Parameter | Conditions/Description | Min | Nom | Max | Units |
|---|---|---|---|---|---|
| Weight | | | | 10 | grams |
| Peak Reflow Temperature | ZM7100 | | | 220 | °C |
| Peak Reflow Temperature | ZY7100G | | 245 | 260 | °C |
| Lead Plating | ZM7100 and ZM7100G | 1.5µm Ag over 1.5µm Ni | | | |
| Moisture Sensitivity Level | JEDEC J-STD-020C | 3 | | | |

## 5. Reliability Specifications

| Parameter | Conditions/Description | Min | Nom | Max | Units |
|---|---|---|---|---|---|
| MTBF | Calculated Per Telcordia Technologies SR-332 | 5.64 | | | MHrs |
| Non-Volatile Memory Endurance | -40°C to 85°C ambient<br>25°C ambient | | 10,000<br>100,000 | | Read-Write cycles |
| Data Retention | | | 40 | | years |

## 6. Electrical Specifications

### 6.1 Power Specifications

| Parameter | Conditions/Description | Min | Nom | Max | Units |
|---|---|---|---|---|---|
| High Input Supply Voltage | Continuous, IBV pin | 4.0 | | 14.0 | VDC |
| High Supply Voltage Reset | DPM stops operating, IBV pin | 3.36 | | 3.6 | VDC |
| High Reset Voltage Hysteresis | IBV pin | | 40 | | mVDC |
| Low Input Supply Voltage | Continuous, 3V3 pin | 3.0 | | 3.6 | VDC |
| Low Supply Voltage Reset | DPM stops operating, 3V3 pin | 2.646 | | 2.754 | VDC |
| Low Reset Voltage Hysteresis | 3V3 pin | | 135 | | mVDC |
| Input Current | $V_{IN}$ from 3.0V to 14V | | 42 | | mA |
| Output Current | 3V3 pin | | | 10 | mA |

### 6.2 Feature Specifications

| Parameter | Conditions/Description | Min | Nom | Max | Units |
|---|---|---|---|---|---|
| **Intermediate Voltage Bus Protections** | | | | | |
| Overvoltage Protection Threshold | Turns off all POLs, the Front End and triggers Crowbar | Programmable | | | |
| Undervoltage Protection Threshold | Turns off all POLs | Programmable | | | |
| **Front End Enable (FE_EN)** [1] | | | | | |
| $V_{FE\_EN}$ | Front End Enable | 2.5 | | VDD | VDC |
| Isrc | Source Current | | | 10 | mA |
| $V_{FE\_EN}$ | Front End Disable | | | 0.5 | VDC |
| Isink | Sink Current | | | 10 | mA |
| **Crowbar (CB)** [1] | | | | | |
| $V_{CB}$ | Crowbar Enable | 2.5 | | VDD | VDC |
| Isrc | Source Current | | | 10 | mA |
| $T_{CB}$ | Duration of Enabling Pulse | | 1 | | ms |

[1] At start-up of the DPM, the output is in the high impedance state. To avoid pulling the pin high due to capacitive coupling, it is recommended to connect a 3.3kOhm resistor between the pin and the Pin 24 GND.

## 6.3 Signal Specifications

| Parameter | Conditions/Description | Min | Nom | Max | Units |
|---|---|---|---|---|---|
| VDD | Internal supply voltage | 3 | 3.3 | 3.6 | V |
| **SYNC/DATA Line** | | | | | |
| ViL_sd | LOW level input voltage | -0.5 | | 0.8 | V |
| ViH_sd | HIGH level input voltage | 1.7 | | | V |
| VoL | LOW level output voltage<br>Isink=8mA | 0 | | 0.4 | V |
| Tf_sd | SD fall time<br>System requirement [1] | | | 75 | ns |
| Tr_sd | SD rise time<br>System requirement [1] | | | 250 | ns |
| Rpu_sd | Pull-up resistor | | 10 | | kΩ |
| Freq_sd | Clock frequency | 475 | | 525 | kHz |
| Tsynq | Sync pulse duration | 22 | | 28 | % of clock cycle |
| T0 | Data=0 pulse duration | 72 | | 78 | % of clock cycle |
| **Interrupt Inputs (INT0_N, INT1_N, INT2_N, INT3_N, AC_FAIL, RES_N)** | | | | | |
| Rup_x | Pull-up resistor | 17.5 | | 52.5 | kΩ |
| ViL_x | LOW level input voltage | -0.5 | | 0.35 x VDD | V |
| ViH_x | HIGH level input voltage | 0.7 x VDD | | VDD+0.5 | V |
| Vhyst_x | Hysteresis of input Schmitt trigger | 0.06XVDD | | | V |
| **I²C Address Inputs** | | | | | |
| Rup_ADDRx | Pull-up resistor | 17.5 | | 52.5 | kΩ |
| ViL_ADDRx | LOW level input voltage | -0.5 | | 0.35 x VDD | V |
| ViH_ADDRx | HIGH level input voltage | 0.7 x VDD | | VDD+0.5 | V |
| Vhyst_ADDRx | Hysteresis of input Schmitt trigger | 0.06xVDD | | | V |
| **Inputs/Outputs (OK_A, OK_B, OK_C, OK_D)** | | | | | |
| Rup_OKx | Pull-up resistor | 17.5 | | 52.5 | kΩ |
| ViL_Okx | LOW level input voltage | -0.5 | | 0.35 x VDD | V |
| ViH_Okx | HIGH level input voltage | 0.7 x VDD | | VDD+0.5 | V |
| Vhyst_OKx | Hysteresis of input Schmitt trigger | 0.06xVDD | | | V |

[1] The SD rise and fall time depends on the number of POL converters connected to the SD bus and the total board distribution capacitance. It is user's responsibility to ensure the fall and rise time specifications given in this table are met.

## 6.4 I²C Interface

| Parameter | Conditions/Description | Min | Nom | Max | Units |
|---|---|---|---|---|---|
| Data Transfer Rate | Standard according to I²C Bus Specifications Version 2.1 | | 100 | | kbit/s |
| ViH_I2C_Sxx | HIGH level input voltage on I2C_SCL and I2C_SDA lines | | | VDD+0.5 | V |
| Available Addresses | 4 MSBs hardwired<br>3 LSBs programmable | 50h, 52h, 54h, 56h, 58h, 5Ah, 5Ch, 5Eh | | | |

## 7. Typical Applications

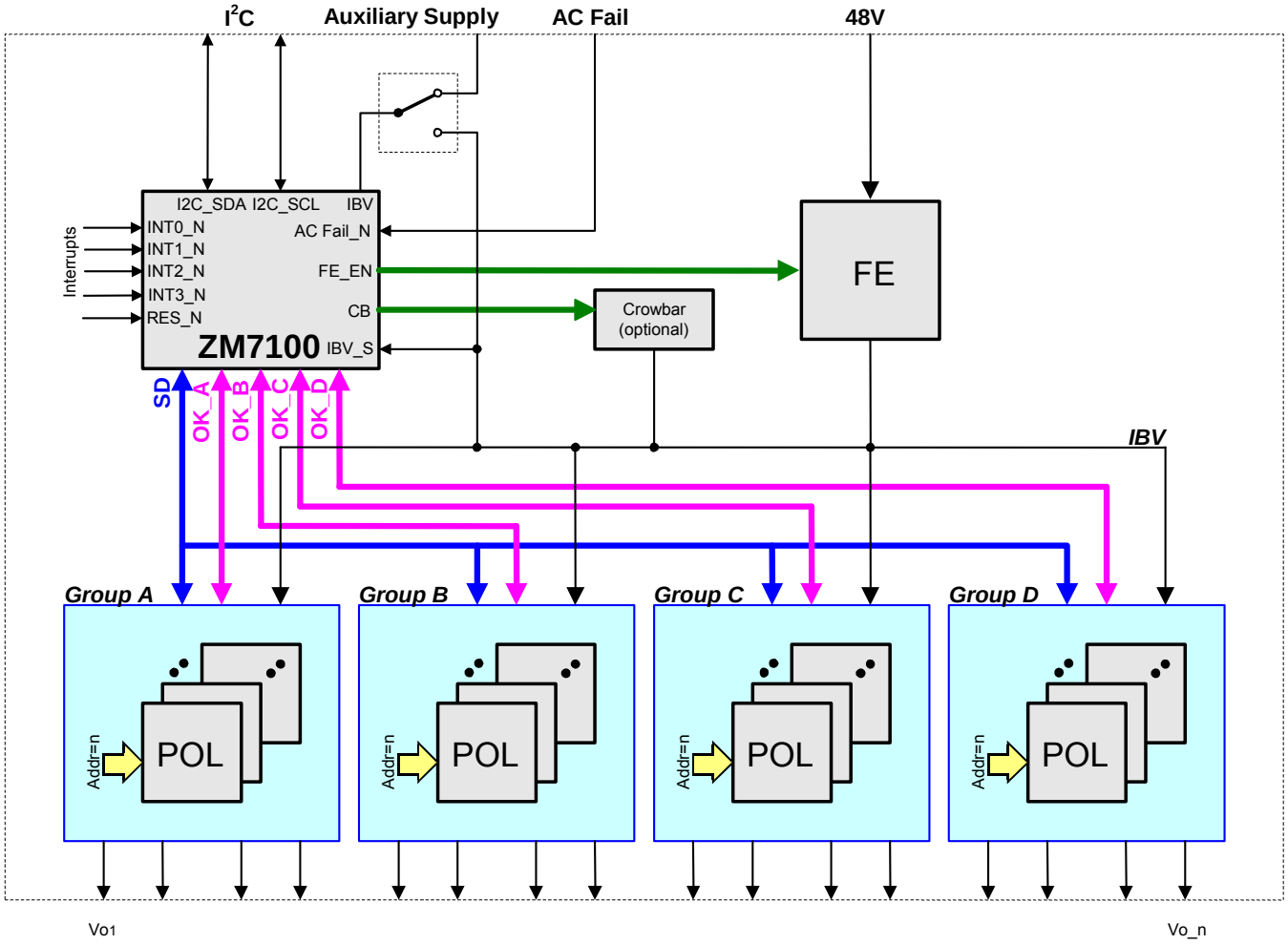



**Figure 1. Block Diagram of Typical Multiple Output Application with Digital Power Manager and I²C Interface**

The block diagram of a typical application of a ZM7100 digital power manager (DPM) is shown in Figure 1. The system may include up to 32 Z-series Point Of Load converters (POLs). Each POL converter has a unique 5-bit address programmed by grounding respective address pins. All POL converters are connected to the DPM and to each other via a single-wire synchronization/data (SD) communication bus. The bus provides synchronization of all POL converters to the master clock generated by the DPM and simultaneously performs bidirectional data transfer between the POL converters and the DPM. The DPM communicates in a bidirectional way via the I²C bus with the host system and/or ZIOS™ Graphical User Interface.

The DPM can be powered either directly from the intermediate voltage bus or from an independent voltage source. In this case the DPM can control a DC-DC Front End via the FE_EN pin. The DPM can also trigger an optional crowbar circuit and provide undervoltage and overvoltage protections of the intermediate bus voltage. In addition, the DPM can be controlled by a host system via the interrupt inputs and the AC-Fail input.

There are four groups of POL converters in the application. A group is defined as a number of POL converters interconnected via OK pins. Grouping of POL converters is optional, it enables users to program advanced fault management schemes and define margining functions, monitoring, startup behavior, and reporting conventions.

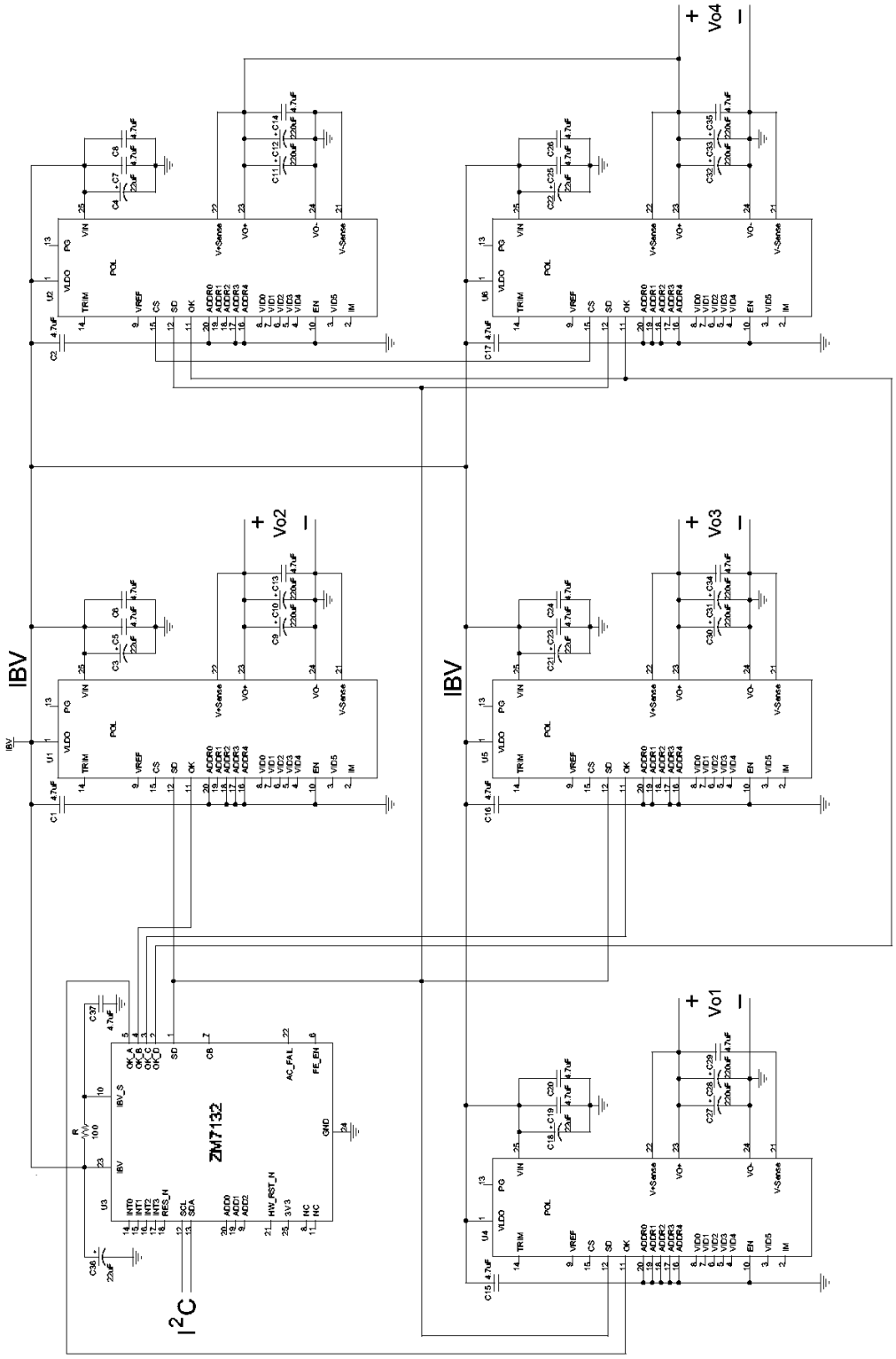



**Figure 2. Complete Schematic of a Multiple Output Application that Includes a High Power Output**

## 8. Pinout Diagram

| Pin Name | Pin No. | Pin Type | Buffer Type | Pin Description | Notes |
|---|---|---|---|---|---|
| SD | 1 | I/O | PU | SYNC/DATA communication line | Bidirectional I/O port |
| OKD[1] | 2 | I/O | PU | OK/FAULT line of POL group D | Bidirectional I/O port |
| OKC[2] | 3 | I/O | PU | OK/FAULT line of POL group C | Bidirectional I/O port |
| OKB | 4 | I/O | PU | OK/FAULT line of POL group B | Bidirectional I/O port |
| OKA | 5 | I/O | PU | OK/FAULT line of POL group A | Bidirectional I/O port |
| FE_EN | 6 | O | CMOS | Front End enable signal | |
| CB | 7 | O | CMOS | IBV crowbar signal | |
| NC | 8 | | | Not used | Leave Floating |
| ADD2 | 9 | I | PU | $I^2C$ Address bit 2 | |
| IBV_S | 10 | I | A | IBV sense | Connect to IBV |
| NC | 11 | | | Not used | Leave Floating |
| I2C_SCL | 12 | I/O | PU | Serial clock $I^2C$ interface | Bidirectional I/O port |
| I2C_SDA | 13 | I/O | PU | Serial data $I^2C$ interface | Bidirectional I/O port |
| INT0_N | 14 | I | PU | Interrupt 0, active low | |
| INT1_N | 15 | I | PU | Interrupt 1, active low | |
| INT2_N[2] | 16 | I | PU | Interrupt 2, active low | |
| INT3_N[1] | 17 | I | PU | Interrupt 3, active low | |
| RES_N | 18 | I | PU | Manual shutdown (active low) | |
| ADD1 | 19 | I | PU | $I^2C$ Address bit 1 | |
| ADD0 | 20 | I | PU | $I^2C$ Address bit 0 | |
| HW_RES_N | 21 | I | PU | DPM reset (active low) | |
| AC_FAIL_N | 22 | I | PU | AC-Fail interrupt (active low) | |
| IBV | 23 | P | --- | Supply Voltage | DPM Input Power Supply |
| GND | 24 | P | --- | Ground | |
| 3V3 | 25 | P | --- | 3.3V Input/Output | Output of the Internal Linear Regulator |

Legend: I=input, O=output, I/O=input/output, P=power, CMOS=CMOS output stage, A=analog, PU=internal pull-up

[1] ZM7132 only

[2] ZM7116 and ZM7132 only

## 9. Pins Description

**AC_FAIL_N, AC Fail Input (Pin 22):** A Schmitt-Trigger input with internal pull-up resistor (active low). Pulling low the input indicates to the DPM that an AC-DC front-end has lost the mains and that a system shut down should immediately be initiated.

**ADD[0:2], $I^2C$ Address Inputs (Pin 20, 19, 9):** Inputs with internal pull-up resistor. The 3 bit encoded address determines the Digital Power Manager's communication address for the $I^2C$ interface.

**CB, Crowbar Output (Pin 7):** A CMOS output which is used to trigger a crowbar (SCR) in case of overvoltage on the Intermediate Voltage Bus.

**FE_EN, Front-End Enable (Pin 6):** A CMOS output which is used to turn-on/off the DC/DC converter generating the IBV.

**HW_RES_N, Hardware Reset (Pin 21):** An input with internal pull-up resistor. When pulled low a cold start of the Digital Power Manager is initiated. This function should not be used to initiate normal system shutdown or turn-on.

**I2C_SDA, I2C_SCL, I2C Interface (Pin 13, 12).** Serial data (SDA) and clock (SCL) lines. Open drain input/outputs with internal pull-up resistors. The pins are not 5V tolerant; therefore, if external pull-ups are added, they must be connected to the 3V3 pin of the DPM.

**IBV_S, Intermediate Voltage Bus Sense (Pin 10):** Analog input to an internal ADC circuit to monitor the Intermediate Bus Voltage.

**INT[0:3]_N, Interrupts (Pin 14, 15, 16, 17):** Four active low inputs with internal pull-ups. Each of the inputs can be programmed to act as a remote enable for a specific group(s) of POL converters. When pulled low, the interrupt will turn-off respective POL converters. When the interrupt is released, the POL converters will turn-on according to their turn-on delay and slew rate settings.

**OKA, OKB, OKC, OKD, Group OK Signals (Pin 5, 4, 3, 2):** Open drain input/outputs with internal pull-up resistors. Pulling low the OK input will indicate to the DPM a fault in a Group. The DPM can also pull an OK line low to disable a Group of POL converters.

**RES_N, Active Low Reset Input (Pin 18):** An input with internal pull-up resistor. When pulled low a soft reset of the system (sequenced turn-off of all POL converters) is initiated. When released the whole system is reprogrammed and started (if Auto Turn-On is enabled).

**SD, Sync/Data Line (Pin 1):** An open drain input/output with internal pull-up resistor. Communication line to distribute a master clock and at the same time to communicate with all POL converters.

**3V3, VDD (Pin 25):** The output of the internal 3.3V linear regulator and input of an external 3.3V supply. Also used for additional pull-ups on SD, I2C_SDA and I2C_SCL lines

IBV, Positive Supply (Pin 23): Supply voltage.

GND, Ground (Pin 24): Ground.

**NC, No Connect (Pin 8, 11):** All NC pins must remain floating.

## 10. Digital Power Manager Description

The ZM7100 series DPMs perform translation between the $I^2C$ interface connected to a host system or the ZIOS™ Graphical User Interface and the SD communication bus connected to Z-series POL converters. In addition, DPMs carry out programming, monitoring, data storage, POL group management, protection, and control.

The DPMs can be controlled via the GUI or directly via the $I^2C$ bus by using high and low level commands as described in the '"ZM7100 DPM Programming Manual".

The DPM registers are listed in Table 1. The table relates to the digital power manager model number ZM7132 capable of supporting up to 32 POL converters. For other DPM models some of the registers and/or bits in the registers are not available depending on the number of supported POLs/Groups/Interrupts/Parallel Buses for the specific DPM. Writing into an unsupported register or bit will have no effect, reading from an unsupported register or bit will return a zero.

**Table 1. DPM Registers**

| Address Base + | Register Name | Content | Register Type | User Access | Write Protect | Initial Value |
|---|---|---|---|---|---|---|
| 0x00 | GAD[3:0] | Group A Definition | Static | R/W | yes | N/A |
| 0x04 | GBD[3:0] | Group B Definition | Static | R/W | yes | N/A |
| 0x08 | GCD[3:0] | Group C Definition | Static | R/W | yes | N/A |
| 0x0C | GDD[3:0] | Group D Definition | Static | R/W | yes | N/A |
| 0x10 | GAC | Group A Configuration | Static | R/W | yes | N/A |
| 0x11 | GBC | Group B Configuration | Static | R/W | yes | N/A |
| 0x12 | GCC | Group C Configuration | Static | R/W | yes | N/A |
| 0x13 | GDC | Group D Configuration | Static | R/W | yes | N/A |
| 0x14 | FPC1 | Fault Propagation Configuration 1 | Static | R/W | yes | N/A |
| 0x15 | FPC2 | Fault Propagation Configuration 2 | Static | R/W | yes | N/A |
| 0x16 | EPC | Error Propagation Configuration | Static | R/W | yes | N/A |
| 0x17 | IC1 | Interrupt Configuration 1 | Static | R/W | yes | N/A |
| 0x18 | IC2 | Interrupt Configuration 2 | Static | R/W | yes | N/A |
| 0x19 | IBL | IBV Low threshold | Static | R/W | yes | N/A |
| 0x1A | IBH | IBV high threshold | Static | R/W | yes | N/A |
| 0x8F | REL0 | DPM Software Release Low Byte | Static | R | | |
| 0x90 | REL1 | DPM Software Release High Byte | Static | R | | |
| 0x1B | ID0 | DPM ID Low Byte | Static | R | | 0xFF |
| 0x1C | ID1 | DPM ID High Byte | Static | R | | 0xFF |
| 0x1D | ADDR | System Controller Address | Static | R/W | yes | N/A |
| 0x1E | PB1[3:0] | Parallel Bus 1 | Static | R/W | yes | N/A |
| 0x22 | PB2[3:0] | Parallel Bus 2 | Static | R/W | yes | N/A |
| 0x26 | PB3[3:0] | Parallel Bus 3 | Static | R/W | yes | N/A |
| 0x2A | PB4[3:0] | Parallel Bus 4 | Static | R/W | yes | N/A |
| 0x2E | PB5[3:0] | Parallel Bus 5 | Static | R/W | yes | N/A |
| 0x32 | PB6[3:0] | Parallel Bus 6 | Static | R/W | yes | N/A |
| 0x36 | PB7[3:0] | Parallel Bus 7 | Static | R/W | yes | N/A |
| 0x3A | PB8[3:0] | Parallel Bus 8 | Static | R/W | yes | N/A |
| 0x3E | PID[31:0] | POL Identification | Static | R/W | yes | N/A |
| 0x80 | RTC[3:0] | Run Time Counter | Run time | R | | value at last shutdown |
| 0x84 | PPS[3:0] | POL Programming Status | Run time | R | | (4x) 0x00 |
| 0x88 | STA | Status of Group A | Run time | R | | 0x00 |
| 0x89 | STB | Status of Group B | Run time | R | | 0x00 |
| 0x8A | STC | Status of Group C | Run time | R | | 0x00 |
| 0x8B | STD | Status of Group D | Run time | R | | 0x00 |
| 0x8C | IMS | DPM Status | Run time | R | | 0x01 |
| 0x8D | EST | Event Status | Run time | R | | 0x00 |

| Address Base + | Register Name | Content | Register Type | User Access | Write Protect | Initial Value |
|---|---|---|---|---|---|---|
| 0x91 | LCMDS | Last Complete Monitoring Data Set | Run time | R | | Offset in Mon data where last set was stored |
| 0x8E | WP | Write Protection | Volatile | R/W | | 0x15 |

The static registers are saved in the non-volatile memory and used to store the system configuration data. The run-time registers contain status information and are evaluated during run-time. Their content is saved to the non-volatile memory together with monitoring data, but is not loaded into RAM when the DPM is powered up. The Write Protection register WP is a volatile register that defaults to write protect at power-up.

### 10.1 POL Programming

Performance parameters of Z-series POL converters can be programmed via the $I^2C$ communication bus without replacing any components or rewiring PCB traces. The POL programming data can be preloaded into DPMs by Power-One or DPMs can be programmed by the user via the GUI and the $I^2C$ bus. The DPMs can be programmed either before or after installation on a host board. The POL programming data (configuration settings) is stored in non-volatile memory. Memory registers are listed in Table 2.

**Table 2. POL Programming Memory**

| Address [1] | Register [1] | Content | Note |
|---|---|---|---|
| 00h | PC1_x | Protection Configuration 1 | |
| 01h | PC2_x | Protection Configuration 2 | |
| 02h | PC3_x | Protection Configuration 3 | |
| 03h | TC_x | Tracking Configuration | |
| 04h | INT_x | Interleave Configuration and Frequency Selection | |
| 05h | DON_x | Turn-On Delay | |
| 06h | DOF_x | Turn-Off Delay | |
| 07h | VOS_x | Output Voltage Set-point | |
| 08h | CLS_x | Current Limit Set-point | |
| 09h | DCL_x | Duty Cycle Limit | |
| 0Ah | B1_x | Dig Controller Denominator $z^{-1}$ Coefficient | 2's complement value |
| 0Bh | B2_x | Dig Controller Denominator $z^{-2}$ Coefficient | 2's complement value |
| 0Ch | B3_x | Dig Controller Denominator $z^{-3}$ Coefficient | 2's complement value |
| 0Dh | C0L_x | Dig Controller Numerator $z^{0}$ Coefficient Low Byte | 2's complement value |
| 0Eh | C0H_x | Dig Controller Numerator $z^{0}$ Coefficient High Byte | |
| 0Fh | C1L_x | Dig Controller Numerator $z^{-1}$ Coefficient Low Byte | 2's complement value |
| 10h | C1H_x | Dig Controller Numerator $z^{-1}$ Coefficient High Byte | |
| 11h | C2L_x | Dig Controller Numerator $z^{-2}$ Coefficient Low Byte | 2's complement value |
| 12h | C2H_x | Dig Controller Numerator $z^{-2}$ Coefficient High Byte | |
| 13h | C3L_x | Dig Controller Numerator $z^{-3}$ Coefficient Low Byte | 2's complement value |
| 14h | C3H_x | Dig Controller Numerator $z^{-3}$ Coefficient High Byte | |
| 15h-1Bh | | reserved | |
| 1Ch | VOL_x [2] | Output Voltage Margining Low Value | |
| 1Dh | VOH_x [2] | Output Voltage Margining High Value | |
| 1Eh | CRC0_x [2] | Cyclic Redundancy Check Register 0 | |
| 1Fh | CRC1_x [2] | Cyclic Redundancy Check Register 1 | |

[1] x denotes the POL address

[2] These registers are only used in the DPM and are not downloaded into POL converters during system programming

Refer to ZY7XXX data sheet for POL registers mapping and descriptions

Programming of POL converters is performed upon power-up, or when the Program Config… button is pressed in the GUI System Configuration window shown in Figure 3, or when the high level command is sent directly via the $I^2C$ bus.

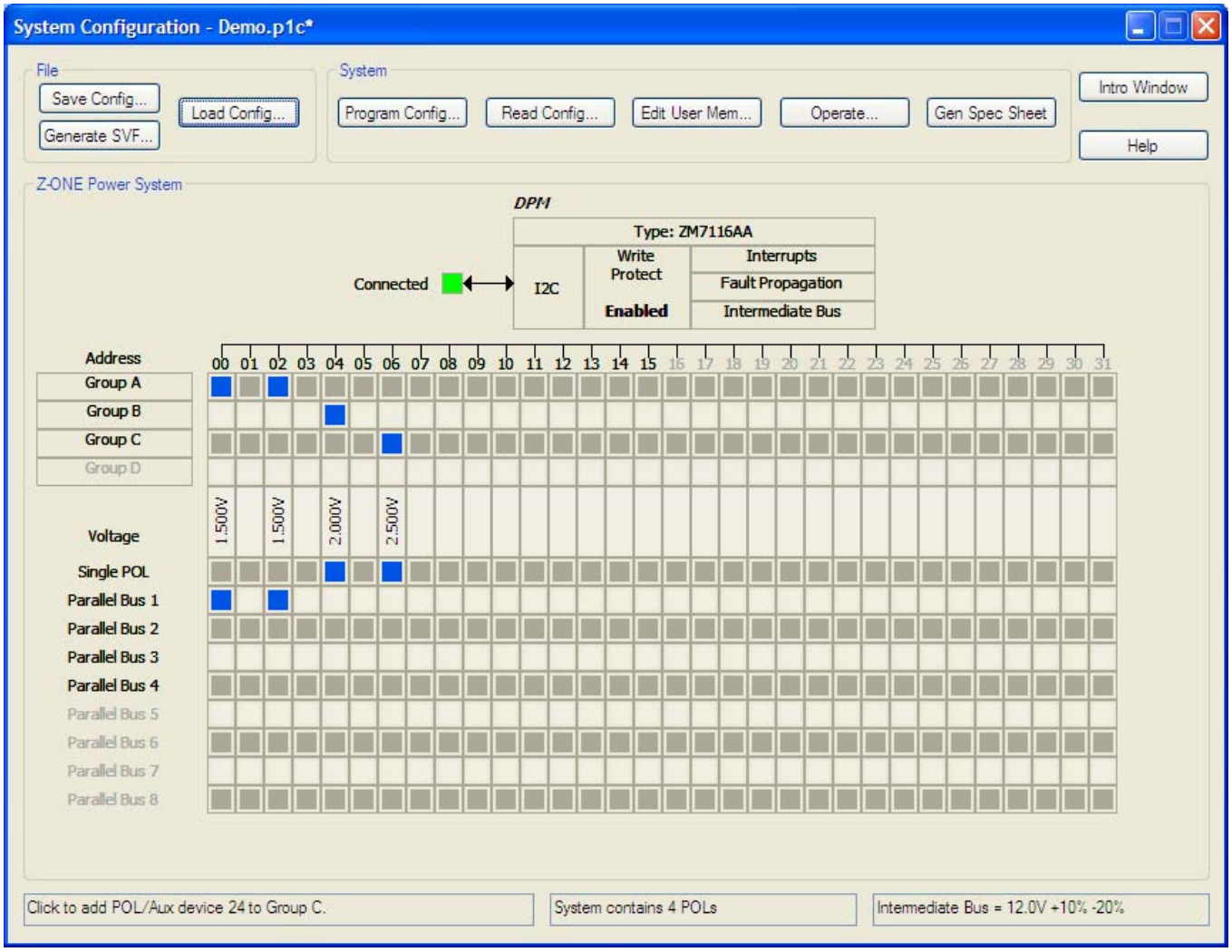



**Figure 3. System Configuration Window**

The programming is performed in several steps. Upon power-up, when the voltage on the IBV_S pin exceeds the undervoltage protection threshold, the DPM uploads programming data from its static registers into RAM. Then the DPM executes the cyclic redundancy check (CRC) to ensure integrity of the programming data. If the result is OK, then the programming data stored in registers 00h through 14h of the DPM is sent to the respective POL converter via the SD line. Every data transfer command is protected by parity check and followed by the POL acknowledgement and read data back procedure. If both acknowledgement and readback operations are successful, the POL converter is considered programmed, and the DPM continues with programming of the next POL converter. It takes DPM approximately 17ms to program one POL.

Upon completion of the programming cycle, programming status information is recorded in the registers PPS0-PPS3, and IMS shown in Figure 4 and Figure 5.

| Byte Address | PPS[3] Base | PPS[2] Base+1 | PPS[1] Base+2 | PPS[0] Base+3 |
|---|---|---|---|---|
| PPS | POL31 … POL24 | POL23 … POL16 | POL15 … POL8 | POL7 … POL0 |

**Figure 4. POL Programming Status Registers PPS0 and PPS1**

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-1 |
|---|---|---|---|---|---|---|---|
| ERR | FAULT | WAR | SP | SD | CRC | CB | FE |
| Bit 7 | | | | | | | Bit 0 |

Bit 7 **ERR**: Error bit
0 = no error
1 = error occured

Bit 6 **FAULT**: Fault bit
0 = no error
1 = fault occured

Bit 5 **WAR**: Warning bit
0 = no error
1 = warning occured

Bit 4 **SP**: System programmed successfully
0 = not all POLs are programmed
1 = all POLs were programmed successfully

Bit 3[1)] **SD**: Transmission error on SD interface
0 = no error
1 = error occurred

Bit 2[1)] **CRC**: CRC error after a memory check
0 = no error
1 = error occurred

Bit 1 **CB**: Crow-Bar (CB) output
0 = low
1 = high

Bit 0 **FE**: Front-End (FE) output
0 = low
1 = high

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

[1)] these bits are cleared when the register is read

**Figure 5. DPM Status Register IMS**

### 10.1.1 Write Protection

Figure 6 gives an overview of the different memory sections contained in the Z-One digital IBA system. A write protection register WP in the DPM limits the write access to the memory blocks in the DPM and the POL converters. The WP register content is defaulted to write protect upon powering up the DPM.

The write protection can be disabled by checking appropriate boxes in the Write Protections window shown in Figure 7 or via the $I^2C$ bus by writing directly into the Write Protection Register WP shown in Figure 8. The write protections are automatically restored when the DPM input power is recycled.

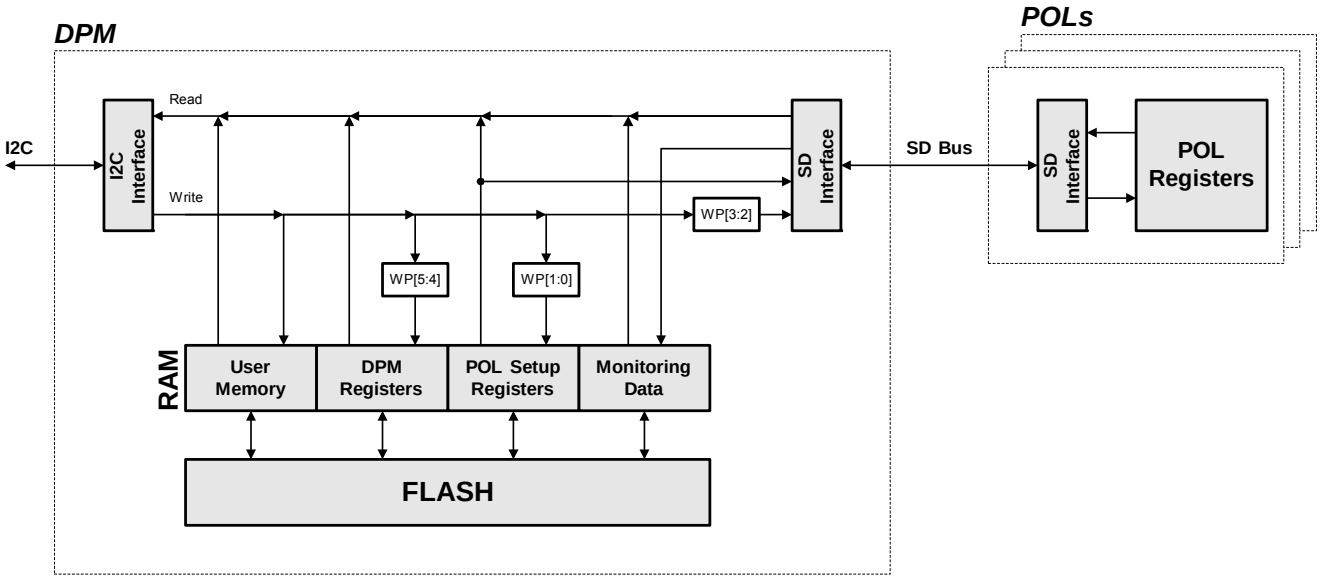



**Figure 6. DPM Memory and Write Protection**

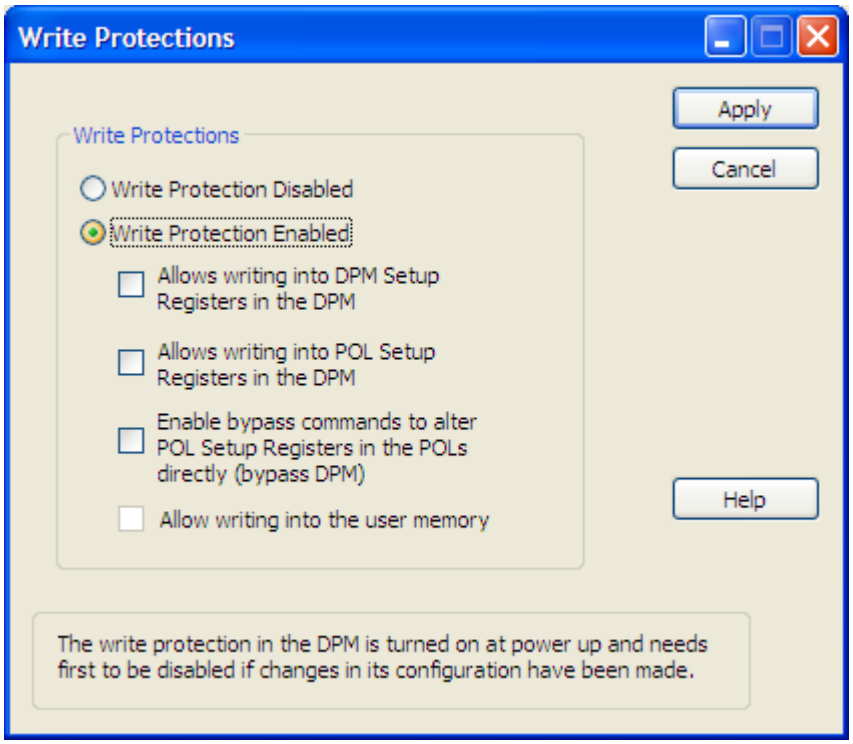



**Figure 7. Write Protections Window**

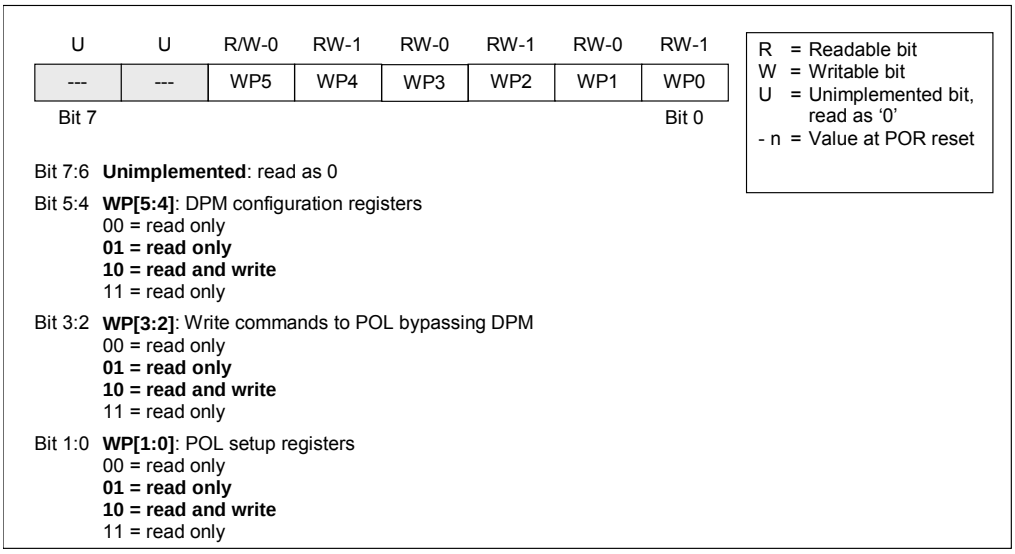



**Figure 8. Write Protection Register WP**

## 10.2 POL Monitoring

Z-series POL converters can monitor own performance parameters such as output voltage, output current, and temperature. Monitored parameters are stored in POL registers VOM, IOM, and TMON that are continuously updated. If monitoring is enabled, the DPM will be continuously copying POL status and parametric data into monitoring data registers. There are two blocks of POL monitoring memory as shown in Table 3. The first block contains 32 bytes representing the status registers of all POL converters. The second block contains monitoring data for each POL converter output voltage, output current, and temperature. For each parameter there is a ring buffer of 10 most recent values (3x10 values times 32 POLs=960 Bytes).

**Table 3. POL Monitoring Memory**

| Address | Register | Content |
|---|---|---|
| 00h | ST0[1)] | Status Register POL0 |
| 01h | ST1[1)] | Status Register POL1 |
| … | … | … |
| 1Eh | ST30[1)] | Status Register POL30 |
| 1Fh | ST31[1)] | Status Register POL31 |
| 20h | VO0[9:0] | Ring buffer Output Voltage POL0 |
| 30h | VO1[9:0] | Ring buffer Output Voltage POL1 |
| | … | … |
| 200h | VO30[9:0] | Ring buffer Output Voltage POL30 |
| 210h | VO31[9:0] | Ring buffer Output Voltage POL30 |
| 220h | IO0[9:0] | Ring buffer Output Current POL0 |
| 220h | IO1[9:0] | Ring buffer Output Current POL1 |
| … | … | |
| 400h | IO30[9:0] | Ring buffer Output Current POL30 |
| 410h | IO31[9:0] | Ring buffer Output Current POL31 |
| 420h | T0[9:0] | Ring buffer Temperature POL0 |
| 430h | T1[9:0] | Ring buffer Temperature POL1 |
| ... | ... | |
| 600h | T15[9:0] | Ring buffer Temperature POL30 |
| 610h | T31[9:0] | Ring buffer Temperature POL31 |

[1)] Initialized at BF at power-up

Monitoring is enabled by checking the Retrieve Monitoring bits in the GUI Group Configuration window shown in Figure 9 or directly via the $I^2C$ bus by writing into the respective Group Configuration Register GxC shown in Figure 10. Update frequency is 1Hz.

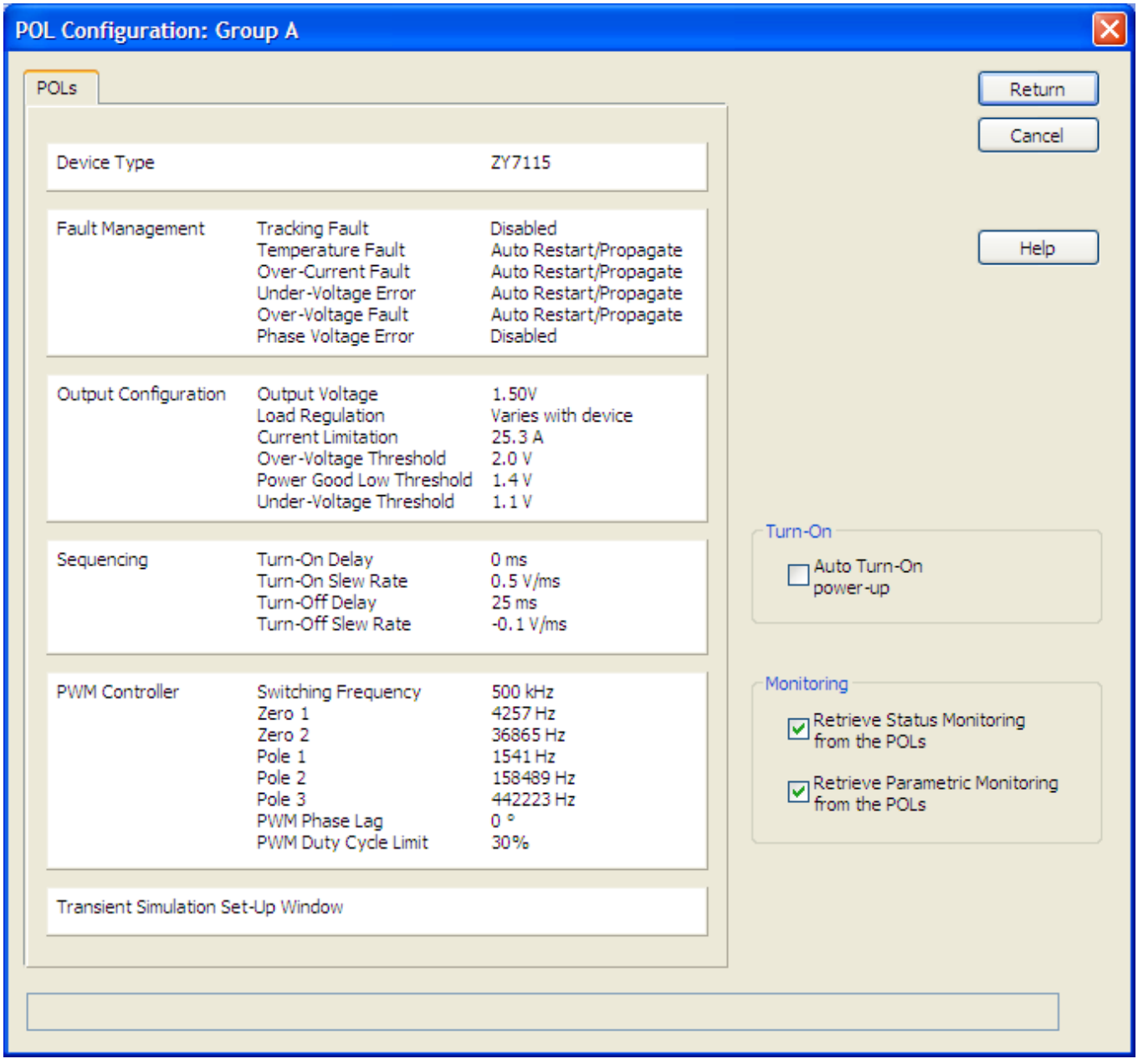



**Figure 9. POL Group Configuration Window**

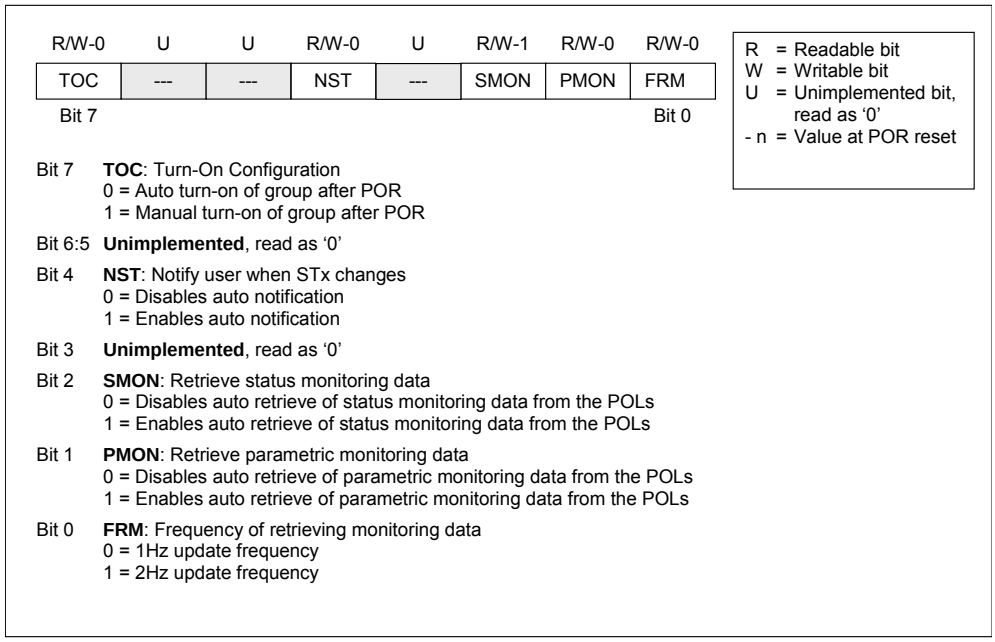



**Figure 10. Group Configuration Registers GxC**

### 10.2.1 Ring Buffer

In the case of system failure (IBV_L, IBV_H, AC_FAIL, RES_N), the data for 10 monitoring cycles immediately preceding the system shutdown is copied into the non-volatile ring buffer memory. After the system shutdown, the ring buffer can be accessed either via the GUI or directly via the $I^2C$ bus using high and low level commands. The data will be stored in the ring buffer until the next time the system is turned on therefore allowing for remote diagnostics and troubleshooting. Once the data is written into the ring buffer it cannot be overwritten until the DPM supply voltage is recycled or the ring buffer is cleared in GUI as shown in Figure 11 or directly via the $I^2C$ bus using high and low level commands.

Contents of the ring buffer can be displayed in the GUI IBS Monitoring Window shown in Figure 12 or can be read directly via the $I^2C$ bus using high and low level commands.

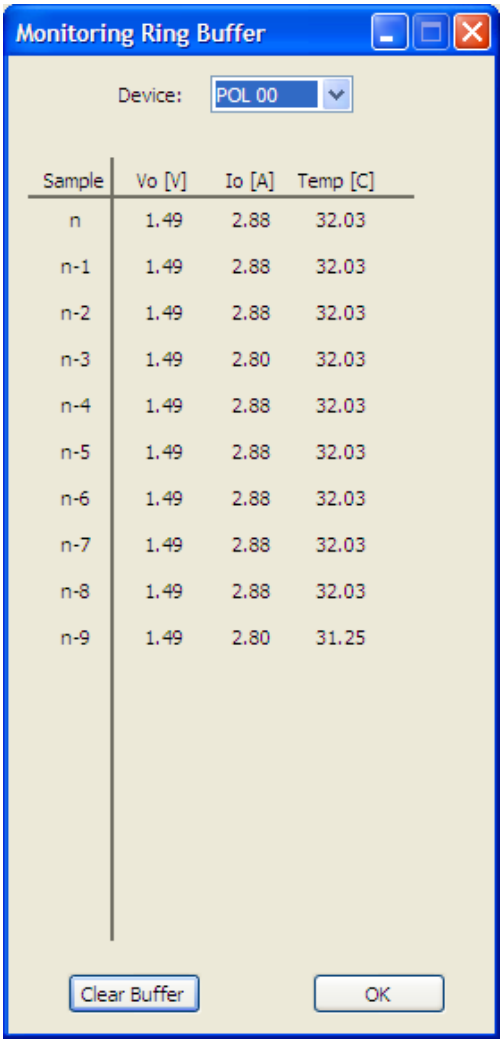



**Figure 11. Monitoring Ring Buffer**

### 10.2.2 Monitoring Setup

Retrieval of status and parametric monitoring data and update frequency are programmed in the GUI Group Configuration window shown in Figure 9 or directly via the $I^2C$ bus by writing into the respective Group Configuration Register GxC. Status and parametric monitoring data of a single POL regulator can be seen in the GUI IBS Monitoring Window shown in Figure 12 or directly via the $I^2C$ bus using the low level Read Monitoring Data command.

### 10.2.3 Run Time Counter

The DPM also monitors the duration of time that it has been in operation. The 4 bytes Run Time Counter is active whenever the DPM is powered up. The count rate is 1 second. New counter state is saved into non-volatile memory at least once per day of continuous operation. Contents of the counter can be examined in the GUI IBS Monitoring Window shown in Figure 12 or directly via the $I^2C$ bus using high and low level commands.

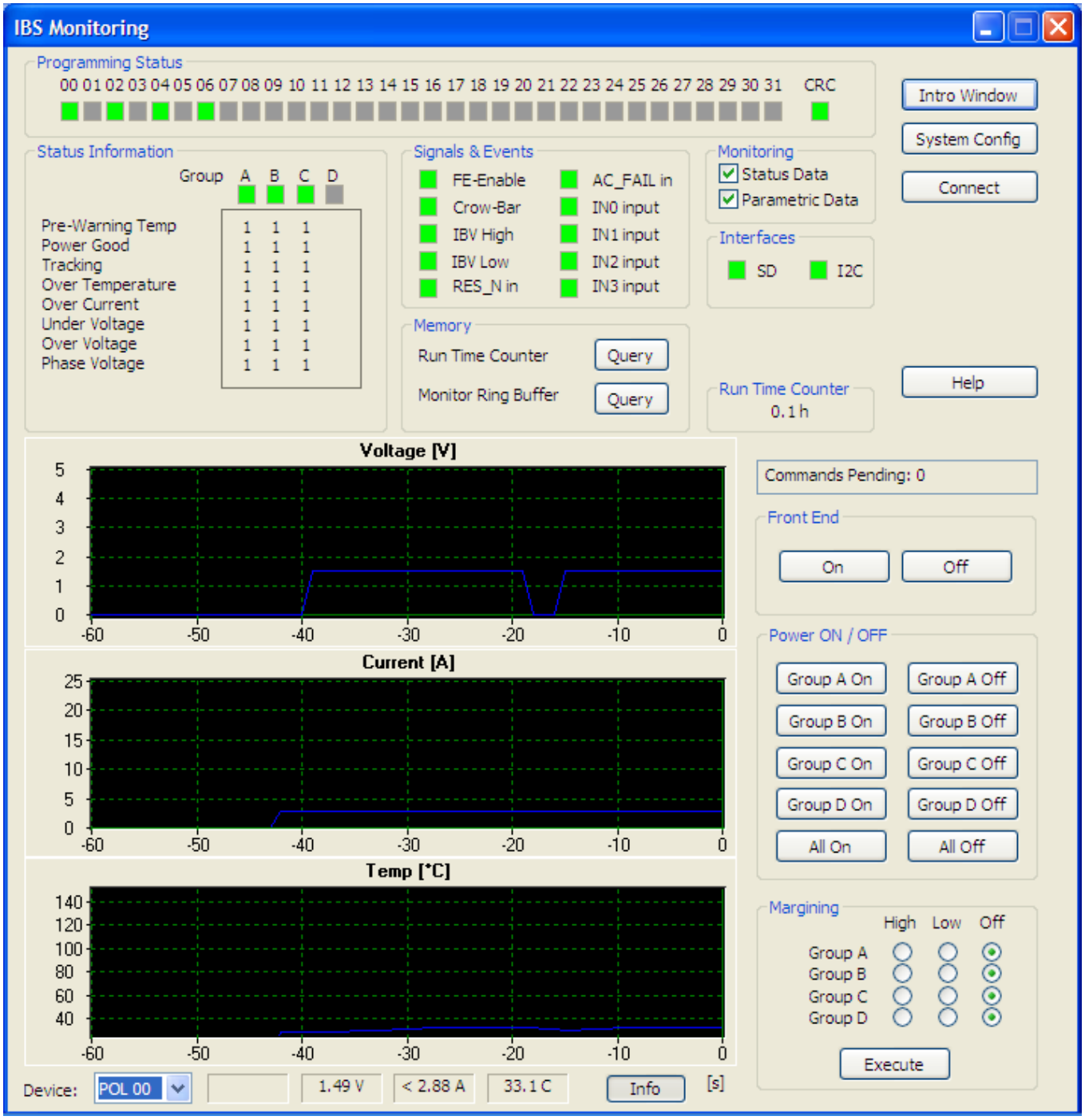



**Figure 12. IBS Monitoring Window**

### 10.3 POL Group Management

Z-series POL converters can be arranged in up to four groups. A group of POL converters is defined as a number of POL converters with interconnected OK pins. A group can include from 1 to 32 POL converters, but a POL converter can be a member of only one group. In addition, the OK lines can be connected to the DPM to facilitate

propagation of faults and errors between groups. One DPM can manage up to four independent groups of POL converters: A, B, C, and D, depending on the model.

Group management includes fault and error propagation, margining, turn-on and turn-off, monitoring setup, and interrupt configuration.

### 10.3.1 Fault and Error Propagation

To enable fault and error propagation between groups, the respective bit needs to be checked in the GUI Fault and Error Propagation window shown in Figure 13.

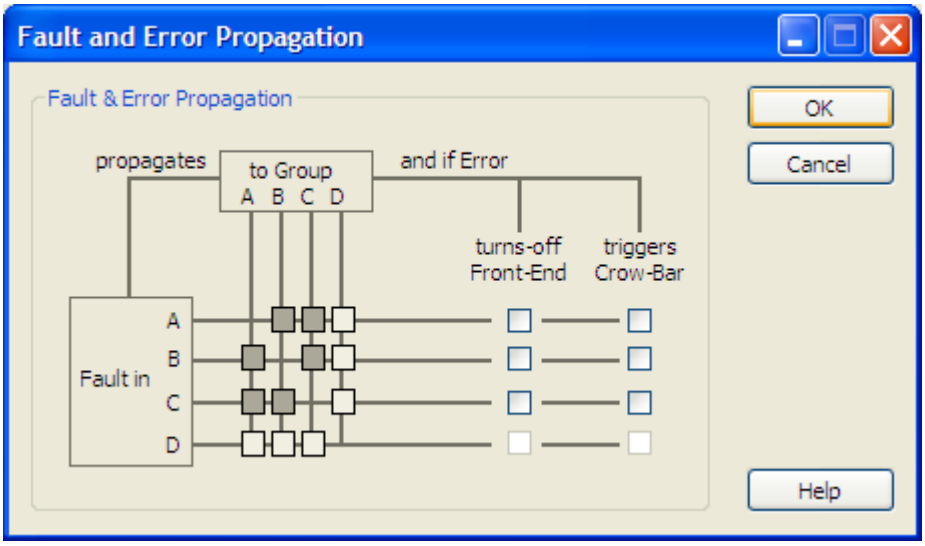



**Figure 13. Fault and Error Propagation Window**

The parameters can also be programmed directly via the $I^2C$ bus by writing into the FPC1, FPC2, and EPC registers shown in Figure 14, Figure 15, and Figure 16, respectively.

When propagation is enabled, the faulty POL converter pulls its OK pin low. A low OK line initiates turn-off of other POL converters in the group and signals the DPM to pull other OK lines low to initiate turn-off of other POL converters as programmed.

Propagation of a fault (overcurrent, undervoltage, overtemperature, and tracking) between groups initiates regular turn-off of other POL converters. The faulty POL converter in this case performs either the regular or the fast turn-off depending on a specific fault.

Propagation of an error (overvoltage or phase voltage error) initiates fast turn-off of other POL converters. The faulty POL converter performs the fast turn-off and turns on its low side switch. In addition, when an error is propagated, the DPM can generate commands to turn off a front end (a DC-DC converter generating the intermediate bus voltage) and trigger an optional crowbar protection to accelerate removal of the intermediate bus voltage (IBV).

| R/W-0 | R/W-0 | U | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U |
|---|---|---|---|---|---|---|---|
| FPBD | FPBC | --- | FPBA | FPAD | FPAC | FPAB | --- |
| Bit 7 | | | | | | | Bit 0 |

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

Bit 7 **FPBD**: Fault propagation from Group B to Group D
0 = disabled
1 = enabled

Bit 6 **FPBC**: Fault propagation from Group B to Group C
0 = disabled
1 = enabled

Bit 5 **Unimplemented**: read as '0'

Bit 4 **FPBA**: Fault propagation from Group B to Group A
0 = disabled
1 = enabled

Bit 3 **FPAD**: Fault propagation from Group A to Group D
0 = disabled
1 = enabled

Bit 2 **FPAC**: Fault propagation from Group A to Group C
0 = disabled
1 = enabled

Bit 1 **FPAB**: Fault propagation from Group A to Group B
0 = disabled
1 = enabled

Bit 0 **Unimplemented**: read as '0'

**Figure 14. Fault Propagation Configuration Register FPC1**

| U | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| --- | FPDC | FPDB | FPDA | FPCD | --- | FPCB | FPCA |
| Bit 7 | | | | | | | Bit 0 |

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

Bit 7 **Unimplemented**: read as '0'

Bit 6 **FPDC**: Fault propagation from Group D to Group C
0 = disabled
1 = enabled

Bit 5 **FPDB**: Fault propagation from Group D to Group B
0 = disabled
1 = enabled

Bit 4 **FPDA**: Fault propagation from Group D to Group A
0 = disabled
1 = enabled

Bit 3 **FPCD**: Fault propagation from Group C to Group D
0 = disabled
1 = enabled

Bit 2 **Unimplemented**: read as '0'

Bit 1 **FPCB**: Fault propagation from Group C to Group B
0 = disabled
1 = enabled

Bit 0 **FPCA**: Fault propagation from Group C to Group A
0 = disabled
1 = enabled

**Figure 15. Fault Propagation Register FPC2**

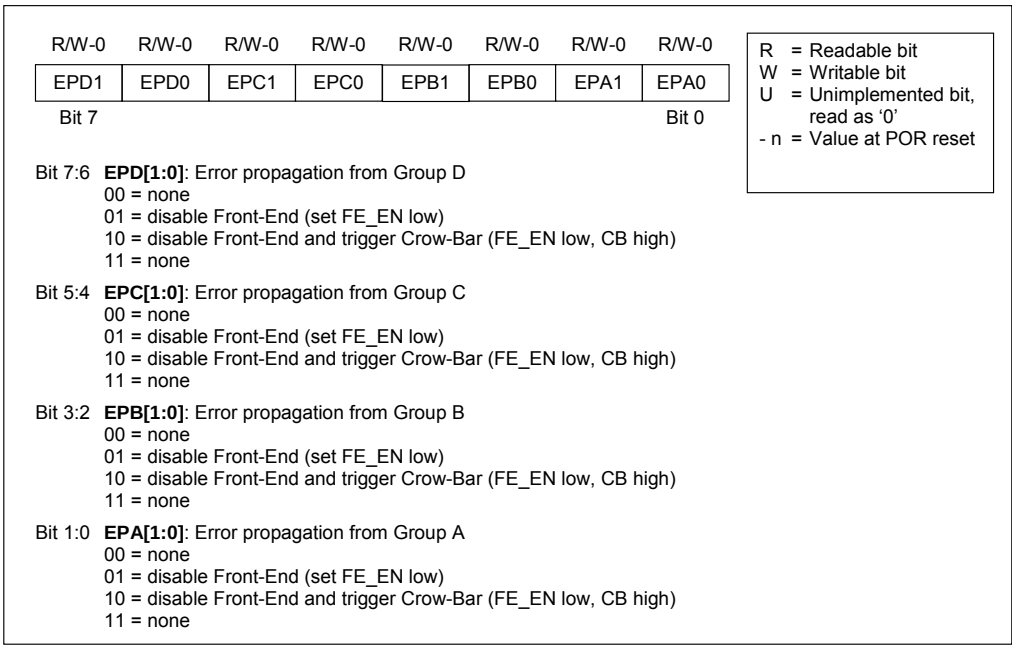



**Figure 16. Error Propagation Register EPC**

Group status information is stored in the Group Status Registers STA, STB, STC, and STD shown in Figure 17.

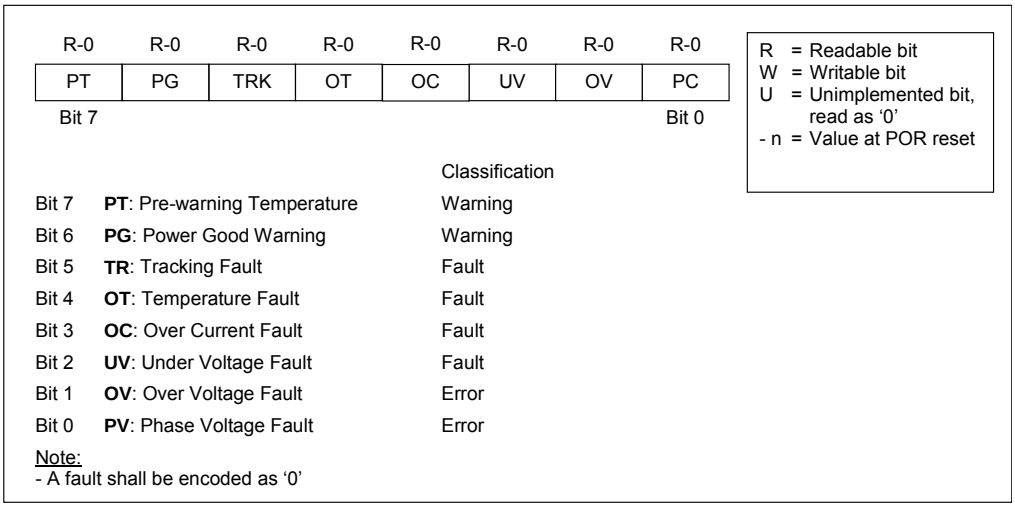



**Figure 17. Group Status Reference Registers STx**

### 10.3.2 Margining

Margining can be executed separately for each group by clicking an appropriate radio button in the GUI IBS monitoring window or directly via the $I^2C$ bus by high level commands.

### 10.3.3 Turn-ON and Turn-Off commands

Automatic turn–on upon application of the input voltage is enabled by checking the Auto Turn-On bit in the GUI Group Configuration window shown in Figure 9 or directly via the $I^2C$ bus by writing into the respective Group Configuration Register GxC register shown in Figure 10.

Turn-on and turn-off of various groups during the operation is controlled from the GUI IBS Monitoring window or directly via the $I^2C$ bus by high level commands. If the commands are used, POL converters will turn on and off according to their tracking and sequencing settings. If the Emergency Turn Off command is used the POL converters will perform the fast turn-off. In this case, the POL converters will immediately turn off both switches and output voltages will decay depending on load parameters.

### 10.3.4 Interrupt Configurations

The DPM has four interrupt inputs that allow temporary turn-off of POL groups by pulling the interrupts inputs low. The interrupts are enabled in the GUI Interrupt Configuration window shown in Figure 18 or directly via the $I^2C$ bus by writing into the Interrupt Configuration registers IC1 and IC2 shown in Figure 19.

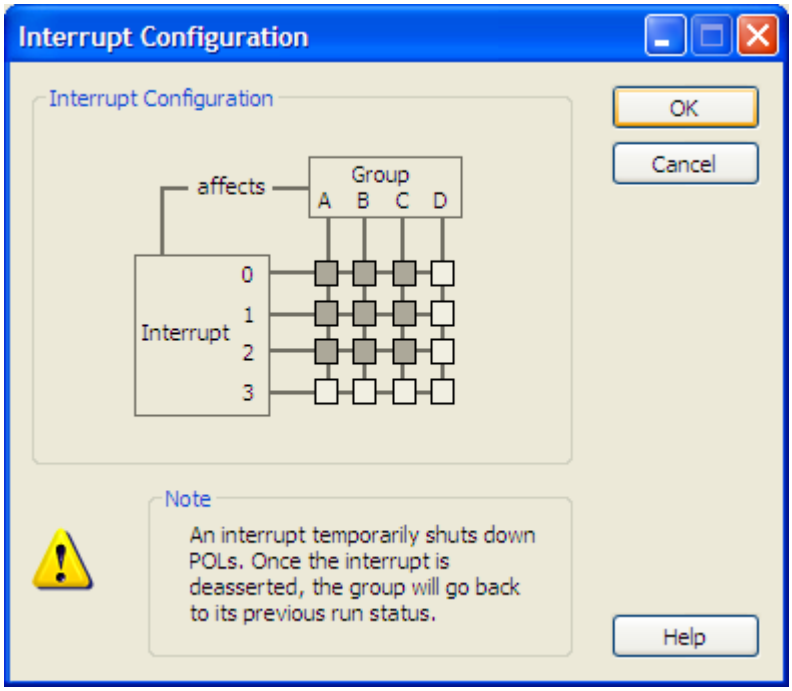



**Figure 18. Interrupt Configuration Window**

| R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-1 |
|---|---|---|---|---|---|---|---|
| I2D | I2C | I2B | I2A | I1D | I1C | I1B | I1A |
| Bit 7 | | | | | | | Bit 0 |

Bit 7 **I1D**: Interrupt 1 propagation to Group D
0 = disabled
1 = enabled

Bit 6 **I1C**: interrupt 1 propagation to Group C
0 = disabled
1 = enabled

Bit 5 **I1B**: interrupt 1 propagation Group B
0 = disabled
1 = enabled

Bit 4 **I1A**: Interrupt 1 propagation Group A
0 = disabled
1 = enabled

Bit 3 **I0D**: Interrupt 0 propagation to Group D
0 = disabled
1 = enabled

Bit 2 **I0C**: interrupt 0 propagation to Group C
0 = disabled
1 = enabled

Bit 1 **I0B**: interrupt 0 propagation Group B
0 = disabled
1 = enabled

Bit 0 **I0A**: Interrupt 0 propagation Group A
0 = disabled
1 = enabled

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

| R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| I4D | I4C | I4B | I4A | I3D | I3C | I3B | I3A |
| Bit 7 | | | | | | | Bit 0 |

Bit 7 **I3D**: Interrupt 3 propagation to Group D
0 = disabled
1 = enabled

Bit 6 **I3C**: interrupt 3 propagation to Group C
0 = disabled
1 = enabled

Bit 5 **I3B**: interrupt 3 propagation Group B
0 = disabled
1 = enabled

Bit 4 **I3A**: Interrupt 3 propagation Group A
0 = disabled
1 = enabled

Bit 3 **I2D**: Interrupt 2 propagation to Group D
0 = disabled
1 = enabled

Bit 2 **I2C**: interrupt 2 propagation to Group C
0 = disabled
1 = enabled

Bit 1 **I2B**: interrupt 2 propagation Group B
0 = disabled
1 = enabled

Bit 0 **I2A**: Interrupt 2 propagation Group A
0 = disabled
1 = enabled

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

**Figure 19. Interrupt Configuration Registers IC1 (left) and IC2**

## 10.4 Protections

The DPM provides undervoltage and overvoltage protections for the intermediate voltage bus, support error protection by controlling a front end and a crowbar circuit, and perform controlled system shutdown in case of the main AC-DC failure.

### 10.4.1 Intermediate Voltage Bus Protections

The DPM continuously monitors the intermediate bus voltage via the IBV_S input. Thresholds of IBV protections are programmed in the GUI Intermediate Bus Configuration Window shown in Figure 20 or directly via the I2C bus by writing into the IBV Low Threshold and High Threshold IBH registers IBL and IBV shown in Figure 21.

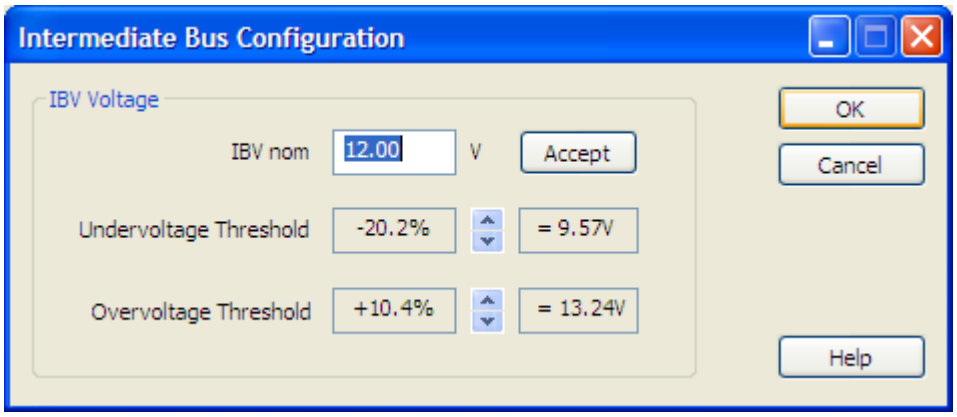



**Figure 20. Intermediate Bus Configuration Window**

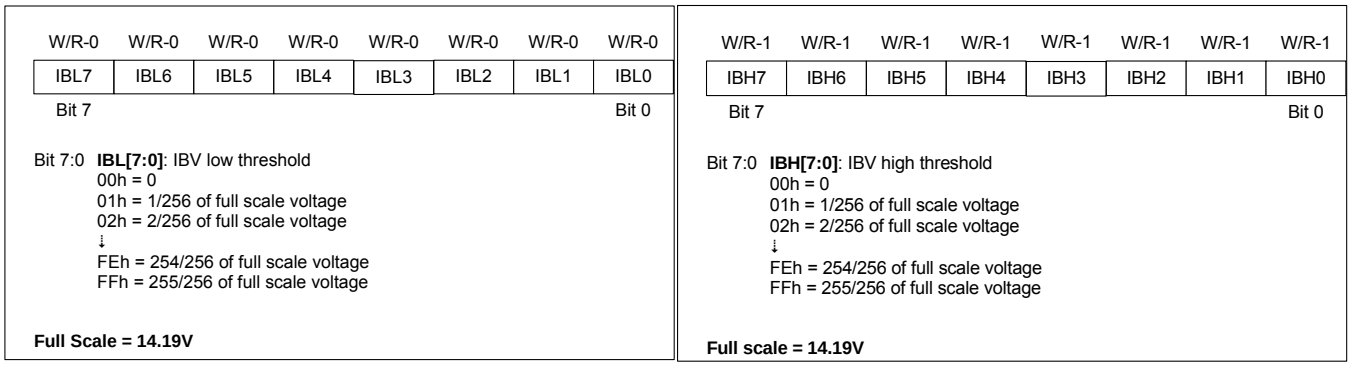



**Figure 21. IBV Low Threshold Register IBL (left) and IBV High Threshold Register IBH**

When the IBV decreases below the IBV Low Threshold, the DPM will pull all OK lines low turning off all POL converters. The POL converters will enter regular turn-off sequence. Contents of the Ring Buffer will be saved in non-volatile memory. When the IBV recovers, the DPM will first reprogram all POL converters and then turn them on, if the Auto Turn On is enabled in the GUI POL Group Configuration Window.

When the IBV exceeds the IBV High Threshold, the DPM will pull all OK lines low turning off all POL converters. The POL converters will enter regular turn-off sequence. Contents of the Ring Buffer will be saved in non-volatile memory. After a delay (typically 50ms), the DPM will turn off the front end. If the voltage does not decrease below the threshold within the next 50ms, the DPM will trigger the crowbar protection. One second after clearing the IBV High fault, the DPM will attempt to turn on the front end. If the IBV is within limits, the DPM will reprogram all POL converters and then turn them on, if the Auto Turn On is enabled in the GUI POL Group Configuration Window.

### 10.4.2 AC_Fail Protection

The AC_Fail signal is generated by a main AC-DC source supplying 48V backplane voltage that in turn powers the DC-DC Front End. Whenever the AC voltage disappears, the AC-Fail signal will be set low. If there is no battery backup, it means the 48V will disappear after 20ms. When DPM receives the AC_Fail signal, it will pull all OK lines low, turning off all POL converters. The POL converters will enter regular turn-off sequence. Contents of the Ring Buffer will be saved in non-volatile memory. When the AC voltage recovers and the AC_Fail goes high, the DPM will reprogram all POL converters and then turn them on, if the Auto Turn On is enabled in the GUI POL Group Configuration Window.

## 10.5 Controls

### 10.5.1 Front End Enable

The FE_EN pin is dedicated to the control of a DC-DC Front End. The Front End is typically used to convert the 48V into the intermediate bus voltage. If the DPM is powered from an auxiliary source, not from the IBV, it can control the Front End.

When FE_EN is internally pulled up to 3V, the Front End is enabled. The FE_EN output can provide up to 10mA of current. When the FE_EN goes below 0.5V, the Front End is disabled. The Front End can be enabled and disabled via the GUI IBS Monitoring Window or directly via the $I^2C$ bus using high and low level commands.

The FE_EN pin should not be directly connected to the Front End Enable pin. Typically, the Enable pin is referenced to the primary side of the Front End that is isolated from low voltage secondary side. In addition, the Enable pin can be pulled up internally to a voltage potentially damaging to the DPM FE_EN output. The best method is to interface the DPM with the Front End through an optocoupler as shown in Figure 22. This configuration provides interface for negative logic front ends. The 3.3k resistor was added between the FE_EN pin and the ground to avoid a glitch during application of input voltage to the DPM.

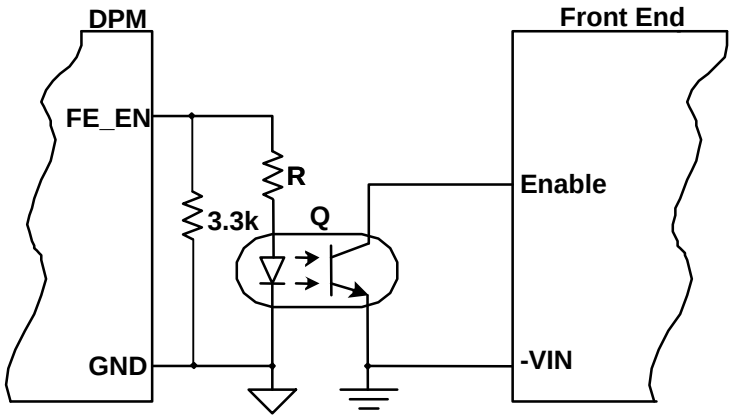



**Figure 22. Interface Between DPM and Front End**

### 10.5.2 Crowbar Enable

When the crowbar protection is enabled, the CB pin goes to 3V for 1ms. It is capable of supplying 10mA to turn on a crowbar circuit.

### 10.5.3 RES_N

If the RES_N pin is pulled low, the DPM will pull all OK lines low, turning off all POL converters. The POL converters will enter regular turn-off sequence. Contents of the Ring Buffer will be saved in non-volatile memory. Releasing the RES_N will first reprogram all POL converters and then turn them on, if the Auto Turn-On is enabled in the GUI POL Group Configuration Window.

## 10.6 User Memory

This non-volatile memory block is reserved for users' notes and it is not related to other functions in the DPM. It can be used to save application information such as manufacturing data and location, application code, configuration file version, etc. A total of 1024 Bytes of user memory is provided. The user memory can be accessed via the GUI System Configuration window shown in Figure 3, or directly via the $I^2C$ bus using high and low level commands.

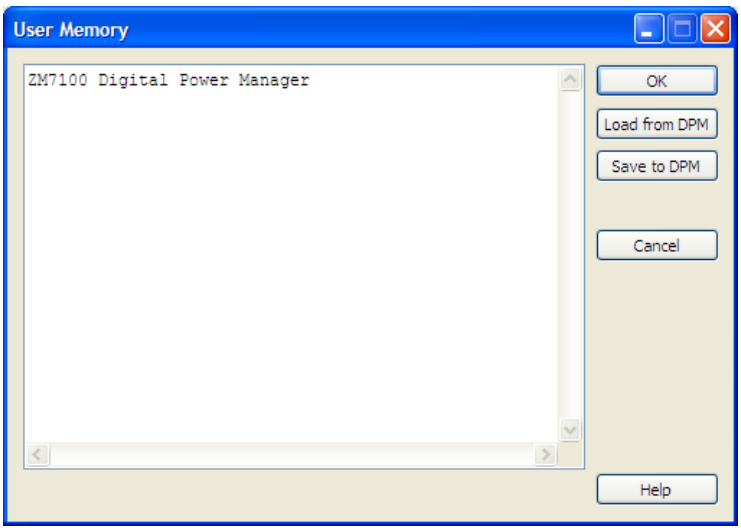



**Figure 23. User Memory Window**

## 11. Application Information

### 11.1 Powering the DPM

The DPM can be powered directly from the intermediate voltage bus (IBV) or from an auxiliary source such as a housekeeping, standby, or backplane supply. In applications where the DPM is used to control the front end generating IBV and/or the crowbar, the DPM must be powered from an auxiliary source.

If the intermediate bus voltage exceeds 4.0V, the DPM can be powered directly from the IBV via Pin 23. Schematic in Figure 24 shows power connections when the DPM input voltage is supplied directly by IBV. A low-pass RC-filter is added to increase noise immunity of the voltage sense line.

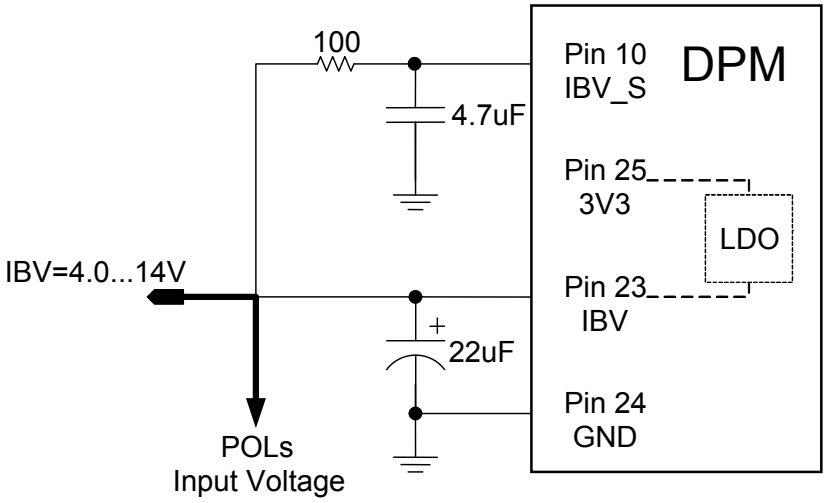



**Figure 24. Power Connections for IBV>4.0V**

If the DPM is powered by an auxiliary source higher than 4.0V, the IBV voltage range can be extended to 3.0 to 14V as shown in Figure 25.

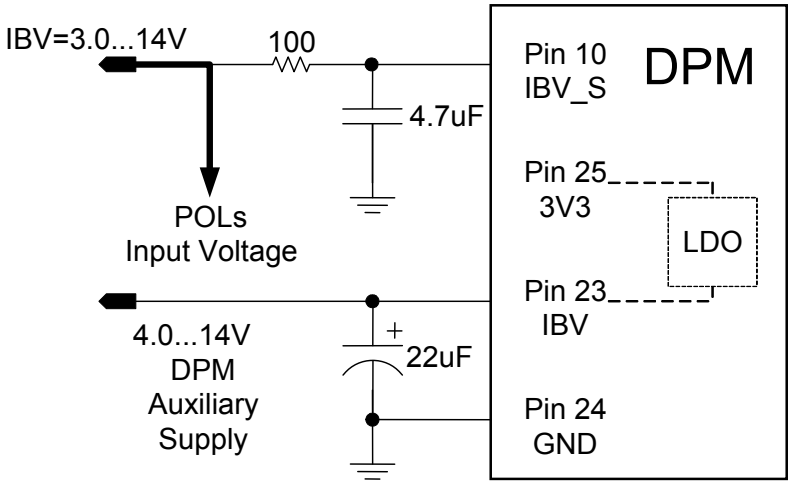



**Figure 25. Power Connections For Application With Auxiliary Source Higher Than 4.0V**

In applications where the DPM is powered from a 3.3V auxiliary supply, the schematic in Figure 25 needs to be modified by adding a jumper between Pin 23 and Pin 25 as shown in Figure 26. This effectively shorts the internal linear regulator and applies the voltage directly to the DPM ASICs. It is user's responsibility to ensure the voltage on Pin 25 never exceeds specified limits.

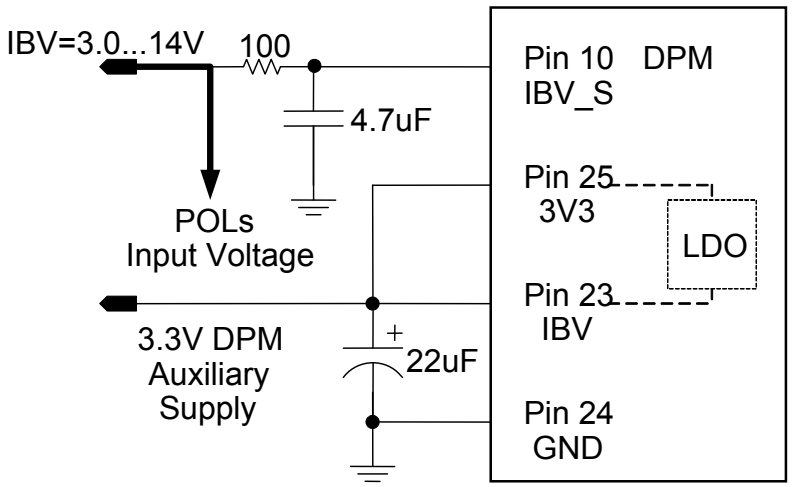



**Figure 26. Power Connections For Application With 3.3V Auxiliary Source**

In applications where the intermediate voltage bus is 3.3V, both the DPM and POL converters can be powered directly from the IBV as shown in Figure 27.

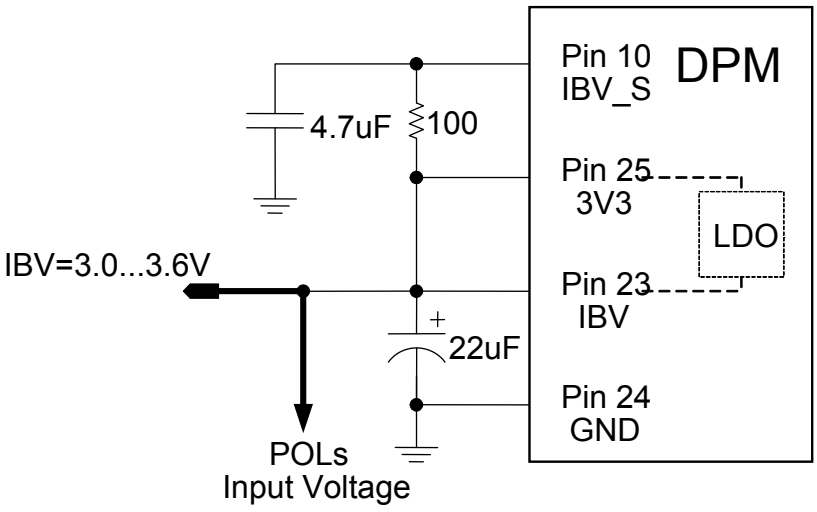



**Figure 27. Power Connections for IBV=3.3V**

## 12. Mechanical Drawings

**All Dimensions are in mm**

**Tolerances:**

**0.5-10 ±0.1**

**10-100 ±0.2**

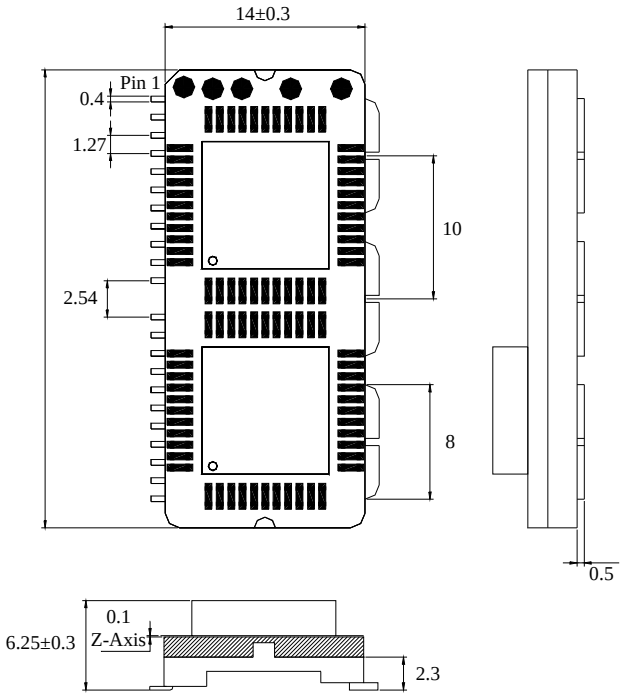



**Figure 28. ZM7100 Mechanical Drawing – Top View**

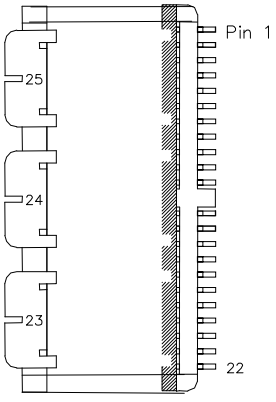



**Figure 29. ZM7100 Mechanical Drawing – Bottom View**

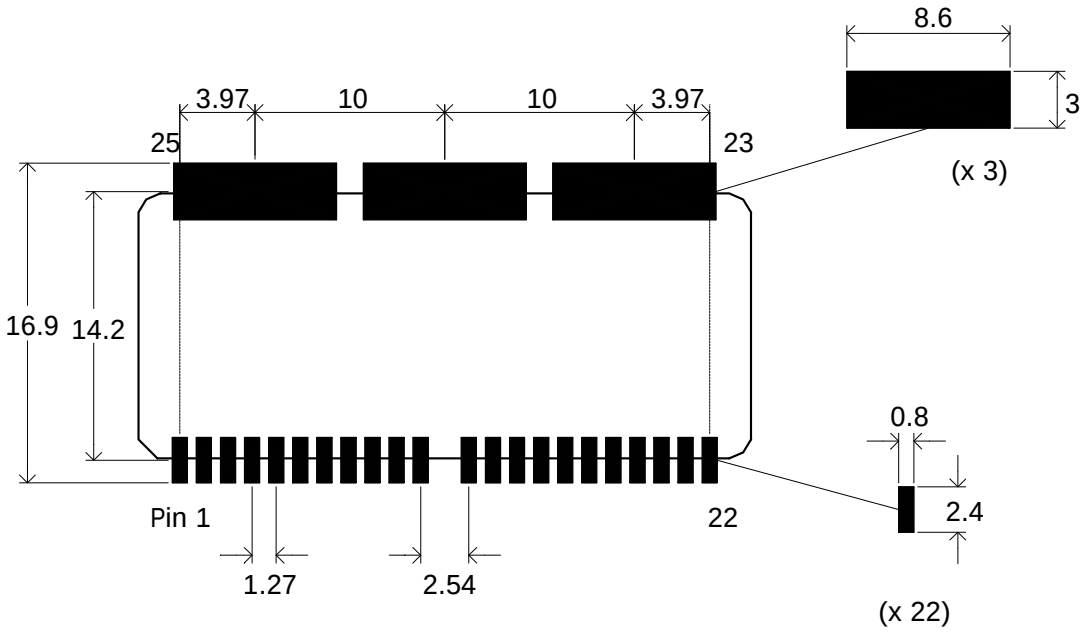



**Figure 30. Recommended PCB Pad Sizes**

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