



STV7699

PLASMA DISPLAY PANEL DATA DRIVER

FEATURES

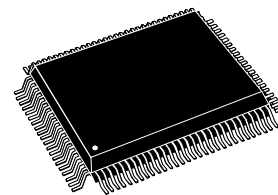
- 64 Outputs Plasma Display Driver
- 130V Absolute Maximum Supply
- 5V Supply for Logic
- 50/40mA Source / Sink Output
- 60/60mA Source / Sink Output Diode
- 64-BIT Shift Register (25MHz)
- BLK, Polarity and HIZ Control
- BCD Technology
- Die or 100-PIN PQFP Package

DESCRIPTION

The STV7699 is a Plasma Display Panel (PDP) data driver implemented in ST's proprietary BCD technology. Using a 4-bit wide cascaded shift register, it drives 64 high current & high voltage outputs. By serially connecting several STV7699, any horizontal pixel definition can be performed. The 25MHz shift clock gives an equivalent 100MHz shift register. The STV7699 is supplied

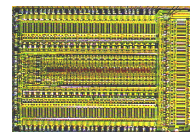
with a separated 130V power output supply and a 5V logic supply.

All command inputs are CMOS compatible. The STV7699 package is a 100-pin PQFP. It is also available as die.



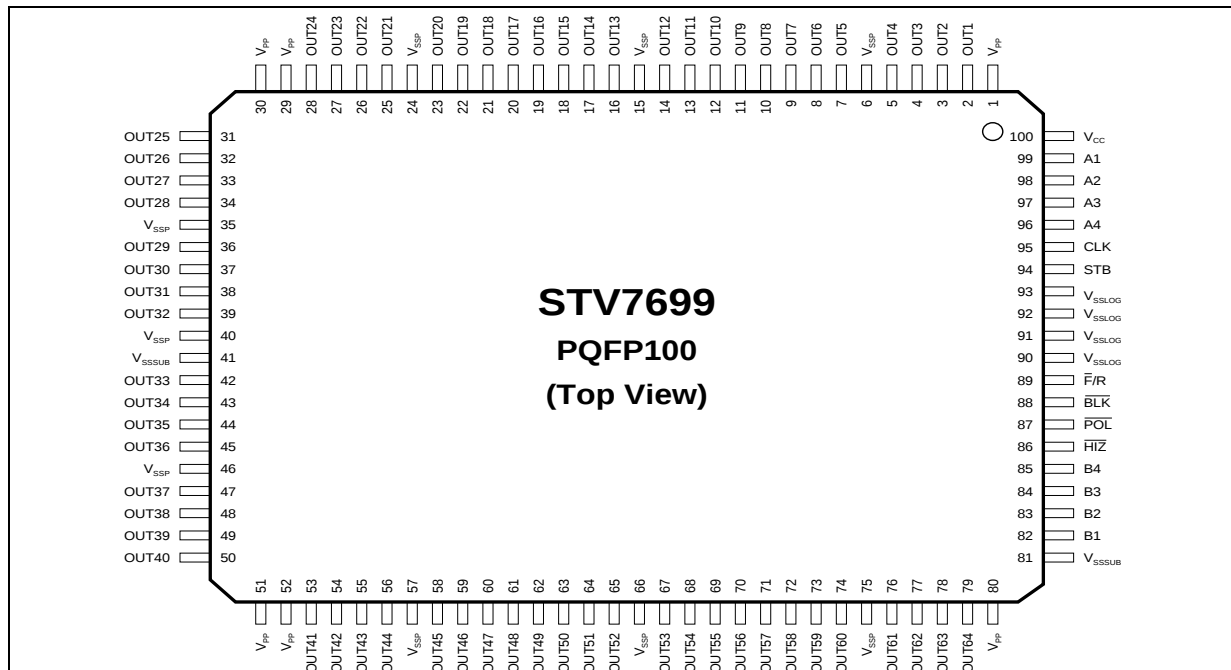
PQFP100 (14 x 20 x 2.80 mm)

(Full Plastic Quad Flat Pack)



CODE ORDER: unsawn tested wafer (1)

PIN CONNECTIONS



Version 4.1

1 PIN ASSIGNMENT (PQFP100)

Pin Number	Symbol	Type	Function
100	V _{CC}	Supply	5V Logic Supply
1-29-30-51-52-80	V _{PP}	Supply	High Voltage Supply of power outputs
6-15-24-35-40-46-57-66-75	V _{SSP}	Ground	Ground of power outputs
90-93	V _{SSLOG}	Ground	Logic Ground
41-81	V _{SSSUB}	Ground	Substrate Ground
2 to 5 - 7 to 14 - 16 to 23 25 to 28 - 31 to 34 - 36 to 39 42 to 45 - 47 to 50 - 53 to 56 58 to 65 - 67 to 74 - 76 to 79	OUT1 to OUT 64	Output	Power Outputs
95	CLK	Input	Clock of data shift register Low to High transition makes the data enter into the shift register and available at the output stage and at the output of the shift register.
94	STB	Input	Latch of data to outputs. When the STB signal is set to low level data are transferred into the latch stage. When STB is set at high level data are held in the latch stage.
88	BLK	Input	Power Output Blanking Control
87	POL	Input	Power Output Polarity Control
86	HIZ	Input	Power Output High Impedance Control
89	$\overline{F/R}$	Input	Selection of shift direction
96 to 99	A4 to A1	Input	Shift register data input and output according to $\overline{F/R}$ value. When set to low, Ai = input and Bi = output
82 to 85	B1 to B4	Output	

2 PIN ASSIGNMENT (power outputs)

Output No.	Pin No.	Output No.	Pin No.	Output No.	Pin No.	Output No.	Pin No.
1	2	17	20	33	42	49	62
2	3	18	21	34	43	50	63
3	4	19	22	35	44	51	64
4	5	20	23	36	45	52	65
5	7	21	25	37	47	53	67
6	8	22	26	38	48	54	68
7	9	23	27	39	48	55	69
8	10	24	28	40	50	56	70
9	11	25	31	41	53	57	71
10	12	26	32	42	54	58	72
11	13	27	33	43	55	59	73
12	14	28	34	44	56	60	74
13	16	29	36	45	58	61	76
14	17	30	37	46	59	62	77
15	18	31	38	47	60	63	78
16	19	32	39	48	61	64	79

3 PAD DIMENSIONS (in μm)

The reference is the centre of the die ($x=0$, $y=0$).

LEFT SIDE from top to bottom

Name	Centre: X	Centre: Y	Size: x	Size: y
V _{PP}	-1738.0	2867.5	90.0	75.0
OUT1	-1738.0	2703.0	90.0	75.0
OUT2	-1738.0	2570.5	90.0	75.0
OUT3	-1738.0	2411.0	90.0	75.0
OUT4	-1738.0	2228.5	90.0	75.0
V _{SSP}	-1738.0	2093.0	90.0	75.0
OUT5	-1738.0	1952.0	90.0	75.0
OUT6	-1738.0	1813.5	90.0	75.0
OUT7	-1738.0	1631.0	90.0	75.0
OUT8	-1738.0	1453.0	90.0	75.0
OUT9	-1738.0	1235.5	90.0	75.0
OUT10	-1738.0	1046.5	90.0	75.0
OUT11	-1738.0	862.0	90.0	75.0
OUT12	-1738.0	712.5	90.0	75.0
V _{SSP}	-1738.0	566.0	90.0	75.0
OUT13	-1738.0	431.0	90.0	75.0
OUT14	-1738.0	293.0	90.0	75.0
OUT15	-1738.0	82.5	90.0	75.0
OUT16	-1738.0	-109.5	90.0	75.0
OUT17	-1738.0	-277.0	90.0	75.0
OUT18	-1738.0	-471.0	90.0	75.0
OUT19	-1738.0	-691.5	90.0	75.0
OUT20	-1738.0	-822.5	90.0	75.0
V _{SSP}	-1738.0	-953.0	90.0	75.0
OUT21	-1738.0	-1096.0	90.0	75.0
OUT22	-1738.0	-1335.5	90.0	75.0
OUT23	-1738.0	-1569.0	90.0	75.0
OUT24	-1738.0	-1697.5	90.0	75.0
V _{PP}	-1715.0	-2045.0	90.0	200.0

BOTTOM SIDE from left to right

Name	Centre: X	Centre: Y	Size: x	Size: y
OUT25	-1443.5	-3077.0	75.0	90.0
OUT26	-1249.0	-3077.0	75.0	90.0
OUT27	-1049.5	-3077.0	75.0	90.0
OUT28	-889.0	-3077.0	5.0	90.0
V _{SSP}	-753.0	-3077.0	75.0	90.0
OUT29	-614.0	-3077.0	75.0	90.0
OUT30	-467.5	-3077.0	75.0	90.0
OUT31	-332.0	-3077.0	75.0	90.0
OUT32	-186.5	-3077.0	75.0	90.0
V _{SSP}	-54.0	-3077.0	75.0	90.0
V _{SSSUB}	78.0	-3077.0	75.0	90.0
OUT33	209.5	-3077.0	75.0	90.0
OUT34	342.5	-3077.0	75.0	90.0
OUT35	467.5	-3077.0	75.0	90.0
OUT36	607.5	-3077.0	75.0	90.0
V _{SSP}	752.0	-3077.0	75.0	90.0
OUT37	892.5	-3077.0	75.0	90.0
OUT38	1045.5	-3077.0	75.0	90.0
OUT39	1252.0	-3077.0	75.0	90.0
OUT40	1433.5	-3077.0	75.0	90.0

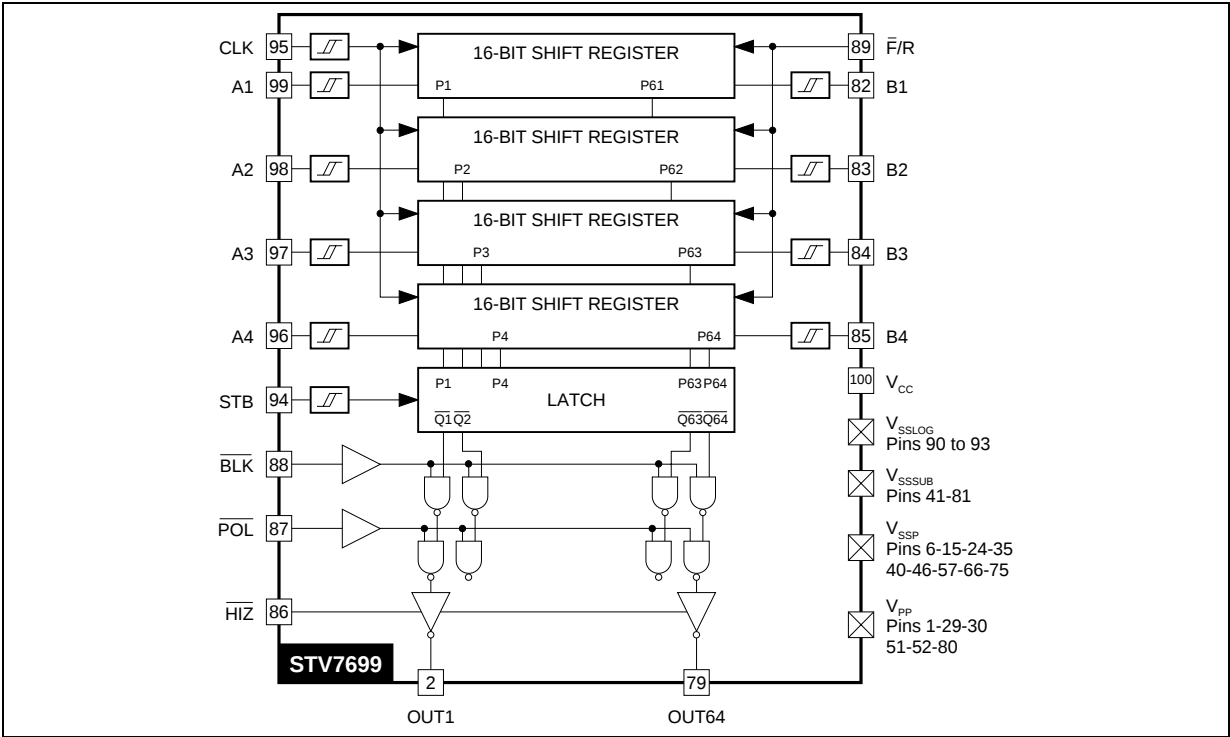
RIGHT SIDE from bottom to top

Name	Centre: X	Centre: Y	Size: x	Size: y
V _{PP}	1737.5	-1646.0	90.0	75.0
OUT41	1737.5	-1507.0	90.0	75.0
OUT42	1737.5	-1328.0	90.0	75.0
OUT43	1737.5	-1096.0	90.0	75.0
OUT44	1737.5	-953.0	90.0	75.0
V _{SSP}	1737.5	-822.5	90.0	75.0
OUT45	1737.5	-691.5	90.0	75.0
OUT46	1737.5	-471.0	90.0	75.0
OUT47	1737.5	-277.0	90.0	75.0
OUT48	1737.5	-109.5	90.0	75.0
OUT49	1737.5	82.5	90.0	75.0
OUT50	1737.5	293.0	90.0	75.0
OUT51	1737.5	431.0	90.0	75.0
OUT52	1737.5	566.0	90.0	75.0
V _{SSP}	1737.5	712.5	90.0	75.0
OUT53	1737.5	862.0	90.0	75.0
OUT54	1737.5	1046.5	90.0	75.0
OUT55	1737.5	1235.5	90.0	75.0
OUT56	1737.5	1453.0	90.0	75.0
OUT57	1737.5	1631.0	90.0	75.0
OUT58	1737.5	1813.5	90.0	75.0
OUT59	1737.5	1952.0	90.0	75.0
OUT60	1737.5	2093.0	90.0	75.0
V _{SSP}	1737.5	2228.5	90.0	75.0
OUT61	1737.5	2411.0	90.0	75.0
OUT62	1737.5	2570.5	90.0	75.0
OUT63	1737.5	2703.0	90.0	75.0
OUT64	1737.5	2873.5	90.0	75.0
V _{PP}	1737.5	-1646.0	90.0	200.0

TOP SIDE from right to left

Name	Centre: X	Centre: Y	Size: x	Size: y
V _{SSSUB}	1628.5	3073.5	75.0	90.0
B1	1478.5	3073.5	75.0	90.0
B2	1228.5	3077.0	75.0	90.0
B3	978.5	3077.0	75.0	90.0
B4	847.5	3077.0	75.0	90.0
HIZ	716.5	3077.0	75.0	90.0
POL	486.5	3077.0	75.0	90.0
BLK	355.5	3077.0	75.0	90.0
F/R	224.5	3077.0	75.0	90.0
V _{SSLOG}	31.0	3077.0	200.0	90.0
V _{SSLOG}	-354.5	3077.0	200.0	90.0
STB	-582.0	3077.0	75.0	90.0
CLK	-713.0	3077.0	75.0	90.0
A4	-844.0	3077.0	75.0	90.0
A3	-975.0	3077.0	75.0	90.0
A2	-1106.0	3077.0	75.0	90.0
A1	-1471.5	3077.0	75.0	90.0
V _{CC}	-1629.0	3077.0	75.0	90.0

4 BLOCK DIAGRAM



5 CIRCUIT DESCRIPTION

The STV7699 contains all the logic and the power circuits necessary to drive the columns of a Plasma Display Panel (P.D.P.). Data are shifted at each low to high transition of the (CLK) shift clock. Data are input in a 4-bit wide data bus to A1 - A4 input (case of forward shift mode; $\overline{F/R}$ = low). After 16 shifts, the first nibble is available at the serial outputs B1- B4. These outputs can be used to cascade several drivers to performed any horizontal resolution. CLK, Ai and Bi inputs are Smith trigger inputs to improve the noise margin.

The Forward/Reverse ($\overline{F/R}$) input is used to select the direction of the shift register.

The maximum frequency of the shift clock is 25MHz.

All the output data are held and memorized into the latch stage when the Latch input (STB) is high. When it is at low level, data are transferred from the shift register to the latch and to the output power stage.

Output state can be forced to high impedance by pulling low $\overline{HIZ}$ input.

When BLK is Low, all the outputs are forced to low level or high level according to $\overline{POL}$ signal value.

Output state copy data that was input, with the same polarity, when BLK, $\overline{HIZ}$ and $\overline{POL}$ are High.

V_{SSLOG} , V_{SSSUB} and V_{SSP} are not internally connected.

V_{SSLOG} and V_{SSSUB} must be connected as close as possible to the logical reference ground of the application.

Table 1 : Power Output Truth Table

Data	STB	$\overline{POL}$	$\overline{BLK}$	$\overline{HIZ}$	Driver Output	Comments
x	x	x	x	L	HIZ	High impedance
x	x	L	x	H	L	Forced to low
x	x	H	L	H	H	Forced to high
x	H	H	H	H	$Q_n^{(1)}$	Latched data
L	L	H	H	H	L	Copy data
H	L	H	H	H	H	Copy data

Note 1: Q_n is the value memorised in the latch stage; it is the value of the parallel shift register output stage after n Clock pulses

Data loaded in the shift register is read on the output power stage without inversion of its polarity.

Table 2 : Control Table

$\overline{F/R}$	Ai	Bi	Comments
L	Input	Output	Forward shift
H	Output	Input	Reverse shift

6 ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Logic Supply	-0.3, +7	V
V_{IN}	Logic Input Voltage	-0.3, $V_{CC} + 0.3$	V
V_{OUT}	Logic Output Voltage	-0.3, $V_{CC} + 0.3$	V
V_{PP}	Driver Power Supply	-0.3, +150	V
V_{POUT}	Driver Output Voltage	-0.3, +150	V
I_{POUT}	Driver Output Current ⁽²⁾	60	mA
I_{DOUT}	Diode Output Current ⁽²⁾	+40/-50	mA
T_{jmax}	Junction Temperature	+150	°C
T_{oper}	Operating Temperature	-20, +85	°C
T_{stg}	Storage Temperature	-50, +150	°C

7 THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Junction-ambient Thermal Resistance ⁽²⁾ Max.	50	°C/W
P_{oper}	Operating Power Dissipation ($T_{amb} = 25^{\circ}C$) Max.	2	W
T_{joper}	Operating Junction Temperature ⁽³⁾ Max.	+125	°C

Note 2: For PQFP100 packaging.

Note 3: Through all power outputs : with power dissipation lower or equal than P_{tot} and junction temperature lower than or equal to T_{jmax}

8 ELECTRICAL CHARACTERISTICS

($V_{CC} = 5V$, $V_{PP} = 130V$, $V_{SSP} = 0V$, $V_{SSLOG} = 0V$, $V_{SSSUB} = 0V$, $T_{amb} = 25^{\circ}C$, $f_{CLK} = 25MHz$, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
SUPPLY						
V_{CC}	Logic Supply Voltage		4.5	5	5.5	V
I_{CCH}	Logic Supply Current		-	-	100	μA
I_{CCL}	Logic Supply Current	$f_{CLK} = 20MHz$	-	12	TBD	mA
V_{PP}	Power Output Supply Voltage		-	-	130	V
I_{PPH}	Power Output Supply Current (steady outputs)		-	-	100	μA
OUTPUT						
OUT1-OUT64						
V_{POUTH}	Power Output High Level	$I_{POUTH} = -10mA$, $V_{PP} = 65V$ $I_{POUTH} = -40mA$, $V_{PP} = 65V$	55 TBD	60 -	- -	V V
V_{POUTL}	Power Output Low Level	$I_{POUTL} = +10mA$ $I_{POUTL} = +30mA$	- -	2 12	5 TBD	V V
V_{DOUTH}	Output Diode High Level	$I_{DOUTH} = +25mA^{(4)(5)}$	-	-	3	V
V_{DOUTL}	Output Diode Low Level	$I_{DOUTL} = -25mA^{(4)(5)}$	-	-	-3	V
I_{OUTHIZ}	Output Stage Leakage Current on HIZ State		-	-	± 10	μA
SHIFT REGISTER OUTPUT (Ai or Bi according to $\bar{F}/R$ Status)						
V_{OH}	Logic Output High Level,	$I_{OH} = -0.5mA$	4	-	-	V
V_{OL}	Logic Output Low Level,	$I_{OL} = +0.5mA$	-	0.1	0.3	V
INPUT (CLK, STB, $\bar{BLK}$, $\bar{HIZ}$, Ai, Bi)						
V_{IH}	Input High Level		$0.8 V_{CC}$	-	-	V
V_{IL}	Input Low Level		-	-	$0.2 V_{CC}$	V
I_{IH}	High Level Input Current	$V_{IH} = V_{CC}$	-	-	1	μA
I_{IL}	Low Level Input Current	$V_{IL} = 0V$	-	-	-1	μA

Note 4: Compatible with power dissipation and $T_{joper} \leq 125^{\circ}$

Note 5: See test diagram

9 AC TIMINGS REQUIREMENTS

($V_{CC} = 4.5V$ to $5.5V$, $T_{amb} = -20$ to $+85^{\circ}C$, input signals max leading edge & trailing edge (t_R , t_F) = 10ns)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{CLK}	Data Clock Period	40	-	-	ns
t_{WHCLK}	Duration of clock (CLK) pulse at high level	15	-	-	ns
t_{WLCLK}	Duration of clock (CLK) pulse at low level	15	-	-	ns
t_{SDAT}	Set-up Time of data input before clock (low to high) transition	0	-	-	ns
t_{HDAT}	Hold Time of data input after clock (low to high) transition	15	-	-	ns
t_{DSTB}	Minimum Delay to latch (STB) after clock (low to high) transition	20	-	-	ns
t_{STB}	Latch (STB) Low Level Pulse Duration	10	-	-	ns
t_{BLK}	Blanking ($\overline{BLK}$) Pulse Duration	100	-	-	ns
t_{POL}	Polarity ($\overline{POL}$) Pulse Duration	100	-	-	ns
t_{HIZ}	High Impedance ($\overline{HIZ}$) Pulse Duration	100	-	-	ns
t_{SFR}	Set-up Time of Forward/Reverse Signal before Clock (low to high) transition	100	-	-	ns

10 AC TIMINGS CHARACTERISTICS

($V_{CC} = 5V$, $V_{PP} = 65V$, $V_{SSP} = 0V$, $V_{SSLOG} = 0V$, $V_{SSSUB} = 0V$, $T_{amb} = 25^{\circ}C$, $V_{ILMax.} = 0.2V_{CC}$, $V_{IHMin.} = 0.8V_{CC}$, $V_{OH} = 4.0V$, $V_{OL} = 0.4V$, $C_L = 10pF$, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{CLK}	Data Clock Period	50	-	-	ns
t_{RDAT}	Logical Data Output Rise Time	-	TBD	30	ns
t_{FDAT}	Logical Data Output Fall Time	-	TBD	30	ns
t_{PHL1}	Delay of logic data output (high to low transition) after clock (CLK) transition	-	40	TBD	ns
t_{PLH1}	Delay of logic data output (low to high transition) after clock (CLK) transition	-	40	TBD	ns
t_{PHL2}	Delay of power output change (high to low transition) after clock (CLK) transition	-	TBD	120	ns
t_{PLH2}	Delay of power output change (low to high transition) after clock (CLK) transition	-	TBD	120	ns
t_{PHL3}	Delay of power output change (high to low transition) after Latch (STB) transition	-	TBD	110	ns
t_{PLH3}	Delay of power output change (low to high transition) after Latch (STB) transition	-	TBD	110	ns
t_{PHL4}	Delay of power output change (high to low transition) to Blank (BLK) or Polarity (POL) transition	-	TBD	110	ns
t_{PLH4}	Delay of power output change (low to high transition) to Blank (BLK) or Polarity (POL) transition	-	TBD	110	ns
t_{PHZ5}	Delay of power output change (high to Hi-Z transition) after high impedance (HIZ) ⁽⁶⁾	-	TBD	110	ns
t_{PLZ5}	Delay of power output change (low to Hi-Z transition) after high impedance (HIZ) ⁽⁶⁾	-	TBD	110	ns
t_{PZH5}	Delay of power output change (Hi-Z to high transition) after high impedance (HIZ) ⁽⁶⁾	-	TBD	110	ns
t_{PZL5}	Delay of power output change (Hi-Z to low transition) after high impedance (HIZ) ⁽⁶⁾	-	TBD	110	ns
t_{ROUT}	Power Output Rise Time ⁽⁷⁾	-	-	150	ns
t_{FOUT}	Power Output Rise Time ⁽⁷⁾	-	-	150	ns

Note 6: See test diagram

Note 7: One output among 64, loading capacitor $C_{OUT} = 50pF$, other outputs at low level.

Figure 1. AC Characteristics Waveform

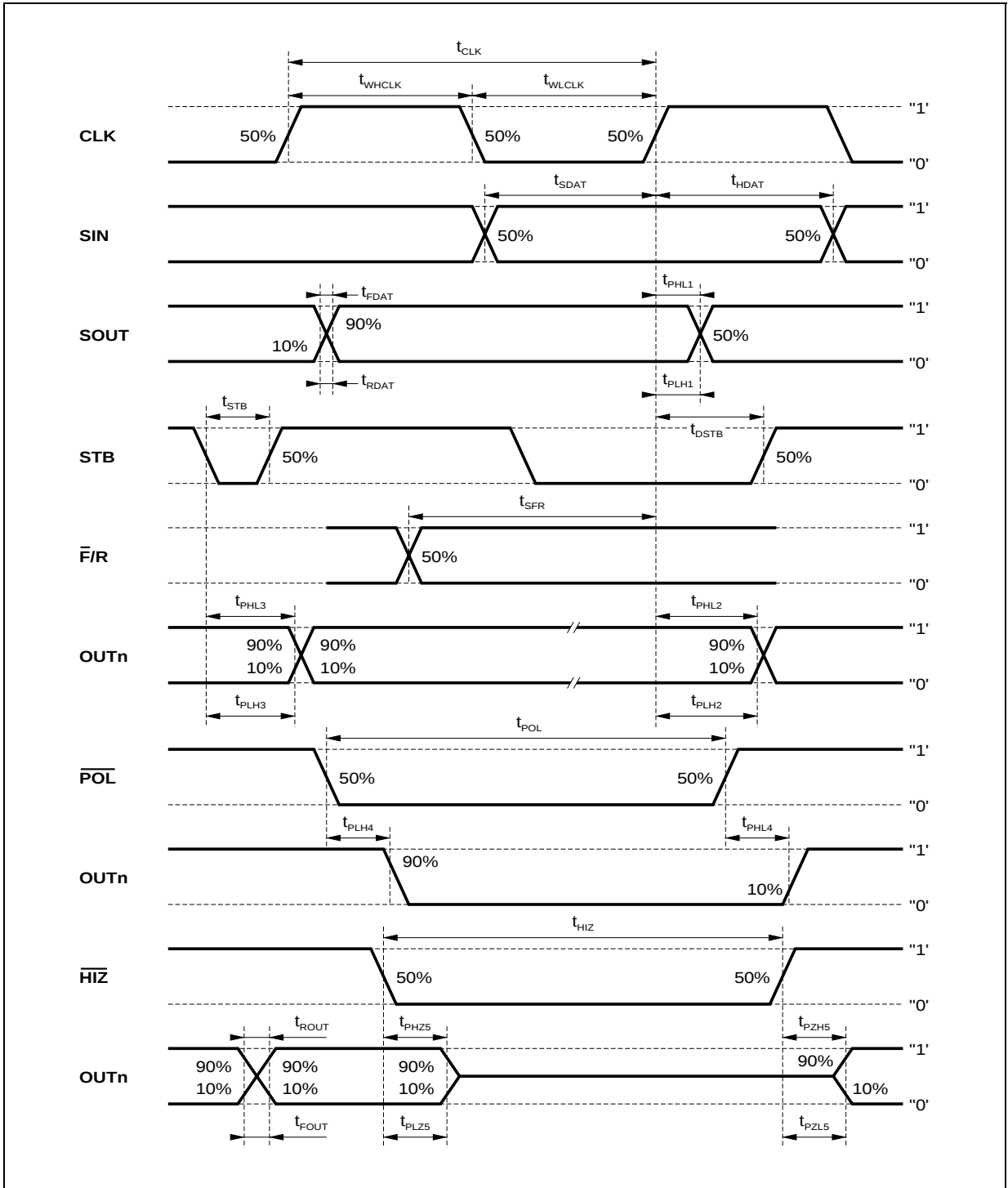


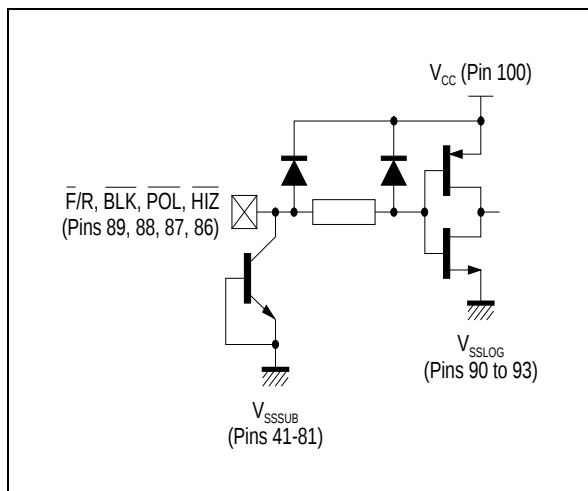
Figure 2. $\overline{F/R}$, $\overline{BLK}$, $\overline{POL}$, $\overline{HIZ}$ 

Figure 4. Ai, Bi

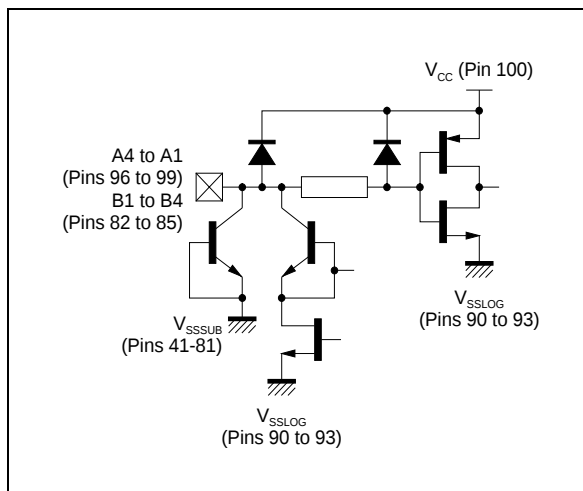


Figure 3. CLK, STB

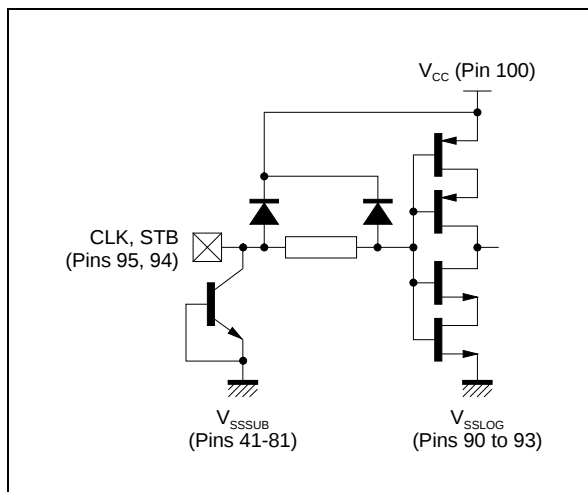
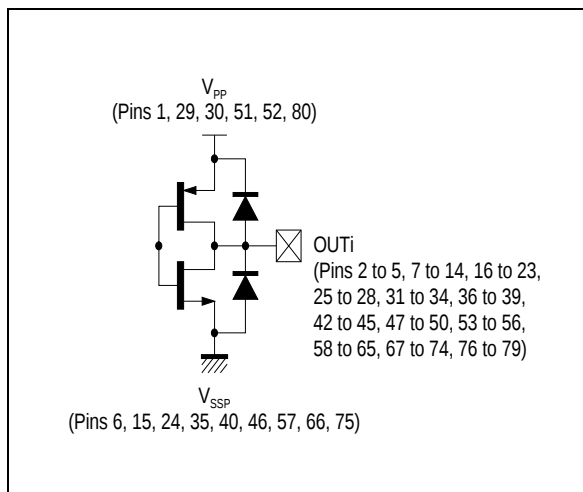
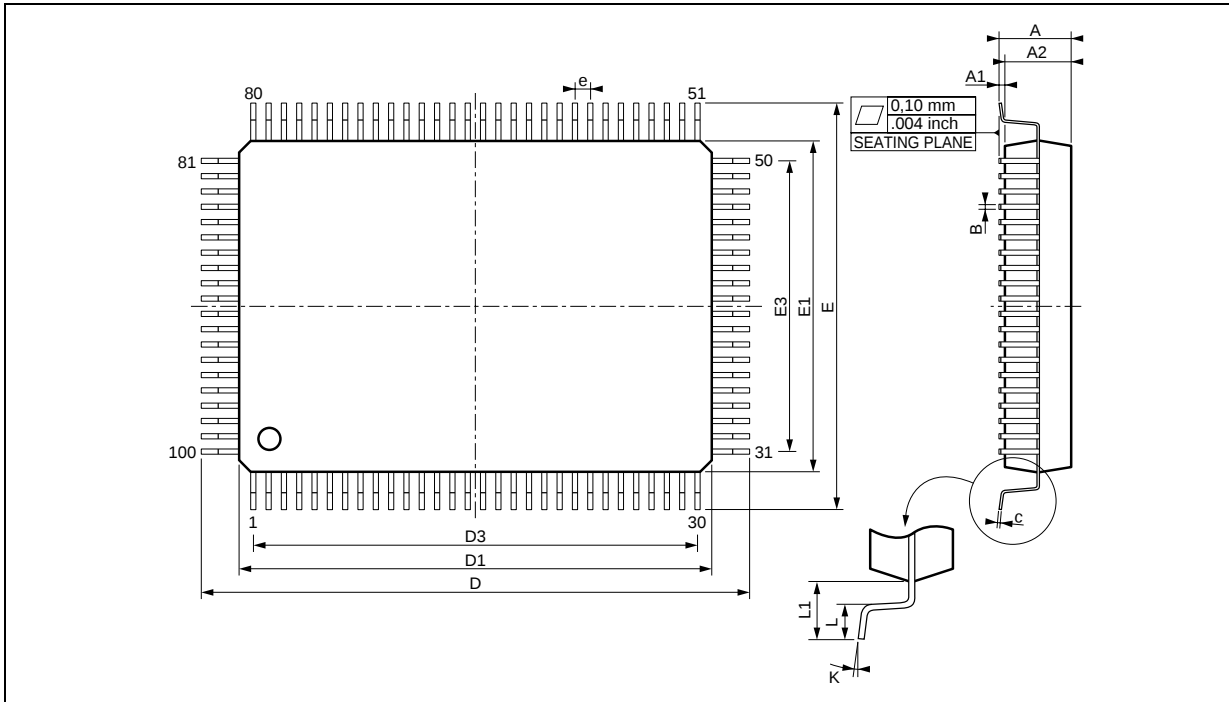


Figure 5. Power Output



11 PACKAGE MECHANICAL DATA

100 PIN-PLASTIC QUAD FLAT PACK (PQFP)



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			3.40			0.134
A1	0.25			0.010		
A2	2.55	2.80	3.05	0.100	0.110	0.120
B	0.22		0.38	0.0087		0.015
c	0.13		0.23	0.005		0.009
D	22.95	23.20	23.45	0.903	0.913	0.923
D1	19.90	20.00	20.10	0.783	0.787	0.791
D3		18.85			0.742	
e		0.65			0.026	
E	16.95	17.20	17.45	0.667	0.677	0.687
E1	13.90	14.00	14.10	0.547	0.551	0.555
E3		12.35			0.486	
L	0.65	0.80	0.95	0.026	0.031	0.037
L1		1.60			0.063	
K	0°(Min.), 7°(Max.)					

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