

**20V P-CHANNEL ENHANCEMENT MODE MOSFET**
**Product Summary**

$V_{(BR)DSS}$	Max $R_{DS(on)}$ (Note 6)	Max $I_D$ $T_A = 25^\circ C$
-20V	60m $\Omega$ @ $V_{GS} = -4.5V$	-4.23A
	90m $\Omega$ @ $V_{GS} = -2.5V$	-3.49A
	113m $\Omega$ @ $V_{GS} = -1.8V$	-3.11A

**Description**

This new generation MOSFET has been designed to minimize the on-state resistance ( $R_{DS(on)}$ ) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

**Applications**

- DC-DC Converters
- Motor Control
- Power management functions
- Analog Switch

**Features**

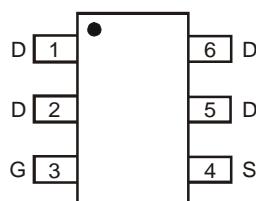
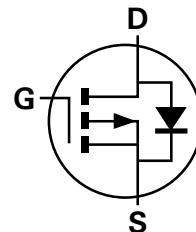
- Low Input Capacitance
- Low On-Resistance
- Fast Switching Speed
- Totally Lead-Free & Fully RoHS compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 Standards for High Reliability

**Mechanical Data**

- Case: TSOT26
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Finish – Matte Tin annealed over Copper leadframe. Solderable per MIL-STD-202, Method 208 (3)
- Weight: 0.0013 grams (approximate)



Top View


 Top View  
 Pin-Out


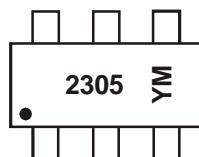
Equivalent Circuit

**Ordering Information** (Note 4)

Part Number	Marking	Reel size (inches)	Tape width (mm)	Quantity per reel
DMP2305UVT-7	2305	7	8	3,000
DMP2305UVT-13	2305	13	8	10,000

## Notes:

- No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- See <http://www.diodes.com> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- For packaging details, go to our website at <http://www.diodes.com>.

**Marking Information**


2305 = Product Type Marking Code

YM = Date Code Marking

Y = Year (ex: Y = 2011)

M = Month (ex: 9 = September)

## Date Code Key

Year	2011	2012	2013	2014	2015	2016	2017					
Code	Y	Z	A	B	C	D	E					
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

**Maximum Ratings** (@ $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Characteristic			Symbol	Value	Units
Drain-Source Voltage			$V_{DSS}$	-20	V
Gate-Source Voltage			$V_{GSS}$	$\pm 8$	V
Continuous Drain Current (Note 6) $V_{GS} = -4.5\text{V}$	Steady State	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	$I_D$	-4.23 -2.98	A
Continuous Drain Current (Note 6) $V_{GS} = -2.5\text{V}$	Steady State	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	$I_D$	-3.49 -2.79	A
Maximum Continuous Body Diode Forward Current (Note 6)			$I_S$	-4.23	A
Pulsed Drain Current (10 $\mu\text{s}$ pulse, duty cycle = 1%)			$I_{DM}$	-16	A

**Thermal Characteristics** (@ $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Characteristic		Symbol	Value	Units
Total Power Dissipation	(Note 5)	$P_D$	1.25	W
	(Note 6)		1.64	
Thermal Resistance, Junction to Ambient	(Note 5)	$R_{\theta JA}$	100	°C/W
	(Note 6)		76	
Thermal Resistance, Junction to Case	(Note 6)	$R_{\theta JC}$	14	
Operating and Storage Temperature Range		$T_J, T_{STG}$	-55 to 150	°C

Notes: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.

6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

**Thermal Characteristics** (@ $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

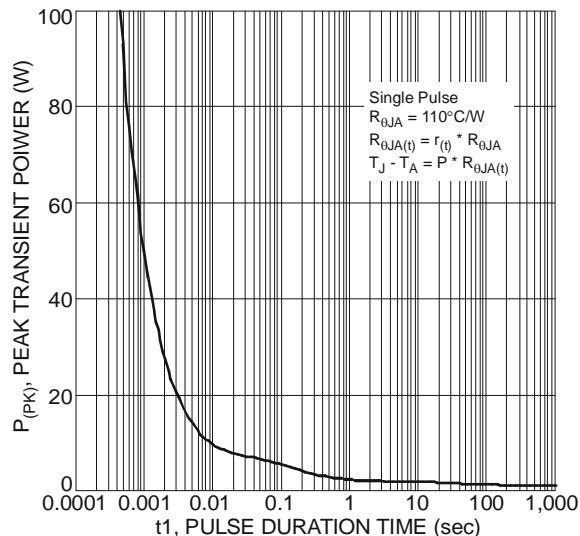


Figure 1 Single Pulse Maximum Power Dissipation

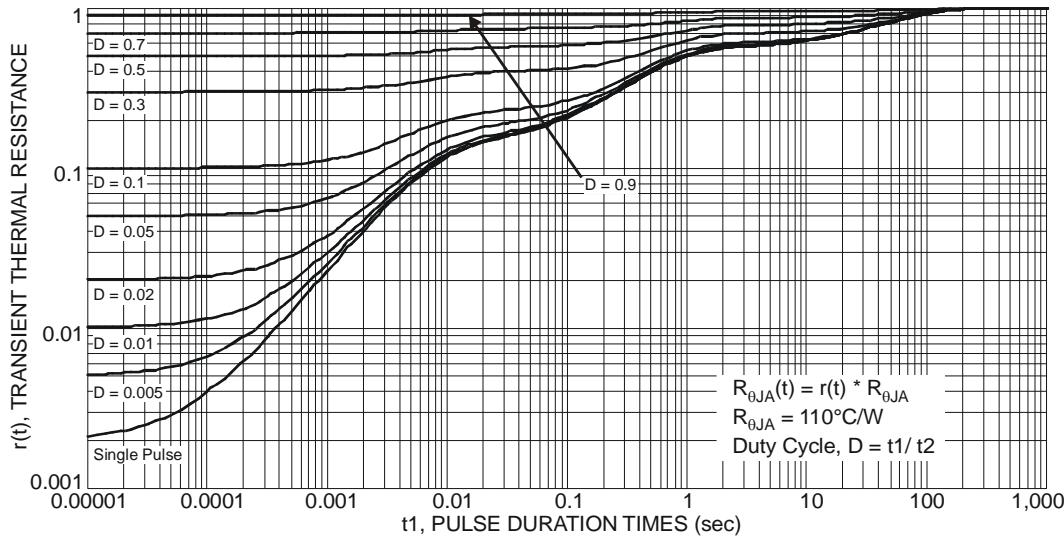


Figure 2 Transient Thermal Resistance

## Electrical Characteristics @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 7)</b>						
Drain-Source Breakdown Voltage	$\text{BV}_{\text{DSS}}$	-20	—	—	V	$V_{\text{GS}} = 0\text{V}$ , $I_D = -250\mu\text{A}$
Zero Gate Voltage Drain Current	$I_{\text{DSS}}$	—	—	-1	$\mu\text{A}$	$V_{\text{DS}} = -20\text{V}$ , $V_{\text{GS}} = 0\text{V}$
Gate-Source Leakage	$I_{\text{GSS}}$	—	—	$\pm 100$	nA	$V_{\text{GS}} = \pm 8\text{V}$ , $V_{\text{DS}} = 0\text{V}$
<b>ON CHARACTERISTICS (Note 7)</b>						
Gate Threshold Voltage	$V_{\text{GS(th)}}$	-0.5	—	-0.9	V	$V_{\text{DS}} = V_{\text{GS}}$ , $I_D = -250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{\text{DS (ON)}}$	—	45	60	$\text{m}\Omega$	$V_{\text{GS}} = -4.5\text{V}$ , $I_D = -4.2\text{A}$
		—	60	90		$V_{\text{GS}} = -2.5\text{V}$ , $I_D = -3.4\text{A}$
		—	87	113		$V_{\text{GS}} = -1.8\text{V}$ , $I_D = -2.0\text{A}$
Forward Transfer Admittance	$ Y_{\text{fs}} $	—	9	—	S	$V_{\text{DS}} = -5\text{V}$ , $I_D = -4\text{A}$
<b>DYNAMIC CHARACTERISTICS (Note 8)</b>						
Input Capacitance	$C_{\text{iss}}$	—	727	—	pF	$V_{\text{DS}} = -20\text{V}$ , $V_{\text{GS}} = 0\text{V}$ $f = 1.0\text{MHz}$
Output Capacitance	$C_{\text{oss}}$	—	69	—		
Reverse Transfer Capacitance	$C_{\text{rss}}$	—	64	—		
Gate Resistance	$R_G$	—	23	—	$\Omega$	$V_{\text{GS}} = 0\text{V}$ , $V_{\text{DS}} = 0\text{V}$ , $f = 1.0\text{MHz}$
Total Gate Charge	$Q_g$	—	7.6	—	nC	$V_{\text{GS}} = -4.5\text{V}$ , $V_{\text{DS}} = -4\text{V}$ , $I_D = -3.5\text{A}$
Gate-Source Charge	$Q_{\text{gs}}$	—	1.4	—		
Gate-Drain Charge	$Q_{\text{gd}}$	—	1.2	—		
Turn-On Delay Time	$t_{\text{D(on)}}$	—	14.0	—	ns	$V_{\text{DS}} = -4\text{V}$ , $V_{\text{GS}} = -4.5\text{V}$ , $R_L = 4\Omega$ , $R_G = 6\Omega$ , $I_D = -1\text{A}$
Turn-On Rise Time	$t_r$	—	13.0	—		
Turn-Off Delay Time	$t_{\text{D(off)}}$	—	53.8	—		
Turn-Off Fall Time	$t_f$	—	23.2	—		

Notes: 7. Short duration pulse test used to minimize self-heating effect.  
8. Guaranteed by design. Not subject to product testing.

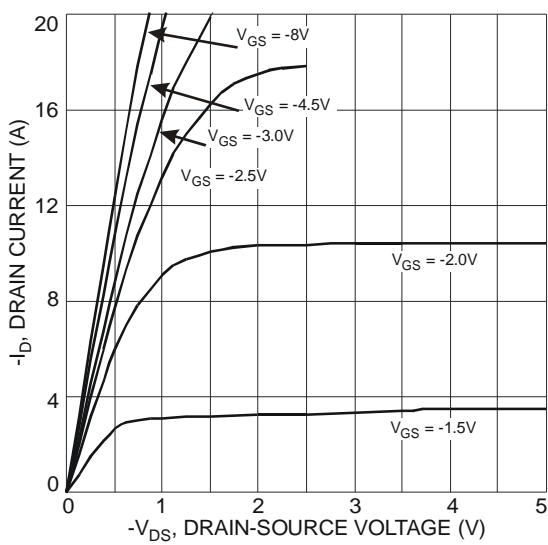


Figure 3 Typical Output Characteristic

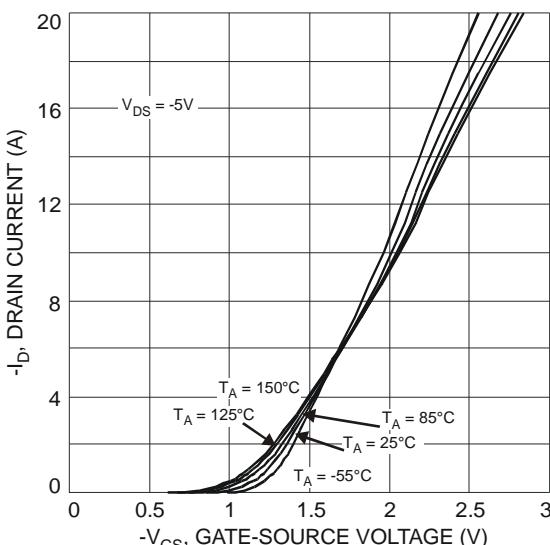


Figure 4 Typical Transfer Characteristic

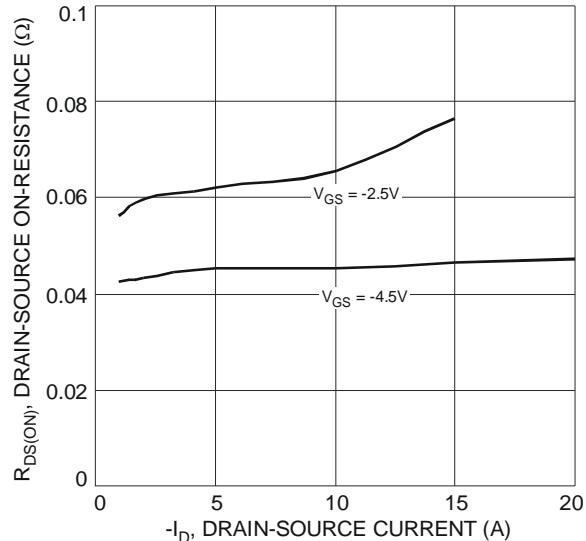


Figure 5 Typical On-Resistance  
vs. Drain Current and Gate Voltage

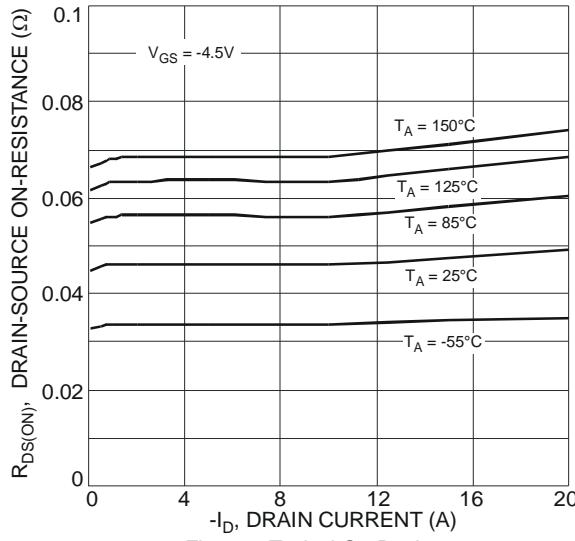


Figure 6 Typical On-Resistance  
vs. Drain Current and Temperature

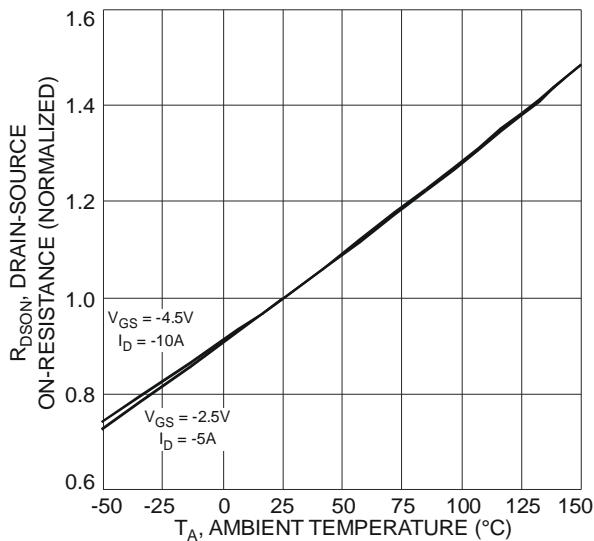


Figure 7 On-Resistance Variation with Temperature

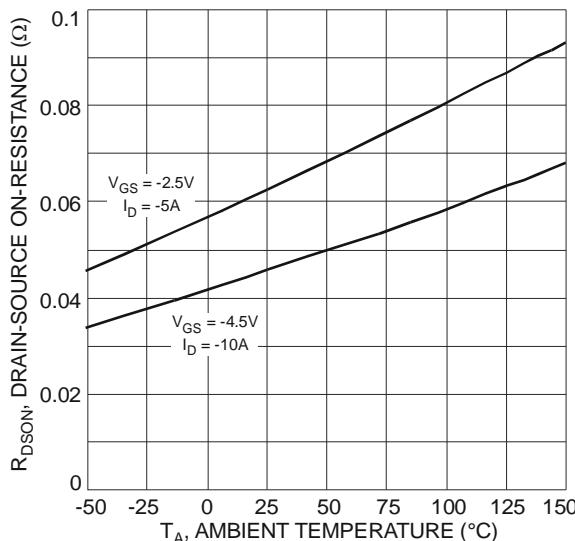


Figure 8 On-Resistance Variation with Temperature

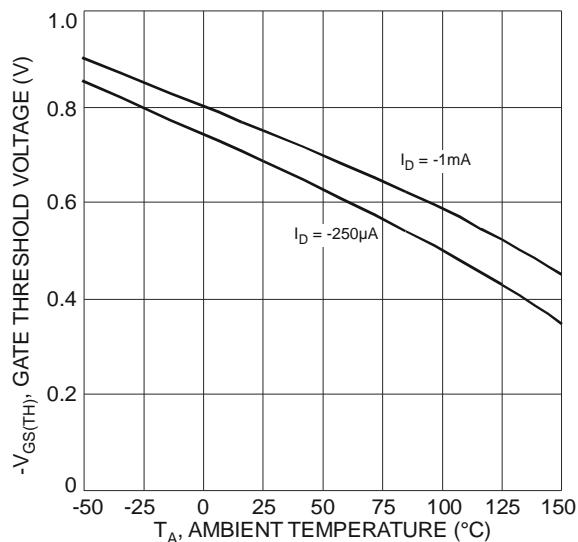


Figure 9 Gate Threshold Variation vs. Ambient Temperature

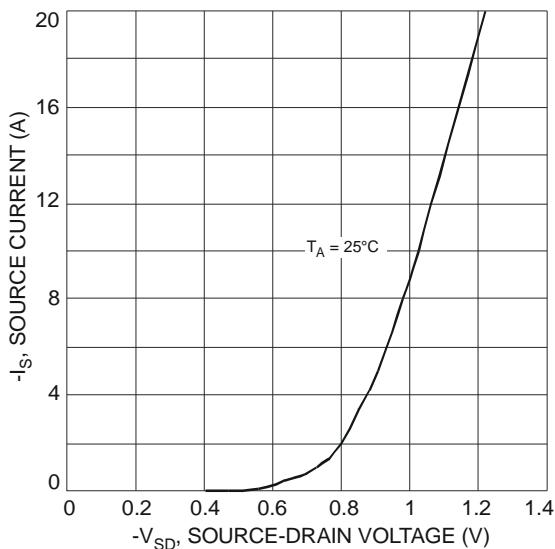


Figure 10 Diode Forward Voltage vs. Current

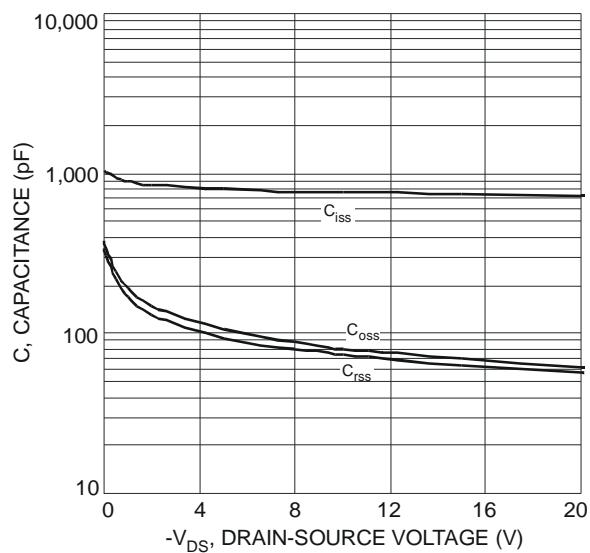


Figure 11 Typical Total Capacitance

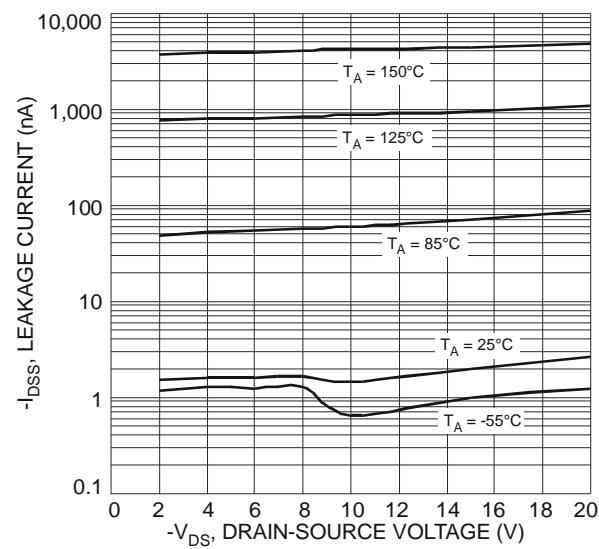
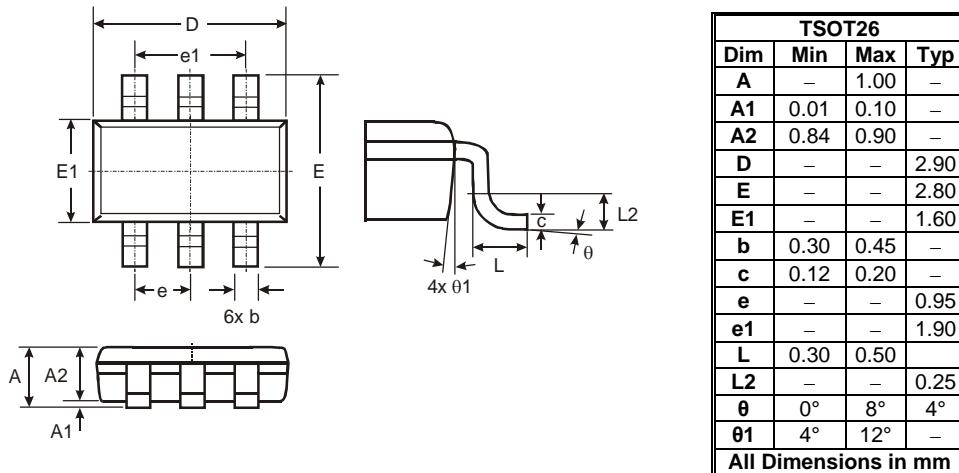


Figure 12 Typical Leakage Current vs. Drain-Source Voltage

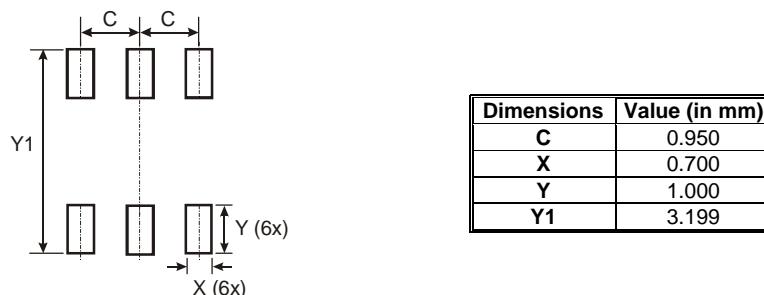
## Package Outline Dimensions

Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.



## Suggested Pad Layout

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



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