

MC10123

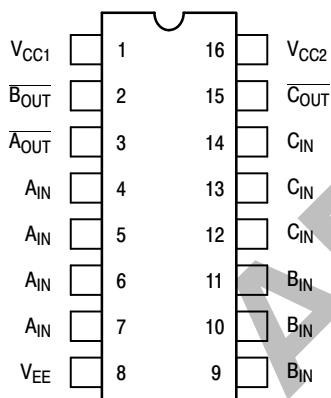
Triple 4-3-3-Input Bus Driver

The MC10123 consists of three NOR gates designed for bus driving applications on card or between cards. Output low logic levels are specified with $V_{OL} = -2.1$ Vdc so that the bus may be terminated to -2.0 Vdc. The gate output, when low, appears as a high impedance to the bus, because the output emitter-followers of the MC10123 are "turned-off." This eliminates discontinuities in the characteristic impedance of the bus.

The V_{OH} level is specified when driving a 25-ohm load terminated to -2.0 Vdc, the equivalent of a 50-ohm bus terminated at both ends. Although 25 ohms is the lowest characteristic impedance that can be driven by the MC10123, higher impedance values may be used with this part. A typical 50-ohm bus is shown in Figure 1.

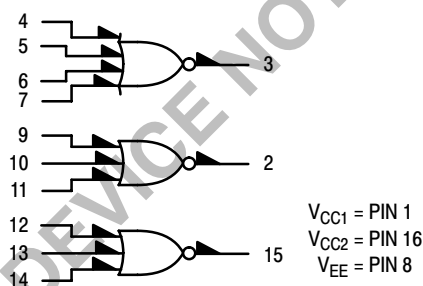
- $P_D = 310$ mW typ/pkg (No Load)
- $t_{pd} = 3.0$ ns typ
- $t_r, t_f = 2.5$ ns typ (20%–80%)

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18 of the ON Semiconductor MECL Data Book (DL122/D).

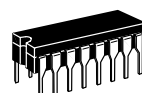
LOGIC DIAGRAM



ON Semiconductor

<http://onsemi.com>

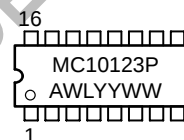
MARKING DIAGRAMS



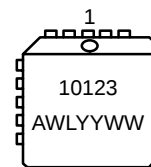
CDIP-16
L SUFFIX
CASE 620



PDIP-16
P SUFFIX
CASE 648



PLCC-20
FN SUFFIX
CASE 775

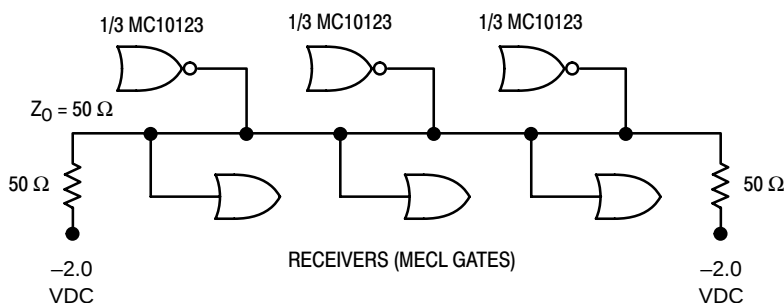


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10123L	CDIP-16	25 Units / Rail
MC10123P	PDIP-16	25 Units / Rail
MC10123FN	PLCC-20	46 Units / Rail

FIGURE 1 — 50-OHM BUS DRIVER (TYPICAL APPLICATION)



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			−30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I _E	8		82		71	75		82	mAdc
Input Current	I _{inH}	4		350			220		220	μAdc
	I _{inL}	4			0.5					μAdc
Output Voltage Logic 1	V _{OH}	3	−1.060	−0.890	−0.960		−0.810	−0.890	−0.700	Vdc
Output Voltage Logic 0	V _{OL}	3	−2.100	−2.030	−2.100		−2.030	−2.100	−2.030	Vdc
Threshold Voltage Logic 1	V _{OHA}	3	−1.080		−0.980			−0.910		Vdc
Threshold Voltage Logic 0	V _{OLA}	3		−2.100			−2.100		−2.100	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay	t _{4+3−}	3	1.2	4.6	1.2	3.0	4.4	1.2	4.8	
	t _{4−3+}	3	1.2	4.6	1.2	3.0	4.4	1.2	4.8	
Rise Time (20 to 80%)	t ₃₊	3	1.0	3.7	1.0	2.5	3.5	1.0	3.9	
Fall Time (20 to 80%)	t _{3−}	3	1.0	3.7	1.0	2.5	3.5	1.0	3.9	

ELECTRICAL CHARACTERISTICS (continued)

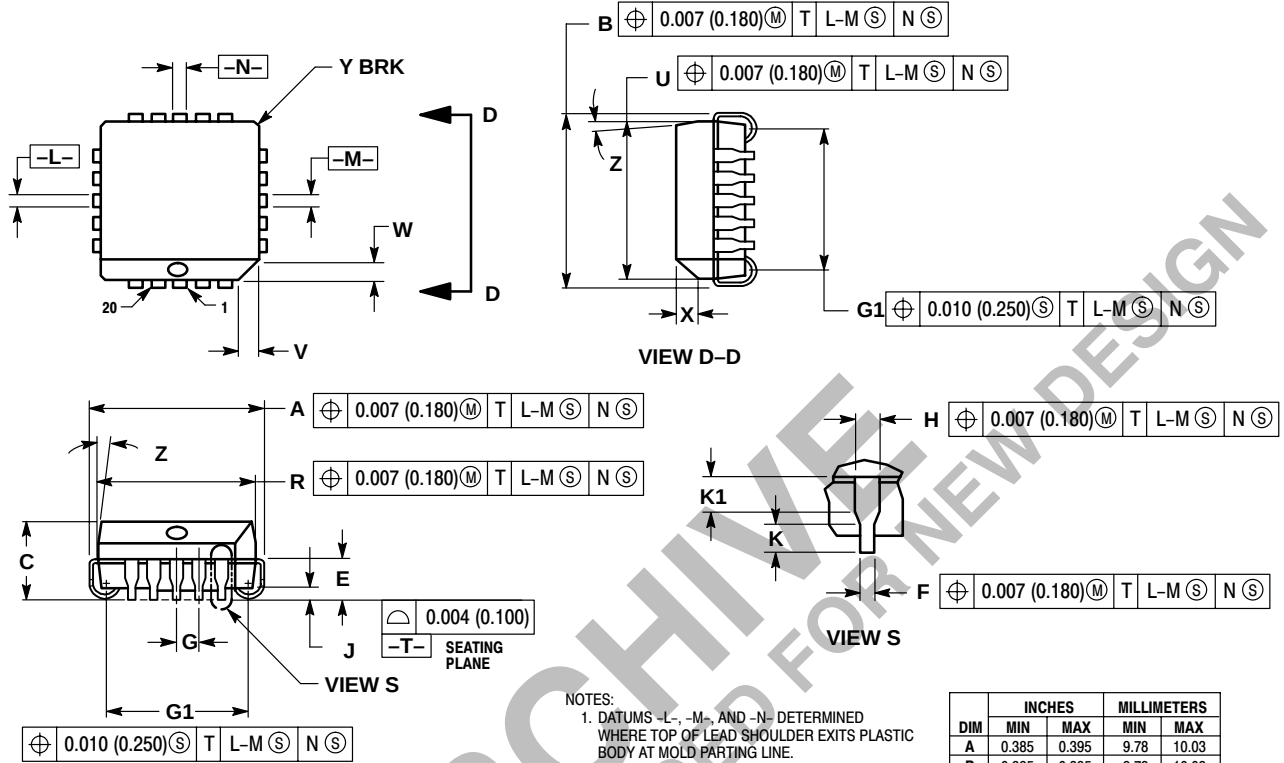
@ Test Temperature			TEST VOLTAGE VALUES (Volts)					(V _{CC}) Gnd
			V _{IHmax}	V _{ILmin}	V _{IHAmin}	V _{ILAmax}	V _{EE}	
			-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
			+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
			+85°C	-0.700	-1.825	-1.035	-1.440	-5.2
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V _{CC}) Gnd
			V _{IHmax}	V _{ILmin}	V _{IHAmin}	V _{ILAmax}	V _{EE}	
Power Supply Drain Current	I_E	8	4,5,6,7,9 10,11,12 13,14				8	1, 16
Input Current	I_{inH}	4	4				8	1, 16
	I_{inL}	4		4			8	1, 16
Output Voltage Logic 1	V_{OH}	3					8	1, 16
Output Voltage Logic 0	V_{OL}	3	4,5,6,7 9,12				8	1, 16
Threshold Voltage Logic 1	V_{OHA}	3				4,5,6,7	8	1, 16
Threshold Voltage Logic 0	V_{OLA}	3	9,12		4,5,6,7		8	1, 16
Switching Times (50 Ω Load)					Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+3-}	3			4	3	8	1, 16
	t_{4-3+}	3			4	3	8	1, 16
Rise Time (20 to 80%)	t_{3+}	3			4	3	8	1, 16
Fall Time (20 to 80%)	t_{3-}	3			4	3	8	1, 16

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

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PACKAGE DIMENSIONS

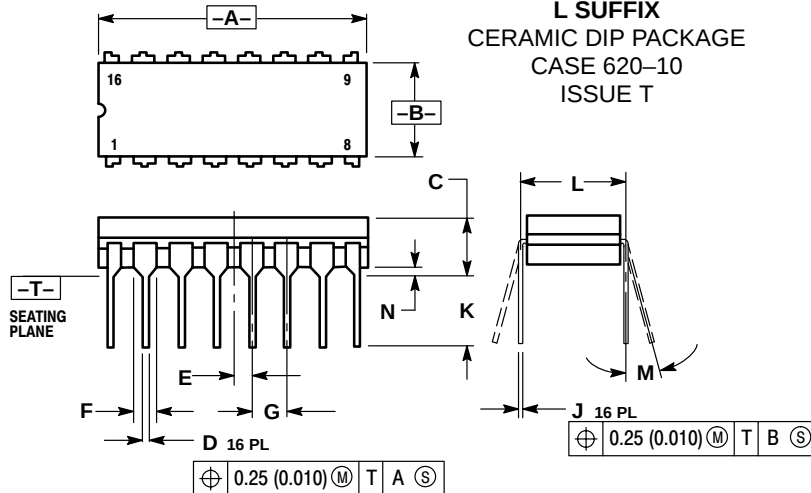
PLCC-20
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 775-02
ISSUE C



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2 °	10 °	2 °	10 °
G1	0.310	0.330	7.88	8.38
K1	0.040	---	1.02	---

MC10123

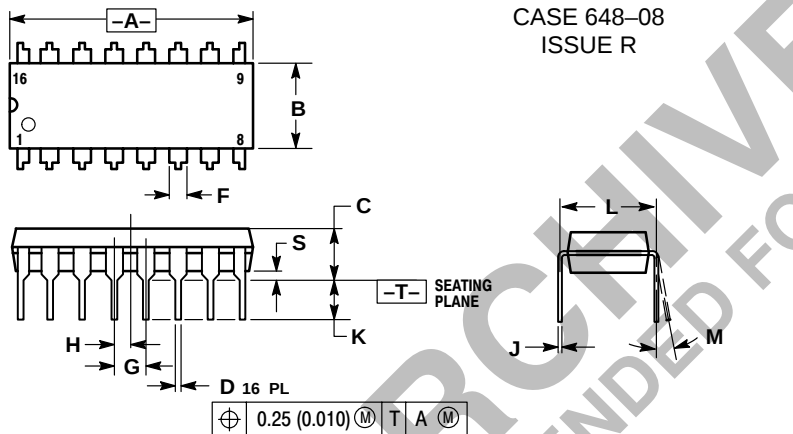
CDIP-16 L SUFFIX CERAMIC DIP PACKAGE CASE 620-10 ISSUE T



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	---	0.200	---	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

PDIP-16 P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
 5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

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