19-2307; Rev 1; 7/95

MAXIM

µP Compatible CMOS 14-Bit D/A Converter

General Description

The Maxim MX7538 is a high performance monolithic 14-bit multiplying digital-to-analog converter (DAC).

The MX7538 operates with a 14-bit data bus using standard chip select and memory write logic. A Load DAC ($\overline{LDAC}$) signal is provided where double buffering is required, such as in systems with multiple DACs. If the $\overline{LDAC}$ signal is kept low, the DAC register becomes transparent. The MX7538 is optimized for unipolar applications, but can be operated as a bipolar DAC with additional external components.

Full accuracy is maintained over the operating temperature range through the use of wafer-level laser-trimmed, thin-film resistors and temperature compensated NMOS switches. In addition, all digital inputs are compatible with both TTL, 74HC and 5V CMOS logic levels.

The MX7538 is available in the narrow (0.3") 24-lead DIP and Wide SO (0.3") packages.

Applications

Machine and Motion Control Systems

Automatic Test Equipment

Digital Audio Synthesis

µP Controlled Calibration Circuitry

Programmable Gain Amplifiers

Digitally Controlled Filters

Programmable Power Supplies

Features

- ◆ 14-Bit Monotonic Over Full Temperature Range
- ◆ 4-Quadrant Multiplication
- ◆ µP Compatible Double Buffered Inputs
- ◆ Low Power Consumption
- ◆ TTL, 74HC and 5V CMOS Compatible
- ◆ Low Output Leakage Over Temperature Range
- ◆ Small 24-Lead 0.3" DIP or Wide SO Packages

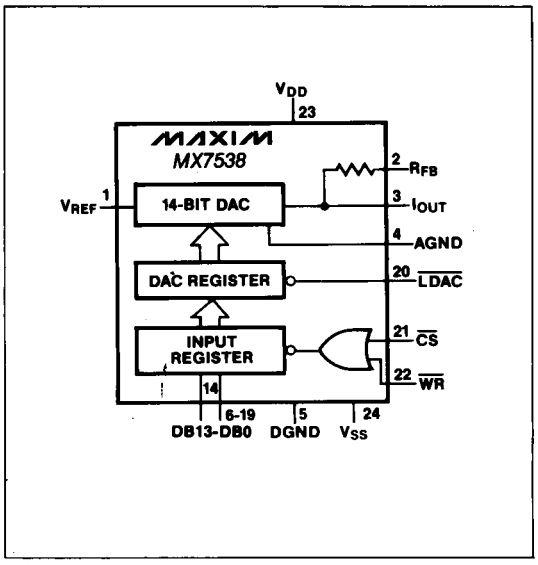
Ordering Information

PART	TEMP. RANGE	PACKAGE*	ERROR
MX7538JN	0°C to +70°C	Plastic DIP	±2 LSB
MX7538KN	0°C to +70°C	Plastic DIP	±1 LSB
MX7538JCWG	0°C to +70°C	Wide SO	±2 LSB
MX7538KCWG	0°C to +70°C	Wide SO	±1 LSB
MX7538JP	0°C to +70°C	PLCC	±2 LSB
MX7538KP	0°C to +70°C	PLCC	±1 LSB
MX7538J/D	0°C to +70°C	Dice	±2 LSB
MX7538JEWG	-40°C to +85°C	Wide SO	±2 LSB
MX7538KEWG	-40°C to +85°C	Wide SO	±1 LSB

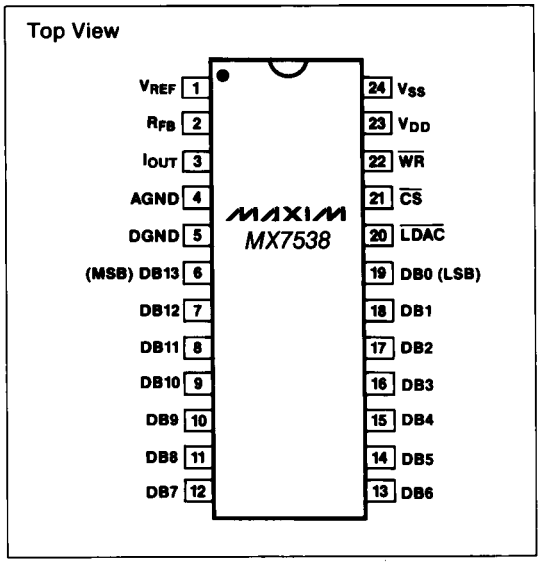
(Ordering Information continued on page 9.)

* *All devices — 24 lead packages*
PLCC — 28 lead package
***Maxim reserves the right to ship Ceramic SB in lieu of CERDIP packages.*

Functional Diagram



Pin Configuration



Call toll free 1-800-998-8800 for free samples or literature.

µP Compatible CMOS 14-Bit D/A Converter

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND ..... -0.3V, +17V
V_{SS} to AGND ..... -15V, +0.3V
V_{REF} to AGND ..... ±25V
V_{RFB} to AGND ..... ±25V
Digital Input Voltage to DGND ..... -0.3V, V_{DD}
V_{IOUT} to DGND ..... -0.3V, V_{DD}
AGND to DGND ..... -0.3V, V_{DD}
Power Dissipation (any Package)
To +75°C 1000mW
Derates above +75°C by ..... 10mW/°C

Operating Temperature Range
MX7538J/K ..... 0°C to +70°C
MX7538A/B ..... -25°C to +85°C
MX7538AE/BE ..... -40°C to +85°C
MX7538S/T ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +11.4V to +15.75V (Note 1), V_{REF} = +10V, V_{IOUT} = V_{AGND} = V_{SS} = 0V, T_A = T_{MIN} to T_{MAX} unless otherwise noted).

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ACCURACY							
Resolution				14			Bits
Relative Accuracy		MX7538K/B/T MX7538J/A/S				±1 ±2	LSB
Differential Nonlinearity		Guaranteed monotonic to 14 bits over temperature				±1	
Full Scale Error (Note 2)		All	T_A = +25°C			±4	LSB
		MX7538J/K MX7538A/B MX7538S MX7538T	T_A = T_{MIN} to T_{MAX} T_A = T_{MIN} to T_{MAX} T_A = T_{MIN} to T_{MAX} T_A = T_{MIN} to T_{MAX}			±8 ±5 ±10 ±6	
Gain Temperature Coefficient Δ Gain/Δ Temperature					±2		ppm/°C
I_{OUT} Output Leakage Current (Note 3)	I_{LKG}	All	T_A = +25°C			±5	nA
		V_{SS} = 0V				±25	nA
		MX7538J/K/A/B MX7538S/T	T_A = T_{MIN} to T_{MAX} T_A = T_{MIN} to T_{MAX}			±150	
REFERENCE INPUT							
V_{REF} Input Resistance	R_{REF}			3.5	6	10	kΩ
DIGITAL INPUTS							
Logic HIGH Threshold	V_{INH}			+2.4			V
Logic LOW Threshold	V_{INL}					+0.8	V
Input Leakage Current		Digital inputs = 0V or V_{DD}	T_A = +25°C T_A = T_{MIN} to T_{MAX}			±1 ±10	µA
Input Capacitance (Note 4)	C_{IN}					7	pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +11.4V to +15.75V (Note 1), V_{REF} = +10V, V_{IOUT} = V_{AGND} = V_{SS} = -300mV, T_A = T_{MIN} to T_{MAX} unless otherwise noted).

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER REQUIREMENTS							
Positive Supply Range	V_{DD}	Operating Range		+11.4		+15.75	V
		Functional with degraded specifications			+5.0		
Negative Supply Range	V_{SS}	Operating Range		-200		-500	mV
Power Supply Current	I_{DD}	Digital Inputs = V_{INH} or V_{INL}				4	mA
		Digital Inputs = 0V or V_{DD}				500	μA
TIMING CHARACTERISTICS (See Figure 1 for timing diagram.)							
$\overline{CS}$ to $\overline{WR}$ Setup Time	t_1			0			ns
$\overline{CS}$ to $\overline{WR}$ Hold Time	t_2			0			ns
$\overline{LDAC}$ Pulse Width	t_3	All	T_A = +25°C	170			ns
		MX7538J/K/A/B	T_A = T_{MIN} to T_{MAX}	200			
		MX7538S/T	T_A = T_{MIN} to T_{MAX}	240			
Write Pulse Width	t_4	All	T_A = +25°C	170			ns
		MX7538J/K/A/B	T_A = T_{MIN} to T_{MAX}	200			
		MX7538S/T	T_A = T_{MIN} to T_{MAX}	240			
Data Setup Time	t_5	All	T_A = +25°C	140			ns
		MX7538J/K/A/B	T_A = T_{MIN} to T_{MAX}	160			
		MX7538S/T	T_A = T_{MIN} to T_{MAX}	180			
Data Hold Time	t_6	All	T_A = +25°C	20			ns
		MX7538J/K/A/B	T_A = T_{MIN} to T_{MAX}	20			
		MX7538S/T	T_A = T_{MIN} to T_{MAX}	30			
DYNAMIC PERFORMANCE (Note 5)							
Output Current Settling Time		T_A = +25°C To ±0.003% of full scale range. I_{OUT} load = 100Ω || C_{EXT} = 13pF. DAC register alternately loaded with all 1s and all 0s.			0.8	1.5	μs
Digital to Analog Glitch Impulse		Measured with V_{REF} = 0V. I_{OUT} load = 100Ω C_{EXT} = 13pF. DAC register alternately loaded with all 1s and all 0s.			20		nV-sec
Multiplying Feedthrough Error		V_{REF} = ±10V, 10KHz sine wave. DAC register loaded with all 0s.	T_A = +25°C T_A = T_{MIN} to T_{MAX}		3 5		mVp-p
Power Supply Rejection Δ G/Δ V_{DD}		Δ V_{DD} = ±5%	T_A = +25°C T_A = T_{MIN} to T_{MAX}			±0.01 ±0.02	%/%
I_{OUT} Output Capacitance	C_{OUT}	DAC Register loaded with all 1s				260	pF
		DAC Register loaded with all 0s				130	
Output Noise Voltage Density (10Hz-100KHz)		Measured between R_{FB} and I_{OUT}			15		$nV\sqrt{Hz}$

Note 1: Specifications are guaranteed for V_{DD} of +11.4V to +15.75V. At V_{DD} of 5V device is still functional with degraded specifications.
Note 2: Measured with internal R_{FB} includes effects of leakage current and gain tempco.
Note 3: DAC register loaded with all 0s.
Note 4: Guaranteed by design.
Note 5: These characteristics are provided for design guidance only and are not subject to test.

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Pin Description

PIN #	NAME	FUNCTION
1	V_{REF}	Voltage Reference Input
2	R_{FB}	Feedback Resistor. Used to close the loop around an external op amp.
3	I_{OUT}	Current Output
4	AGND	Analog Ground. Reference point for external circuitry. This pin should carry minimum current.
5	DGND	Digital Ground
6-19	DB13-DB0	Data Inputs. DB13 (MSB), DB0 (LSB).
20	$\overline{LDAC}$	Asynchronous Load-DAC Control Input. Active Low.
21	$\overline{CS}$	Chip Select Control Input. Active Low.
22	$\overline{WR}$	Write Control Input. Active Low.
23	V_{DD}	Positive Supply Voltage Input. +12V to +15V, ±5% tolerance.
24	V_{SS}	Negative Supply Voltage Input. Bias pin for high temperature, low leakage configuration. To implement a low leakage system, this pin should be at a negative voltage. Otherwise, it can be connected to the AGND pin. See Figures 4 and 5 for the recommended circuitry.

Detailed Description

D/A Section

As shown in Figure 2, the basic MX7538 D/A section consists of an 11-bit R-2R resistor array, a 3-bit segmented resistor array, and NMOS current switches. The three MSBs of the digital input are decoded to drive switches A-G of the segmented array, and the remaining 11 bits drive switches S0-S10 of the R-2R array.

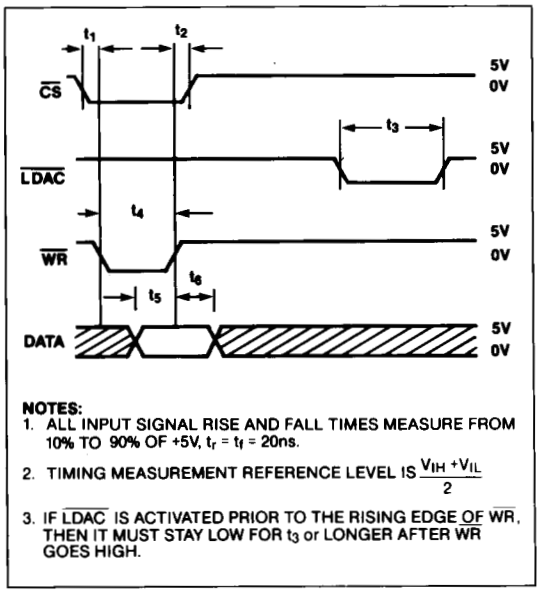
7/8th of the input current flows through the segmented resistors, and the remaining 1/8th flows through the R-2R resistor network. Switches A-G steer equally weighted currents to either AGND or I_{OUT}, depending on the three MSBs of the digital input, and switches S0-S10 steer binarily weighted currents to either AGND or I_{OUT}, depending on the 11 LSBs of the digital input. The input resistance at V_{REF} is constant, therefore, it can be driven by a voltage or current source of positive or negative polarity.

The MX7538 is optimized for unipolar output operation (analog output from 0 to $-V_{REF}$) although bipolar operation (analog output from $+V_{REF}$ to $-V_{REF}$) is possible with additional components (see Figure 5).

Logic Input Truth Table

$\overline{CS}$	$\overline{LDAC}$	$\overline{WR}$	FUNCTION
0	1	0	Load Input Register
1	0	X	Load DAC Register from Input Register
0	0	0	Input and DAC Registers are transparent
1	1	X	No operation
X	1	1	No operation

Note: X = Don't Care



NOTES:
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURE FROM 10% TO 90% OF +5V, $t_r = t_f = 20ns$.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH}+V_{IL}}{2}$
3. IF $\overline{LDAC}$ IS ACTIVATED PRIOR TO THE RISING EDGE OF $\overline{WR}$, THEN IT MUST STAY LOW FOR t_3 or LONGER AFTER $\overline{WR}$ GOES HIGH.

Figure 1. MX7538 Timing Diagram

The equivalent circuit for the analog portion of the DAC is shown in Figure 3. C_{OUT} varies from about 90 to 180pF depending on the digital code. Ro, the equivalent output resistance of the DAC, also varies with input code. $g(V_{REF},N)$ is the Thevenin equivalent voltage generator due to the reference input voltage, V_{REF}, and the transfer function of the R-2R ladder, N.

Digital Section

All digital inputs are both TTL and 5V CMOS logic compatible, with typical input currents of less than 1nA. Further, digital inputs are protected against electrostatic discharge (ESD). To minimize power supply current high and low logic levels (V_{INH} and V_{INL}) digital input voltages should be kept close to 5V and 0V, respectively.

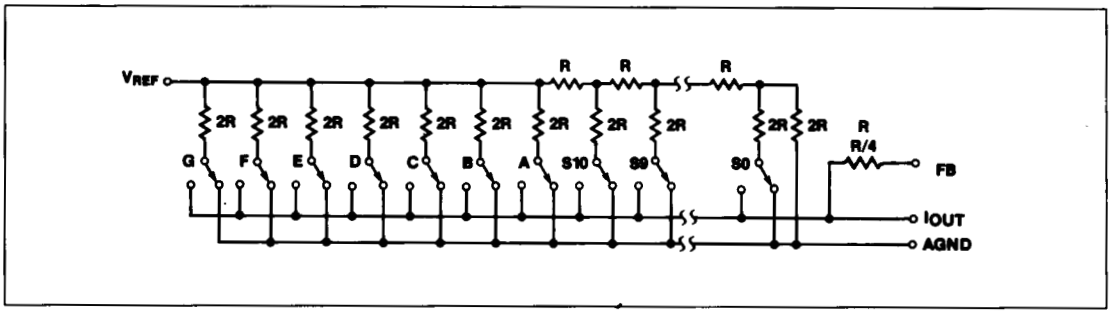


Figure 2. Simplified Circuit Diagram for the MX7538 D/A Section

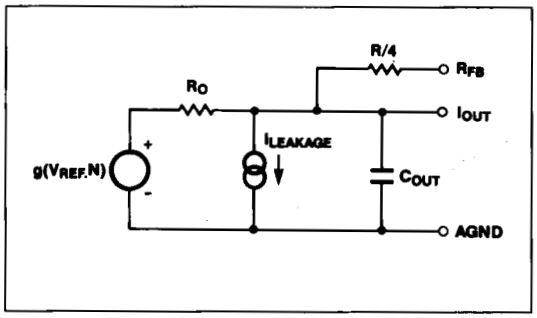


Figure 3. MX7538 Equivalent Analog Output Circuit

Application Information

Unipolar Operation (2-Quadrant Multiplication)

Figure 4 shows the circuit diagram for unipolar binary operation. With an AC input, the circuit performs 2-quadrant multiplication. The code table for Figure 4 is given in Table 1.

Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when high speed op amps are used. Note that the polarity of the output is the inverse of the reference input.

Typical connections for unipolar operation are shown in Figure 4. R3 and R4 are included for gain adjustment. However, if precision exceeding that specified in the Electrical Characteristics is not required, R3 and R4 may be omitted.

Offset Error Adjustment

1. Load DAC register with all 0s.
2. Adjust offset of amplifier A1 so that V_{OUT} is at a minimum (i.e., $\leq 30\mu V$).

Gain Error Adjustment

1. Load DAC register with all 1s.
2. Trim potentiometer, R3, so that $V_{OUT} = -V_{IN}$ (16383/16384).

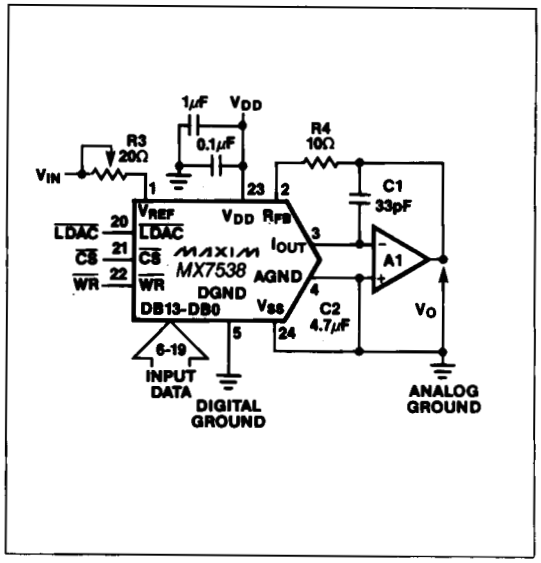


Figure 4. Unipolar Binary Operation

Table 1. Unipolar Binary Code

BINARY NUMBER MSB LSB	ANALOG OUTPUT
11 1111 1111 1111	$-V_{IN}\left(\frac{16383}{16384}\right)$
10 0000 0000 0000	$-V_{IN}\left(\frac{8192}{16384}\right) = -1/2\ V_{IN}$
00 0000 0000 0001	$-V_{IN}\left(\frac{1}{16384}\right)$
00 0000 0000 0000	0V

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In fixed reference applications, full scale can also be adjusted by omitting R3 and R4 and trimming the reference voltage magnitude. In many applications, the excellent Gain Tempco and Gain Error specifications eliminate the need for gain adjustment. However, if trim resistors are required and the DAC is to operate over a wide temperature range, low tempco (<300ppm/°C) resistors must be used.

Bipolar Operation (4-Quadrant Multiplication)

Bipolar, or 4-quadrant operation, is shown in Figure 5. This configuration uses offset binary coding. With the DAC loaded to 10 0000 0000 0000, adjust R3 for V_{OUT} = 0V. Alternatively, one can omit R3 and R4 and adjust the ratio of R7 and R8 for V_{OUT} = 0V. Full scale trimming is done by adjusting the amplitude of V_{IN} or by varying the value of R9.

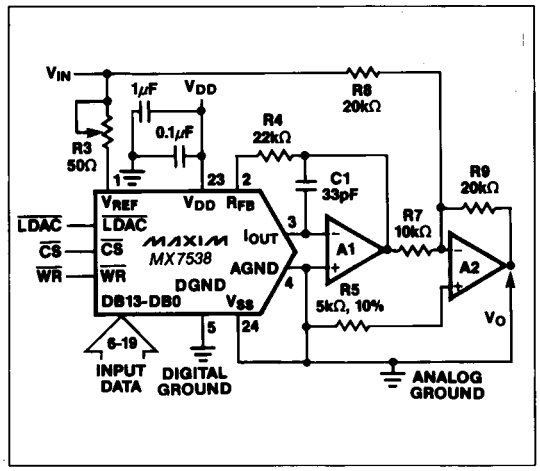

Figure 5. Bipolar Operation

Table 2. Bipolar Code for Offset Binary

BINARY NUMBER MSB LSB	ANALOG OUTPUT
11 1111 1111 1111	$+V_{IN}\left(\frac{8191}{8192}\right)$
10 0000 0000 0001	$+V_{IN}\left(\frac{1}{8192}\right)$
10 0000 0000 0000	0
01 1111 1111 1111	$-V_{IN}\left(\frac{1}{8192}\right)$
00 0000 0000 0000	$-V_{IN}\left(\frac{8192}{8192}\right)$

Resistors R7, R8, R9 must be matched to 0.003%. Mismatching of R7 and R8 causes both offset and full scale errors. For wide temperature range operation, resistors should be of the same material so that their temperature coefficients match and track.

Table 2 shows the Offset Binary Code obtained with the circuit of Figure 5. Note that by inverting the MSB of the DAC, a 2's Complement transfer function is obtained.

Grounding Considerations

Since I_{OUT} and the output amplifier's noninverting input are sensitive to offset voltages, nodes that need to be grounded should be connected directly to a "single point" ground through a separate, very low resistance path. Note that the output currents at I_{OUT} and AGND vary with input code and create code dependent errors if these terminals are connected to ground (or a virtual ground) through a resistive path.

It is important to use a proper grounding technique to obtain high accuracy.

Low Leakage Configuration

Leakage current in the DAC flowing into the I_{OUT} line can cause gain, linearity and offset errors. Leakage is worse at high temperatures.

Dynamic Considerations

In static or DC applications, the AC characteristics of the output amplifier are not critical. In higher speed applications, where either the reference input is an AC signal or the DAC output must quickly settle to a new programmed value, the AC parameters of the output op amp must be considered.

Another error source in dynamic applications is parasitic coupling of signals from the V_{REF} terminal to I_{OUT}. This coupling is normally caused by board layout and lead-to-lead package capacitance. Signals can also be injected into the DAC outputs when the digital inputs are switched. This digital feedthrough is mostly dependent on circuit board layout and on-chip capacitive coupling. Layout induced feedthrough can be minimized with guard traces between digital inputs, V_{REF}, and the DAC outputs.

Digital Feedthrough

In the microprocessor interface diagrams shown in Figures 6-8, the digital inputs of the DAC are directly connected to the microprocessor bus. Even when the device is not selected, activity on the bus can feed through on the DAC output through package capacitance and show up as noise. This can be minimized by isolating the DAC from the digital bus as shown in Figure 9.

Compensation

A compensation capacitor, C1, may be needed when the DAC is used with a high speed output amplifier. The purpose of the capacitor is to cancel the pole formed by the DAC's output capacitance and internal feedback resistance. Its value depends on the type of op amp used but typical values range from 10 to 33pF. Too small a value causes output ringing while excess capacitance overdamps the output. The size of C1 can be minimized, and output settling performance improved, by keeping the PC board traces short and keeping stray capacitance at I_{OUT} as small as possible.

Bypassing

A 1μF bypass capacitor, in parallel with a 0.1μF ceramic cap, should be connected as close to the DAC's V_{DD} and GND pins as possible. High frequency noise rejection is optimized if tantalum is used for the 1μF capacitor. A V_{SS} decoupling capacitor of 4.7μF is also required if a low leakage configuration is desired.

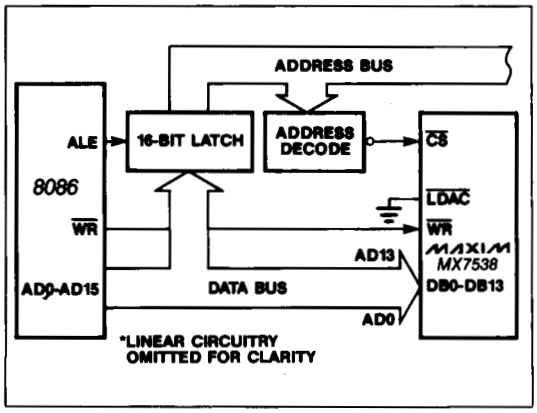

Figure 6. MX7538 - 8086 Interface Circuit

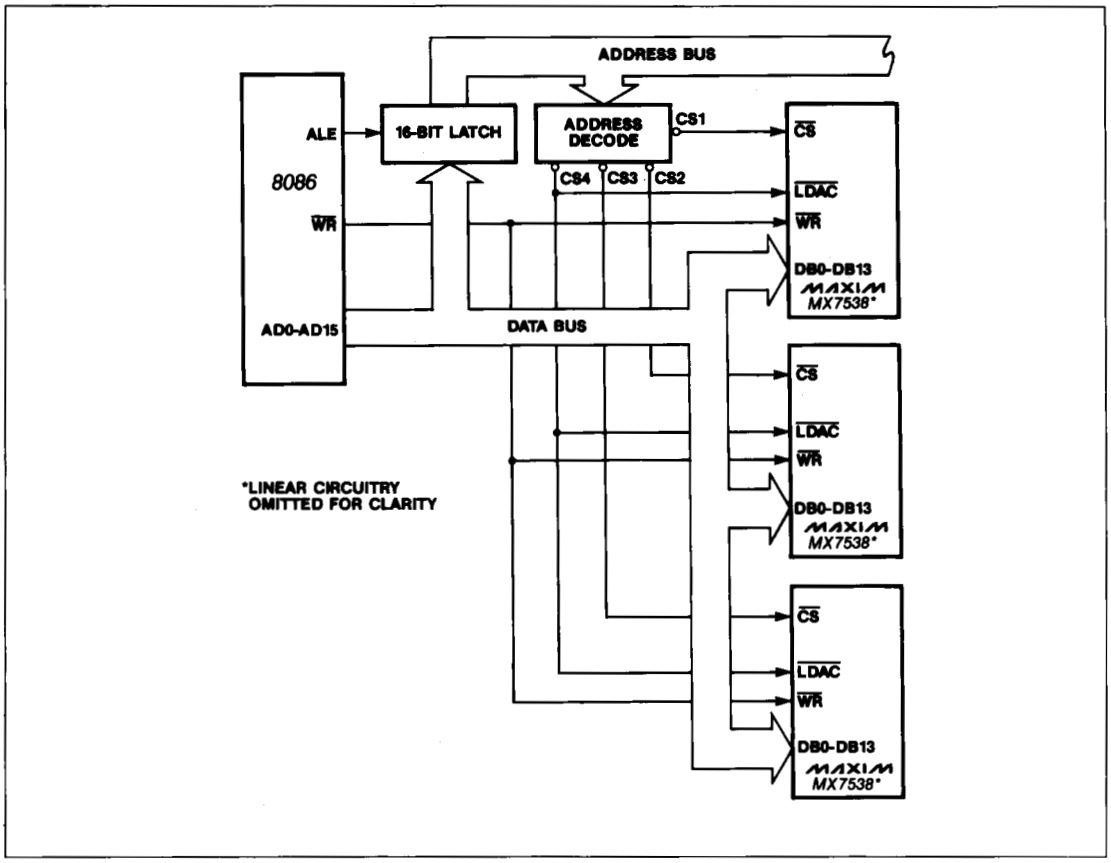

Figure 7. MX7538 - 8086 Interface: Multiple DAC System

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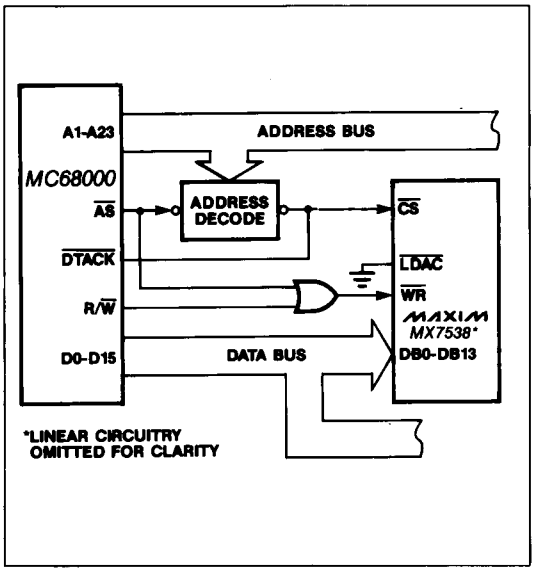


Figure 8. MX7538 - MC6800 Interface

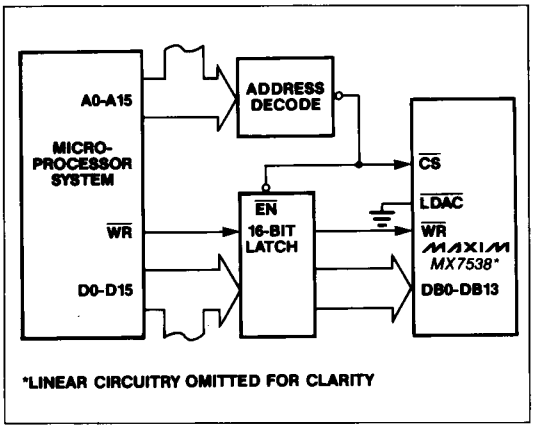


Figure 9. MX7538 Interface Circuit Using Latches to Minimize Digital Feedthrough

The MX7538 has high-impedance digital inputs. To minimize noise pick-up, they should be connected to either V_{DD} or GND terminals when not used. It is also good practice to connect active inputs to V_{DD} or GND through high valued resistors (1MΩ) to prevent static charge accumulation if these pins are left floating, as might be the case when a circuit card is left unconnected.

Op Amp Selection

Input offset voltage (V_{OS}), input bias current (I_B) and offset voltage drift (TC V_{OS}) are key parameters determining choice of a suitable amplifier (see Table 3). To maintain specified accuracy with V_{REF} of 10V, V_{OS} should be less than 30µV, and I_B should be less than 2nA. Open loop gain should be greater than 340,000. Maxim's MAX400 has low V_{OS}(10µV max), low I_B(2nA) and low TC V_{OS}(0.3µV/°C max). This op amp can be used without adjustments. For medium frequency applications the OP-27 is suggested and for even higher frequency applications the HA 2620 is recommended. Note however, these op amps require external offset adjustment.

Microprocessor Interfacing

Maxim MX7538 to 8086A Interface

Figure 6 shows the 8086 16-bit microprocessor interfacing to a single MX7538. In this setup the double buffering feature of the DAC is not used. AD13-AD0 of the 16-bit data bus are connected to the DAC data bus (DB13-DB0). The 14-bit word is written to the DAC in one MOV instruction, and the analog output responds immediately. In this example the DAC address is D000. A software routine for Figure 6 is given in Table 4.

In a multiple DAC system, the double buffering of the DAC chips allows the user to simultaneously update all DACs. In Figure 7, a 14-bit word is loaded into the Input Registers of each of the DACs in sequence. Then, with one instruction to the appropriate address, CS4 (i.e., $\overline{LDAC}$) is brought low, updating all the DACs simultaneously.

MX7538 to MC68000 Interface

Figure 8 shows the MX7538 interfaced with the MC68000. The following routine in Table 5 inputs data to the MX7538 from the MC68000. First, data is written to the DAC Input Registers, then data is output via the DAC Register.

Table 3. Op Amp Selection

OP AMP	INPUT OFFSET VOLTAGE (V_{OS})	INPUT BIAS CURRENT (I_B)	OFFSET VOLTAGE DRIFT (TC V_{OS})	SETTLING TO 0.003% FS
MAX400	10µV	2nA	0.3µV/°C	50µs
Maxim OP-07	25µV	2nA	0.6µV/°C	50µs
AD544L*	500µV	25pA	5µV/°C	5µs
HA2620*	4mV	35nA	20µV/°C	0.8µs

*AD544L is an Analog Devices part, HA2620 is a Harris Semiconductor part.

Table 4. Loading MX7538 from an 8086

ASSUME DS:DACLOAD, CS:DACLOAD DACLOAD SEGMENT AT 000			
00	8CC9	MOV CX,CS	:DEFINE DATA SEGMENT REGISTER EQUAL
02	8ED9	MOVDS,CX	:TO CODES SEGMENT REGISTER
04	BF00D0	MOVDI,#D000	:LOAD DI WITH D000
07	C705"YZWX"	MOV MEM,#YZWX	:DAC LOADED WITH WXYZ
0B	EA0000		:CONTROL IS RETURNED TO THE
0E	00FF		MONITOR PROGRAM

Table 5. Loading MX7538 from a 68000

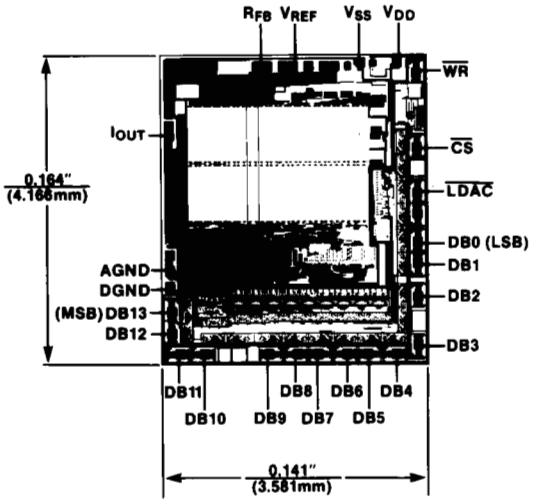
01000	MOVE.W	#W,D0	The desired DAC data, W, is loaded into Data Register 0.
	MOVE.W	D0,$E000	The Data W is transferred between D0 and DAC register.
	MOVE.B	#228,D7	Control returned to the System Monitor Program.
	TRAP	#14	

Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE*	ERROR
MX7538AQ	-25°C to + 85°C	CERDIP**	±2 LSB
MX7538BQ	-25°C to +85°C	CERDIP**	±1 LSB
MX7538AD	-25°C to +85°C	Ceramic SB	±2 LSB
MX7538BD	-25°C to +85°C	Ceramic SB	±1 LSB
MX7538SQ	-55°C to +125°C	CERDIP**	±2 LSB
MX7538TQ	-55°C to +125°C	CERDIP**	±1 LSB
MX7538SD	-55°C to +125°C	Ceramic SB	±2 LSB
MX7538TD	-55°C to +125°C	Ceramic SB	±1 LSB

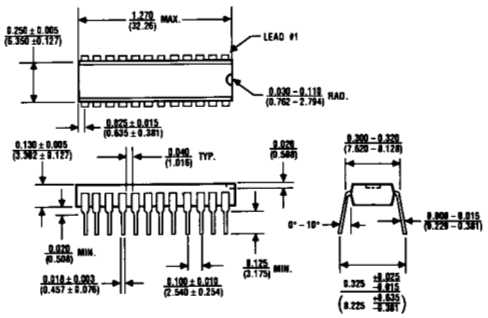
* *All devices — 24 lead packages*
PLCC — 28 lead package
** *Maxim reserves the right to ship Ceramic SB in lieu of CERDIP packages.*

Chip Topography

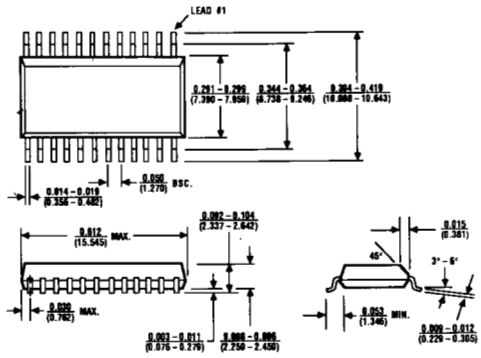


µP Compatible CMOS 14-Bit D/A Converter

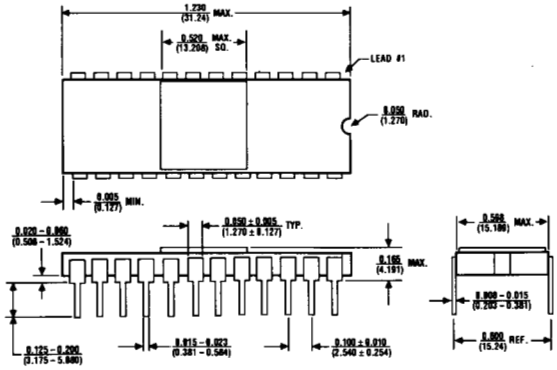
Package Information



24 Lead Plastic Narrow DIP (NG)
θ_{JA} = 120°C/W
θ_{JC} = 60°C/W

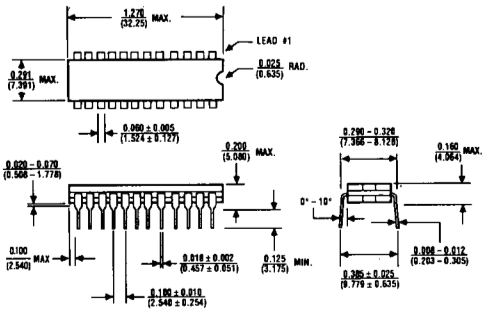


24 Lead Small Outline, Wide (WG)
θ_{JA} = 85°C/W
θ_{JC} = 45° C/W

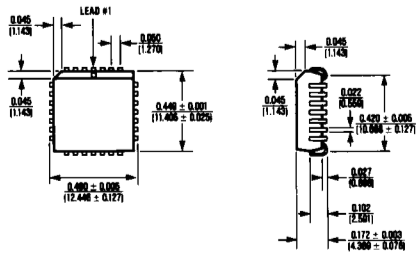


24 Lead Ceramic Sidebraze (DG)
θ_{JA} = 50°C/W
θ_{JC} = 15°C/W

Package Information (continued)



24 Lead Narrow CERDIP (RG)
θ_{JA} = 80°C/W
θ_{JC} = 40°C/W



28 Lead Plastic Chip Carrier (Quad Pak) (QI)
θ_{JA} = 100°C/W
θ_{JC} = 45°C/W