

# 1:2 CML Fanout Buffer with Selectable Clock Input

## Features

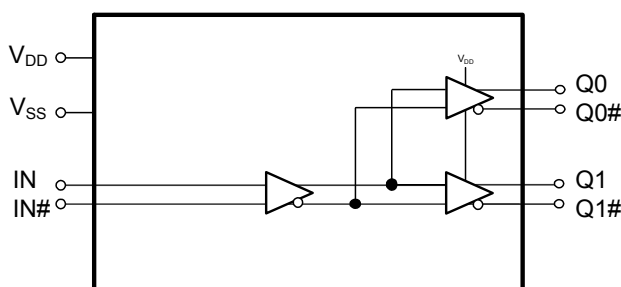
- One current mode logic (CML), High-speed current steering logic (HCSL), or low-voltage positive emitter-coupled logic (LVPECL) input pair distributed to two CML output pairs
- 20-ps maximum output-to-output skew
- 480-ps maximum propagation delay
- 0.15-ps maximum additive RMS phase jitter at 156.25 MHz (12-kHz to 20-MHz offset)
- Up to 1.5 GHz operation
- 8-pin thin shrunk small outline package (TSSOP) package
- 2.5-V or 3.3-V operating voltage <sup>[1]</sup>
- Commercial and industrial operating temperature range

## Functional Description

The CY2DM1502 is an ultra-low noise, low-skew, low-propagation delay 1:2 CML, HCSL, or LVPECL to CML fanout buffer targeted to meet the requirements of high-speed clock distribution applications. The device has a fully differential internal architecture that is optimized to achieve low additive jitter and low skew at operating frequencies of up to 1.5 GHz.

For a complete list of related documentation, [click here](#).

## Logic Block Diagram



### Note

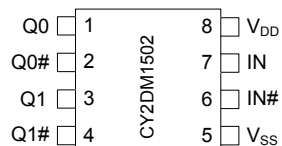
1. Input AC-coupling capacitors are required for voltage-translation applications.

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## Pinouts

Figure 1. 8-pin TSSOP Package pinout



## Pin Definitions

Pin No.	Pin Name	Pin Type	Description
1, 3	Q(0:1)	Output	CML output clocks
2, 4	Q(0:1)#	Output	CML complementary output clocks
5	V <sub>SS</sub>	Power	Ground
6	IN#	Input	CML/HCSL/LVPECL complementary input clock
7	IN	Input	CML/HCSL/LVPECL input clock
8	V <sub>DD</sub>	Power	Power supply

## Absolute Maximum Ratings

Parameter	Description	Condition	Min	Max	Unit
$V_{DD}$	Supply voltage	Nonfunctional	−0.5	4.6	V
$V_{IN}^{[2]}$	Input voltage, relative to $V_{SS}$	Nonfunctional	−0.5	lesser of 4.0 or $V_{DD} + 0.4$	V
$V_{OUT}^{[2]}$	DC output or I/O voltage, relative to $V_{SS}$	Nonfunctional	−0.5	lesser of 4.0 or $V_{DD} + 0.4$	V
$T_S$	Storage temperature	Nonfunctional	−55	150	°C
$ESD_{HBM}$	Electrostatic discharge (ESD) protection (Human body model)	JEDEC STD 22-A114-B	2000	–	V
$L_U$	Latch up		Meets or exceeds JEDEC Spec JESD78B IC Latch-up Test		
UL–94	Flammability rating	At 1/8 in	V-0		
MSL	Moisture sensitivity level		3		

## Operating Conditions

Parameter	Description	Condition	Min	Max	Unit
$V_{DD}$	Supply voltage	2.5-V supply	2.375	2.625	V
		3.3-V supply	3.135	3.465	V
$T_A$	Ambient operating temperature	Commercial	0	70	°C
		Industrial	−40	85	°C
$t_{PU}$	Power ramp time	Power-up time for $V_{DD}$ to reach minimum specified voltage (power ramp must be monotonic).	0.05	500	ms

### Note

2. The voltage on any I/O pin cannot exceed the power pin during power up. Power supply sequencing is NOT required.

## DC Electrical Specifications

( $V_{DD} = 3.3\text{ V} \pm 5\%$  or  $2.5\text{ V} \pm 5\%$ ;  $T_A = 0\text{ }^{\circ}\text{C}$  to  $70\text{ }^{\circ}\text{C}$  (Commercial) or  $-40\text{ }^{\circ}\text{C}$  to  $85\text{ }^{\circ}\text{C}$  (Industrial))

Parameter	Description	Condition	Min	Max	Unit
$I_{DD}$	Operating supply current	All CML outputs floating (internal $I_{DD}$ )	–	50	mA
$V_{IH}$	Input high voltage, CML/HCSL/LVPECL inputs IN and IN#		–	$V_{DD} + 0.3$	V
$V_{IL}$	Input low voltage, CML/HCSL/LVPECL inputs IN and IN#		–0.3	–	V
$V_{ID}^{[3]}$	Input differential amplitude	See <a href="#">Figure 2 on page 7</a>	0.4	1.0	V
$V_{ICM}$	Input common mode voltage	See <a href="#">Figure 2 on page 7</a>	0.2	$V_{DD} - 0.2$	V
$I_{IH}$	Input high current, CML/HCSL/LVPECL inputs IN and IN#	Input = $V_{DD}^{[4]}$	–	150	$\mu\text{A}$
$I_{IL}$	Input low current, CML/HCSL/LVPECL inputs IN and IN#	Input = $V_{SS}^{[4]}$	–150	–	$\mu\text{A}$
$V_{OH}$	CML output high voltage	Terminated with $50\text{ }\Omega$ to $V_{DD}^{[5]}$	$V_{DD} - 0.1$	–	V
$V_{OL}$	CML output low voltage	Terminated with $50\text{ }\Omega$ to $V_{DD}^{[5]}$	$V_{DD} - 0.7$	$V_{DD} - 0.3$	V
$C_{IN}$	Input capacitance	Measured at 10 MHz; per pin	–	3	pF

## Thermal Resistance

Parameter <sup>[6]</sup>	Description	Test Conditions	8-pin TSSOP	Unit
$\theta_{JA}$	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	162	$^{\circ}\text{C/W}$
$\theta_{JC}$	Thermal resistance (junction to case)		29	$^{\circ}\text{C/W}$

### Notes

- $V_{ID}$  minimum of 400 mV is required to meet all output AC Electrical Specifications. The device is functional with  $V_{ID}$  minimum of greater than 200 mV.
- Positive current flows into the input pin, negative current flows out of the input pin.
- Refer to [Figure 3 on page 7](#).
- These parameters are guaranteed by design and are not tested.

## AC Electrical Specifications

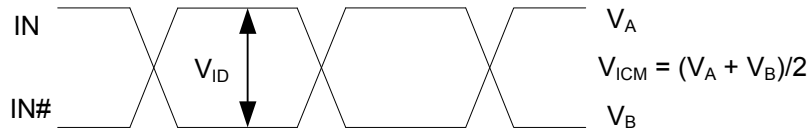
( $V_{DD} = 3.3 \text{ V} \pm 5\%$  or  $2.5 \text{ V} \pm 5\%$ ;  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$  (Commercial) or  $-40^\circ\text{C}$  to  $85^\circ\text{C}$  (Industrial))

Parameter	Description	Condition	Min	Typ	Max	Unit
$F_{IN}$	Input frequency		DC	–	1.5	GHz
$F_{OUT}$	Output frequency	$F_{OUT} = F_{IN}$	DC	–	1.5	GHz
$V_{PP}$	CML differential output voltage peak-to-peak, single-ended. Terminated with $50 \Omega$ to $V_{DD}$ <sup>[5]</sup>	$F_{OUT} = \text{DC to } 150 \text{ MHz}$	250	–	700	mV
		$F_{OUT} = >150 \text{ MHz to } 1.5 \text{ GHz}$	250	–	600	mV
$t_{PD}$ <sup>[7]</sup>	Propagation delay input pair to output pair	Input rise/fall time $< 1.5 \text{ ns}$ (20% to 80%)	–	–	480	ps
$t_{ODC}$ <sup>[8]</sup>	Output duty cycle	50% duty cycle at input Frequency range up to 1 GHz	48	–	52	%
$t_{SK1}$ <sup>[9]</sup>	Output-to-output skew	Any output to any output, with same load conditions at DUT	–	–	20	ps
$t_{SK1 D}$ <sup>[9]</sup>	Device-to-device output skew	Any output to any output between two or more devices. Devices must have the same input and have the same output load.	–	–	150	ps
$PN_{ADD}$	Additive RMS phase noise 156.25-MHz Input Rise/fall time $< 150 \text{ ps}$ (20% to 80%) $V_{ID} > 400 \text{ mV}$	Offset = 1 kHz	–	–	–120	dBc/Hz
		Offset = 10 kHz	–	–	–130	dBc/Hz
		Offset = 100 kHz	–	–	–135	dBc/Hz
		Offset = 1 MHz	–	–	–145	dBc/Hz
		Offset = 10 MHz	–	–	–153	dBc/Hz
		Offset = 20 MHz	–	–	–155	dBc/Hz
$t_{JIT}$ <sup>[10]</sup>	Additive RMS phase jitter (Random)	156.25 MHz, 12 kHz to 20 MHz offset; input rise/fall time $< 150 \text{ ps}$ (20% to 80%), $V_{ID} > 400 \text{ mV}$	–	–	0.15	ps
$t_R, t_F$ <sup>[11]</sup>	Output rise/fall time	50% duty cycle at input, 20% to 80% of full swing ( $V_{OL}$ to $V_{OH}$ ) Input rise/fall time $< 1.5 \text{ ns}$ (20% to 80%) Measured at 1 GHz	–	–	250	ps

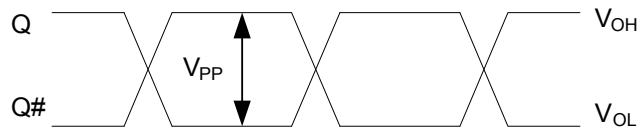
### Notes

7. Refer to Figure 4 on page 7.
8. Refer to Figure 5 on page 7.
9. Refer to Figure 6 on page 8.
10. Refer to Figure 7 on page 8.
11. Refer to Figure 8 on page 8.

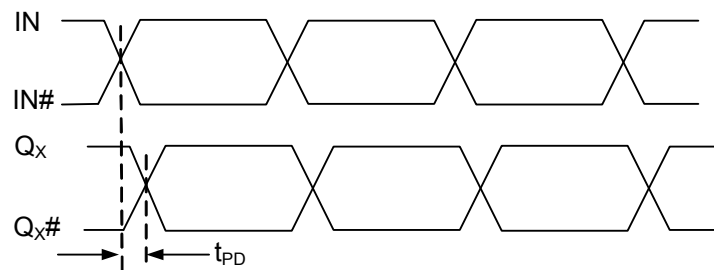
**Figure 2. Input Differential and Common Mode Voltages**



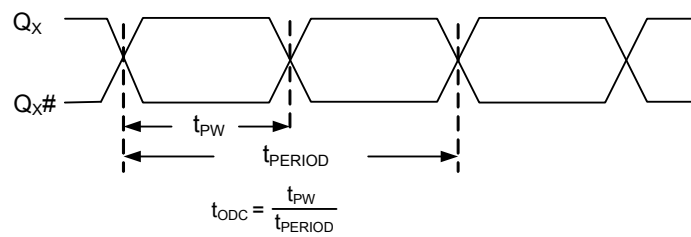
**Figure 3. Output Differential Voltage**



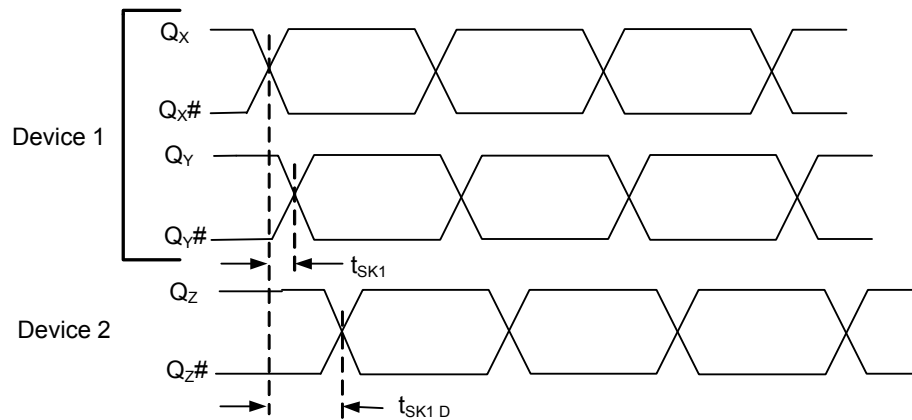
**Figure 4. Input to Any Output Pair Propagation Delay**



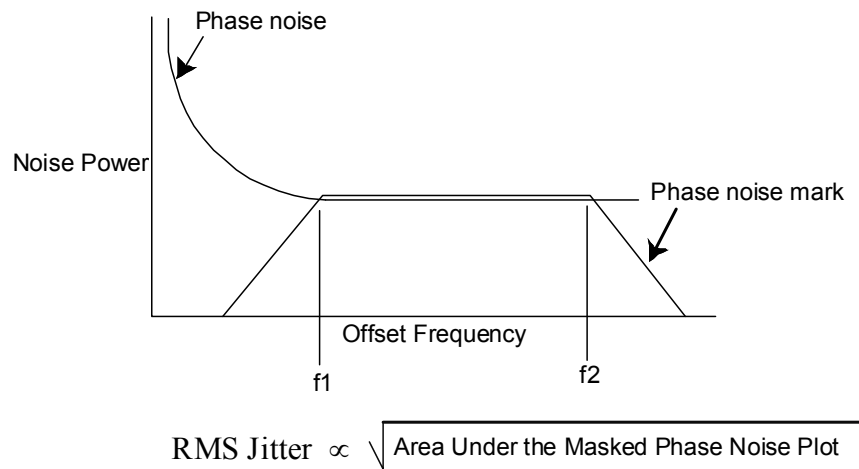
**Figure 5. Output Duty Cycle**



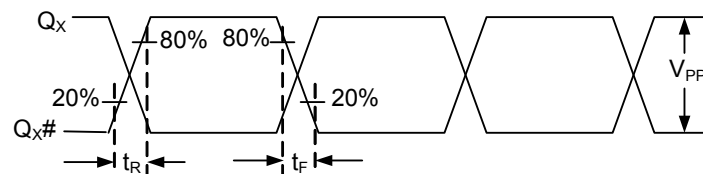
**Figure 6. Output-to-Output and Device-to-Device Skew**



**Figure 7. RMS Phase Jitter**



**Figure 8. Output Rise/Fall Time**

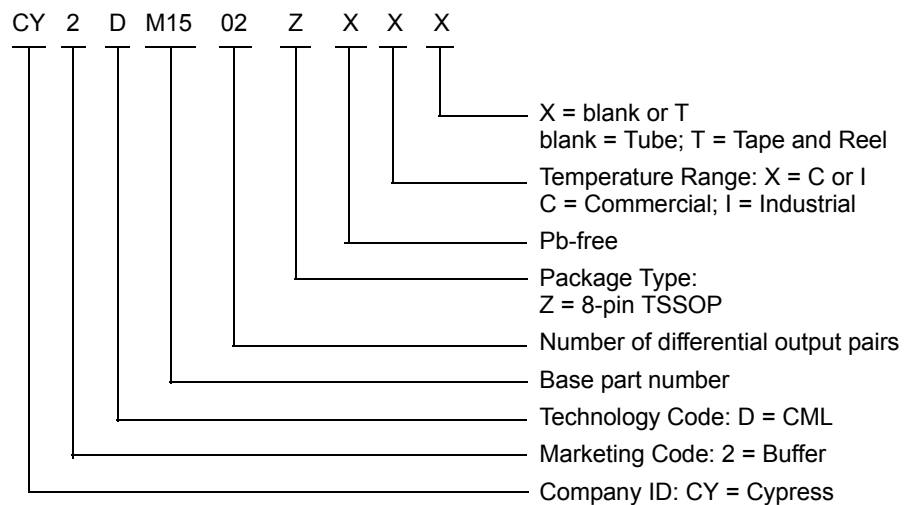




## Ordering Information

Part Number	Type	Production Flow
<b>Pb-free</b>		
CY2DM1502ZXI	8-pin TSSOP	Industrial, -40 °C to 85 °C
CY2DM1502ZXIT	8-pin TSSOP tape and reel	Industrial, -40 °C to 85 °C

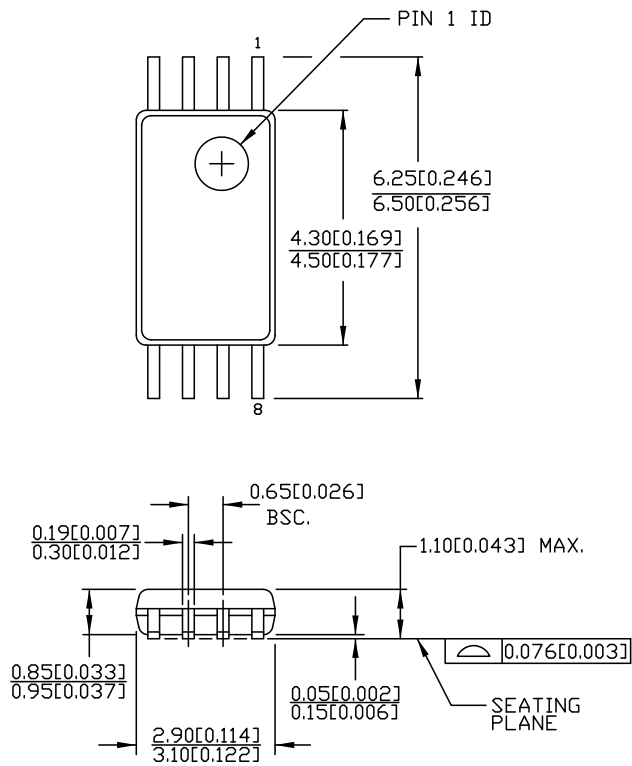
## Ordering Code Definitions



## Package Diagram

Figure 9. 8-pin TSSOP (4.40 MM Body) Z08.173/ZZ08.173 Package Outline, 51-85093

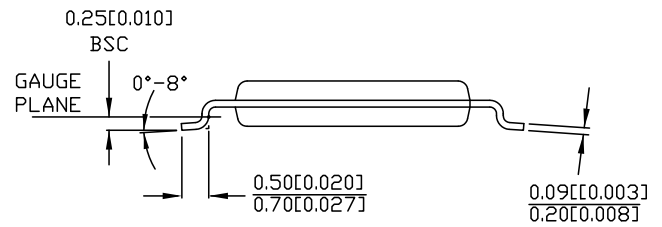
### 8 Lead TSSOP 4.40 MM BODY



DIMENSIONS IN MM[INCHES] MIN.  
MAX.

REFERENCE JEDEC MO-153

PART #	
Z08.173	STANDARD PKG.
ZZ08.173	LEAD FREE PKG.



51-85093 \*E

## Acronyms

**Table 1. Acronyms Used in this Document**

Acronym	Description
CML	current mode logic
ESD	electrostatic discharge
HBM	human body model
HCSL	high-speed current steering logic
JEDEC	joint electron devices engineering council
LVDS	low-voltage differential signal
LVC MOS	low-voltage complementary metal oxide semiconductor
LVPECL	low-voltage positive emitter-coupled logic
RMS	root mean square
TSSOP	thin shrunk small outline package

## Document Conventions

### Units of Measure

**Table 2. Units of Measure**

Symbol	Unit of Measure
°C	degree Celsius
dBc	decibels relative to the carrier
GHz	gigahertz
Hz	hertz
kΩ	kilohm
μA	microampere
μF	microfarad
μs	microsecond
mA	milliampere
ms	millisecond
mV	millivolt
MHz	megahertz
ns	nanosecond
Ω	ohm
pF	picofarad
ps	picosecond
V	volt
W	watt

## Document History Page

Document Title: CY2DM1502, 1:2 CML Fanout Buffer with Selectable Clock Input Document Number: 001-56315				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2782891	CXQ	10/09/09	New Datasheet.
*A	2838916	CXQ	01/05/2010	<p>Changed status from "ADVANCE" to "PRELIMINARY".</p> <p>Changed from 0.34 ps to 0.25 ps maximum additive jitter in "Features" on page 1 and in <math>t_{JIT}</math> in the AC Electrical Specs table on page 4.</p> <p>Added <math>t_{PU}</math> spec to the Operating Conditions table on page 2.</p> <p>Removed <math>V_{OH}</math> spec maximum of <math>V_{DD}</math> in the DC Electrical Specs table on page 3.</p> <p>Changed <math>V_{OL}</math> spec min from <math>V_{DD} - 0.6V</math> to <math>V_{DD} - 0.7V</math>; changed max from <math>V_{DD} - 0.4V</math> to <math>V_{DD} - 0.3V</math> in the DC Electrical Specs table on page 3.</p> <p>Removed <math>V_{OD}</math> spec of minimum 300 mV, maximum 450 mV in the DC Electrical Specs table on page 3.</p> <p>Added <math>R_P</math> spec in the DC Electrical Specs table on page 3. Min = 60 k<math>\Omega</math>, Max = 140 k<math>\Omega</math>.</p> <p>Added a measurement definition for <math>C_{IN}</math> in the DC Electrical Specs table on page 3.</p> <p>Added <math>V_{PP}</math> spec to the AC Electrical Specs table on page 4. <math>V_{PP}</math> max = 700 mV for DC - 150 MHz and max = 600 mV for 150 MHz to 1.5 GHz. <math>V_{PP}</math> min = 250 mV over the entire range.</p> <p>Changed letter case and some names of all the timing parameters in the AC Electrical Specs table on page 4 to be consistent with EROS.</p> <p>Lowered all additive phase noise mask specs by 3 dB in the AC Electrical Specs table on page 4.</p> <p>Added condition to <math>t_R</math> and <math>t_F</math> specs in the AC Electrical specs table on page 4 that input rise/fall time must be less than 1.5 ns (20% to 80%).</p> <p>Changed letter case and some names of all the timing parameters in Figures 3, 4, 5, 6 and 8, to be consistent with EROS.</p>
*B	3011766	CXQ	08/20/2010	<p>Changed from 0.25 ps to 0.11 ps maximum additive jitter in "Features" on page 1 and in <math>t_{JIT}</math> in the AC Electrical Specs table.</p> <p>Added note 3 to describe <math>I_{IH}</math> and <math>I_{IL}</math> specs.</p> <p>Removed reference to data distribution from "Functional Description".</p> <p>Changed <math>R_P</math> for diff inputs from 100 k<math>\Omega</math> to 150 k<math>\Omega</math> in the Logic Block Diagram and from 60 k<math>\Omega</math> min / 140 k<math>\Omega</math> max to 90 k<math>\Omega</math> min / 210 k<math>\Omega</math> max in the DC Electrical Specs table.</p> <p>Added max <math>V_{ID}</math> of 1.0V in DC Electrical Specs table.</p> <p>Updated phase noise specs for 1 k/10 k/100 k/1 M/20 MHz offset to -120/-130/-135/-150/-150dBC/Hz, respectively, in the AC Electrical Specs table.</p> <p>Added "Frequency range up to 1 GHz" condition to <math>t_{ODC}</math> spec.</p> <p>Updated package diagram.</p> <p>Added Acronyms and Ordering Code Definition.</p>
*C	3017258	CXQ	08/27/2010	Corrected Output Rise/Fall time diagram.
*D	3100234	CXQ	11/18/2010	<p>Updated Phase jitter to 0.15ps max from 0.11ps max.</p> <p>Changed <math>V_{IN}</math> and <math>V_{OUT}</math> specs from 4.0V to "lesser of 4.0 or <math>V_{DD} + 0.4</math>"</p> <p>Removed 200mA min LU spec, replaced with "Meets or exceeds JEDEC Spec JESD78B IC Latchup Test"</p> <p>Removed <math>R_P</math> spec for differential input clock pins <math>IN_X</math> and <math>IN_{X\#}</math>.</p> <p>Changed <math>C_{IN}</math> condition to "Measured at 10 MHz".</p> <p>Changed <math>PN_{ADD}</math> specs for 1MHz, 10MHz, and 20MHz offsets.</p> <p>Added condition "Measured at 1 GHz" to <math>t_R</math>, <math>t_F</math> specs.</p>
*E	3137726	CXQ	01/13/2011	<p>Removed "Preliminary" status heading.</p> <p>Removed resistors from <math>IN/IN\#</math> in <a href="#">Logic Block Diagram</a>.</p>
*F	3090938	CXQ	02/25/2011	Post to external web.

**Document History Page** (continued)

Document Title: CY2DM1502, 1:2 CML Fanout Buffer with Selectable Clock Input Document Number: 001-56315				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
*G	3410372	PURU	10/18/2011	Adding HCSL to <a href="#">Features</a> , <a href="#">Functional Description</a> , <a href="#">Pin Definitions</a> , and <a href="#">DC Electrical Specifications</a> sections. The min value of $V_{ICM}$ is changed from 0.5 to 0.2 in <a href="#">DC Electrical Specifications</a> .
*H	3878396	PURU	01/21/2013	Updated to new template.
*I	4587249	PURU	12/04/2014	Updated <a href="#">Functional Description</a> : Added "For a complete list of related documentation, <a href="#">click here</a> ." at the end. Updated <a href="#">Ordering Information</a> : Removed the prune part numbers CY2DM1502ZXC and CY2DM1502ZXCT. Updated <a href="#">Package Diagram</a> : spec 51-85093 – Changed revision from *D to *E.
*J	5272915	PSR	05/16/2016	Added <a href="#">Thermal Resistance</a> . Updated to new template.
*K	5966682	AESATMP8	11/14/2017	Updated logo and Copyright.

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