2N6782

Data Sheet November 1998 File Number 1592.2

3.5A, 100V, 0.600 Ohm, N-Channel Power MOSFET

The 2N6782 is an N-Channel enhancement mode silicon gate power field effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

Ordering Information

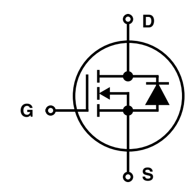
PART NUMBER	PACKAGE	BRAND
2N6782	TO-205AF	2N6782

NOTE: When ordering, use the entire part number.

Features

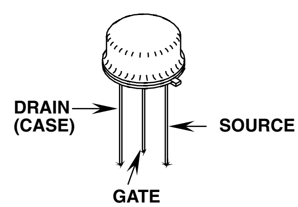
- 3.5A, 100V
- $r_{DS(ON)} = 0.600\Omega$
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- Related Literature
  - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol



Packaging

JEDEC TO-205AF



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		2N6782	UNITS
Drain to Source Breakdown Voltage (Note 1)	V_{DS}	100	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	100	V
Continuous Drain Current	I_D	3.5	A
$T_C = 100^oC$		2.25	A
Pulsed Drain Current (Notes 3)	I_{DM}	14	A
Gate to Source Voltage	V_{GS}	±20	V
Continuous Source Current (Body Diode)	I_S	3.5	A
Pulse Source Current (Body Diode)	I_{SM}	14	A
Maximum Power Dissipation	P_D	15	W
Linear Derating Factor		0.12	W/^{o}C
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	^{o}C
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^{o}C
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 0.25mA, V_{GS} = 0V	100	-	-	V
Gate to Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 0.5mA	2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100V, V_{GS} = 0V	-	-	250	μA
		V_{DS} = 80V, V_{GS} = 0V $T_C = 125^oC$	-	-	1000	μA
On-State Drain Current (Note 2)	$V_{DS(ON)}$	I_D = 3.5A, V_{GS} = 10V	-	-	2.1	V
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V	-	-	±100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	I_D = 2.25A, V_{GS} = 10V	-	0.5	0.600	Ω
		I_D = 2.25A, V_{GS} = 10V, $T_C = 125^oC$	-	-	1.080	Ω
Diode Forward Voltage (Note 2)	V_{SD}	$T_C = 25^oC$, I_S = 3.5A, V_{GS} = 0V	0.75	-	1.5	V
Forward Transconductance (Note 2)	g_{fs}	V_{DS} = 5V, I_D = 2.25A	1	1.5	3	S
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} ≅ 34V, I_D = 2.25A, R_G = 50Ω (Figure 17) MOSFET Switching Times are Essentially Independent of Operating Temperature	-	-	15	ns
Rise Time	t_r		-	-	25	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	-	25	ns
Fall Time	t_f		-	-	20	ns
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz (Figure 11)	60	135	200	pF
Output Capacitance	C_{OSS}		40	80	100	pF
Reverse Transfer Capacitance	C_{RSS}		10	20	25	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	8.33	^{o}C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Free Air Operation	-	-	175	^{o}C/W
Safe Operating Area	SOA	V_{DS} = 80V, I_D = 188mA	15	-	-	W
		V_{DS} = 4.28V, I_D = 3.5A	15	-	-	W

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reverse Recovery Time	t_{rr}	$T_J = 150^oC$, I_{SD} = 3.5A, dI_{SD}/dt = 100A/μs	-	200	-	ns
Reverse Recovered Charge	Q_{RR}	$T_J = 150^oC$, I_{SD} = 3.5A, dI_{SD}/dt = 100A/μs	-	1.0	-	μC

NOTES:

2. Pulse test: pulse width ≤ 300μs, duty cycle ≤ 2%.
3. Repetitive rating: pulse width limited by maximum junction temperature. See Transient Thermal Impedance curve (Figure 3).

Typical Performance Curves Unless Otherwise Specified

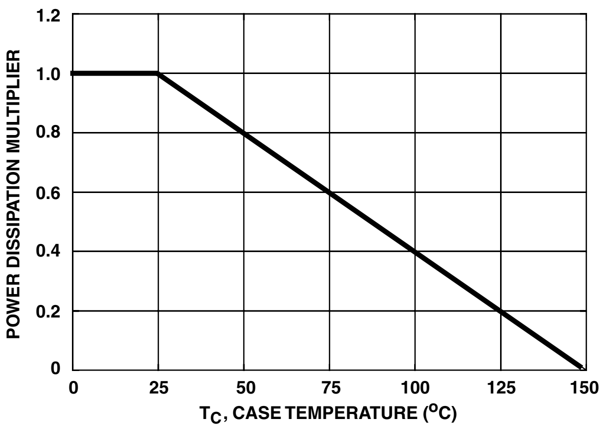


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

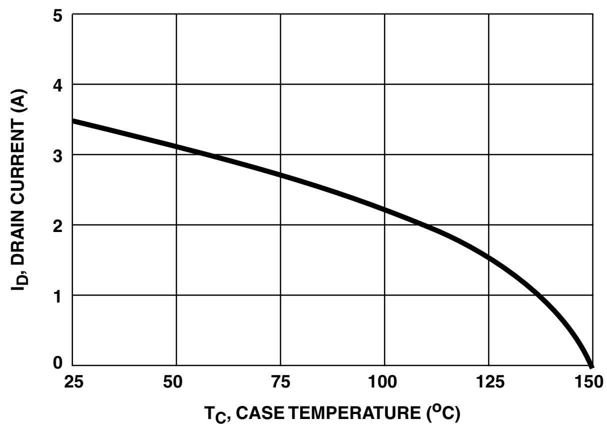


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

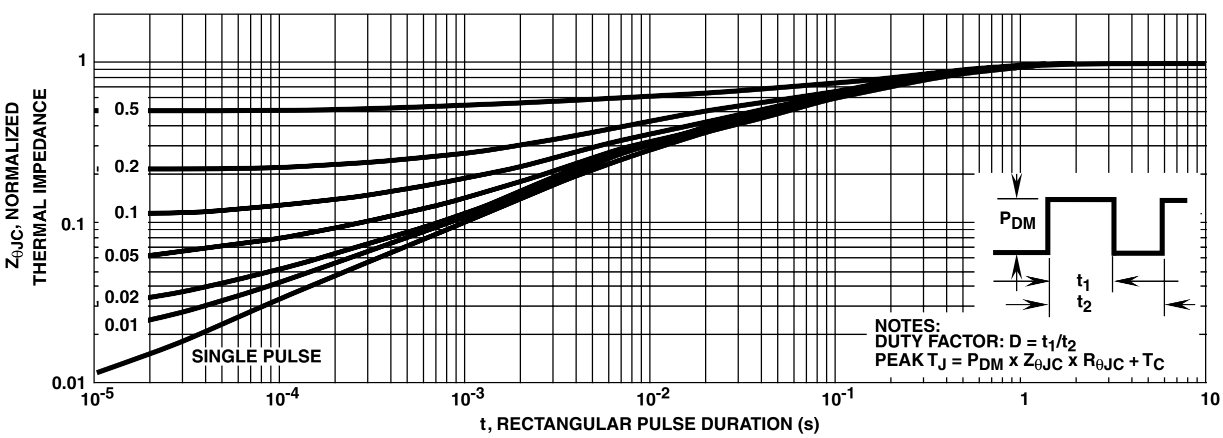


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

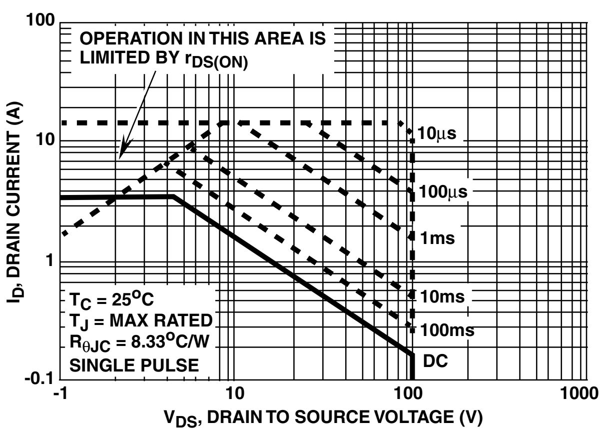


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

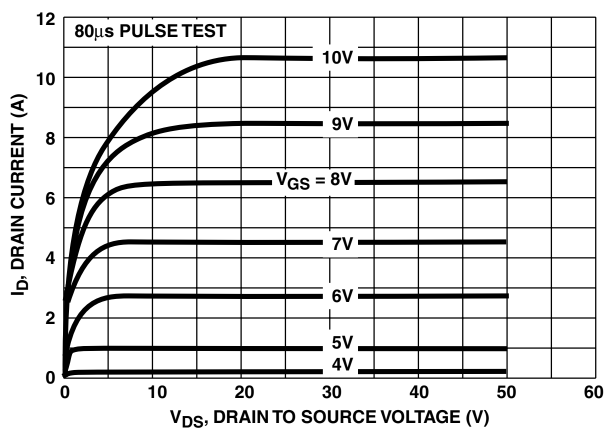


FIGURE 5. OUTPUT CHARACTERISTICS

Typical Performance Curves Unless Otherwise Specified **(Continued)**

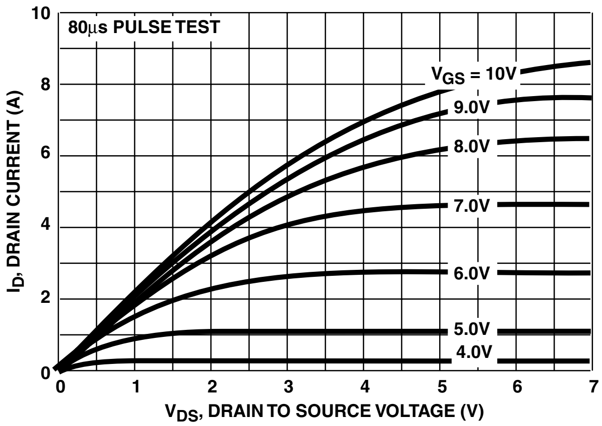


FIGURE 6. SATURATION CHARACTERISTICS

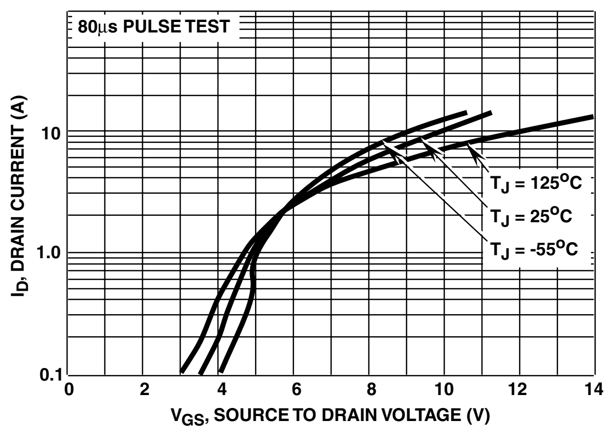
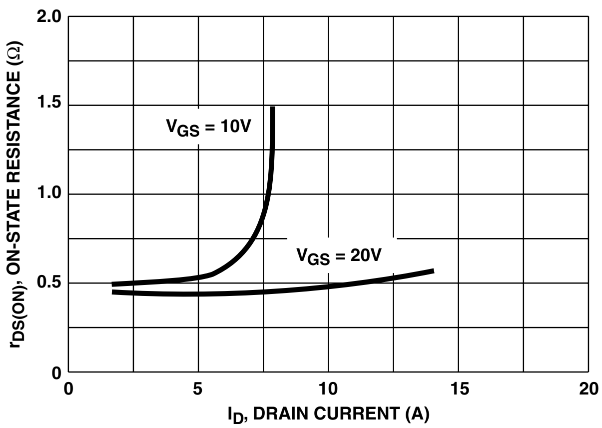


FIGURE 7. TRANSFER CHARACTERISTICS



NOTE: Heating effect of 2µs pulse is minimal.

FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

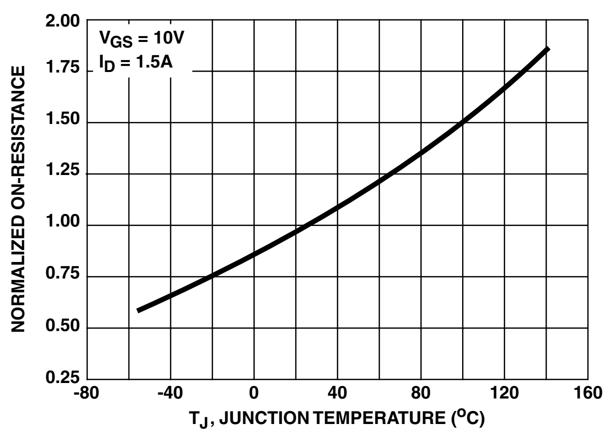


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

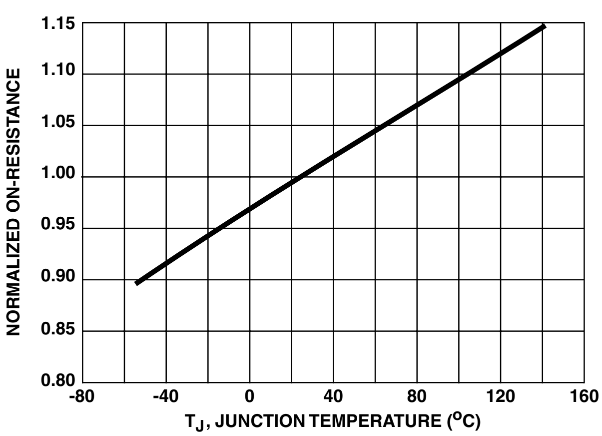


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

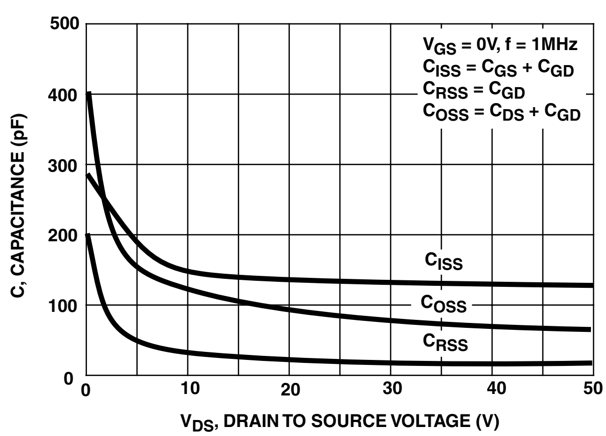


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

Typical Performance Curves Unless Otherwise Specified **(Continued)**

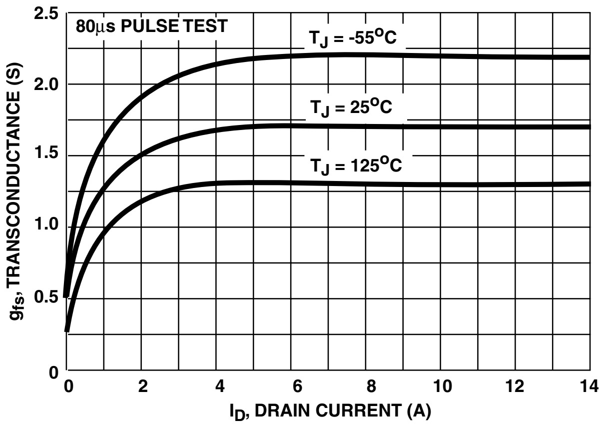


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

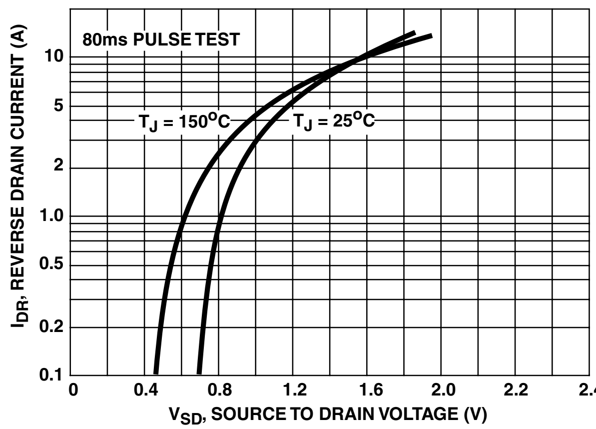


FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE

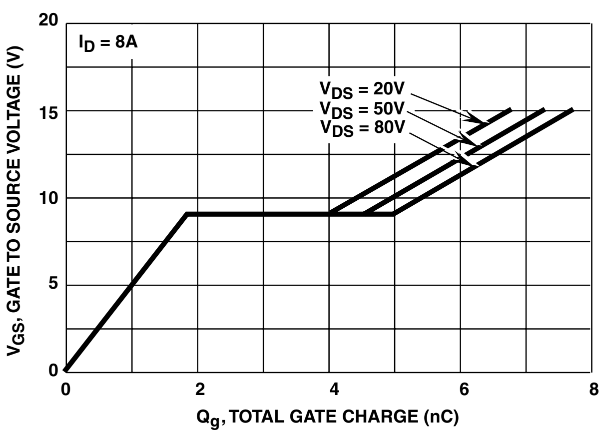


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

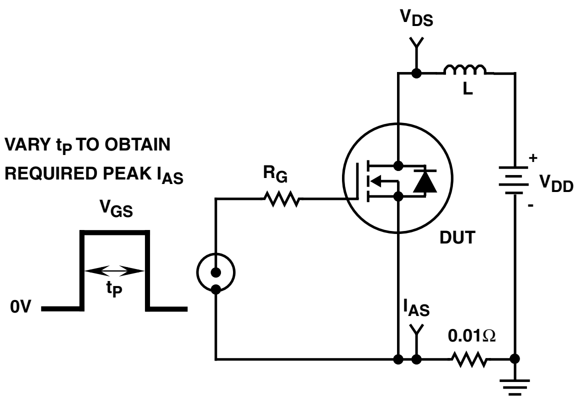


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

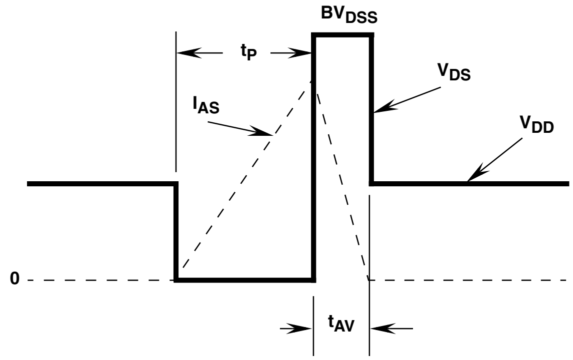


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

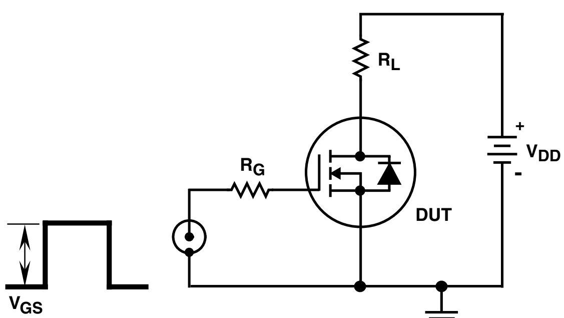


FIGURE 17. SWITCHING TIME TEST CIRCUIT

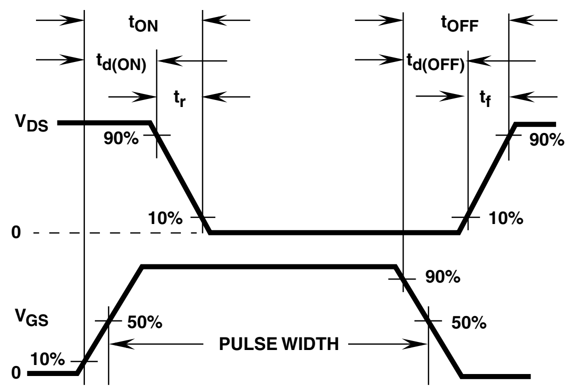


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

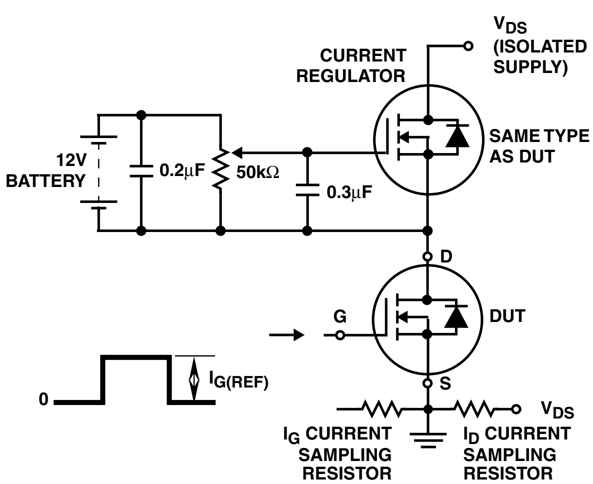


FIGURE 19. GATE CHARGE TEST CIRCUIT

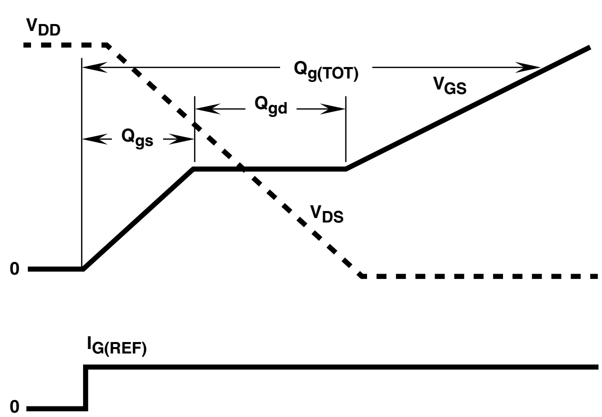


FIGURE 20. GATE CHARGE WAVEFORMS

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