

# PH4530L

N-channel TrenchMOS™ logic level FET

Rev. 02 — 26 January 2005

Product data sheet

## 1. Product profile

### 1.1 General description

Logic level N-channel enhancement mode field effect transistor in a plastic package using TrenchMOS™ technology.

### 1.2 Features

- Low thermal resistance
- Logic level gate drive
- SO8 equivalent area footprint
- Low on-state resistance.

### 1.3 Applications

- DC-to-DC converters
- Portable appliances
- Switched-mode power supplies
- Notebook computers.

### 1.4 Quick reference data

- $V_{DS} \leq 30 \text{ V}$
- $I_D \leq 80 \text{ A}$
- $P_{tot} \leq 62.5 \text{ W}$
- $R_{DS(on)} \leq 5.7 \text{ m}\Omega$ .

## 2. Pinning information

Table 1: Discrete pinning

| Pin   | Description                          | Simplified outline                     | Symbol        |
|-------|--------------------------------------|----------------------------------------|---------------|
| 1,2,3 | source                               | <p>Top view</p> <p>SOT669 (LFPACK)</p> | <p>mbb076</p> |
| 4     | gate                                 |                                        |               |
| mb    | mounting base;<br>connected to drain |                                        |               |

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### 3. Ordering information

Table 2: Ordering information

| Type number | Package |                                                              |         |
|-------------|---------|--------------------------------------------------------------|---------|
|             | Name    | Description                                                  | Version |
| PH4530L     | LFAK    | plastic single-ended surface mounted package (LFAK); 4 leads | SOT669  |

### 4. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

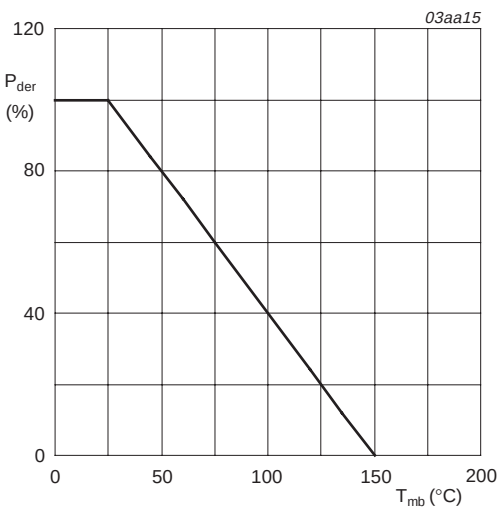
| Symbol    | Parameter                 | Conditions                                                                                        | Min | Max      | Unit |
|-----------|---------------------------|---------------------------------------------------------------------------------------------------|-----|----------|------|
| $V_{DS}$  | drain-source voltage (DC) | $25\text{ °C} \leq T_j \leq 150\text{ °C}$                                                        | -   | 30       | V    |
| $V_{GS}$  | gate-source voltage (DC)  |                                                                                                   | -   | $\pm 20$ | V    |
| $I_D$     | drain current (DC)        | $T_{mb} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; <a href="#">Figure 2</a> and <a href="#">3</a> | -   | 80       | A    |
|           |                           | $T_{mb} = 100\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; <a href="#">Figure 2</a>                      | -   | 240      | A    |
| $I_{DM}$  | peak drain current        | $T_{mb} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; <a href="#">Figure 3</a>     | -   | 50.7     | A    |
| $P_{tot}$ | total power dissipation   | $T_{mb} = 25\text{ °C}$ ; <a href="#">Figure 1</a>                                                | -   | 62.5     | W    |
| $T_{stg}$ | storage temperature       |                                                                                                   | -55 | +150     | °C   |
| $T_j$     | junction temperature      |                                                                                                   | -55 | +150     | °C   |

#### Source-drain diode

|          |                                     |                                                                    |   |     |   |
|----------|-------------------------------------|--------------------------------------------------------------------|---|-----|---|
| $I_S$    | source (diode forward) current (DC) | $T_{mb} = 25\text{ °C}$                                            | - | 52  | A |
| $I_{SM}$ | peak source (diode forward) current | $T_{mb} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ | - | 150 | A |

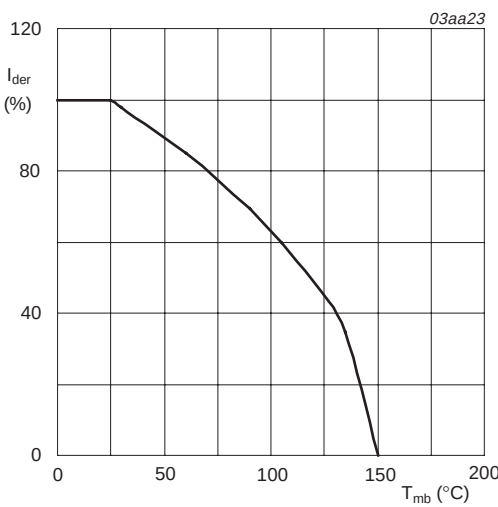
#### Avalanche ruggedness

|               |                                              |                                                                                                                                                               |   |     |    |
|---------------|----------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|---|-----|----|
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | unclamped inductive load; $I_D = 36.2\text{ A}$ ; $t_p = 0.24\text{ ms}$ ; $V_{DD} \leq 30\text{ V}$ ; $V_{GS} = 10\text{ V}$ ; starting $T_j = 25\text{ °C}$ | - | 130 | mJ |
|---------------|----------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|---|-----|----|



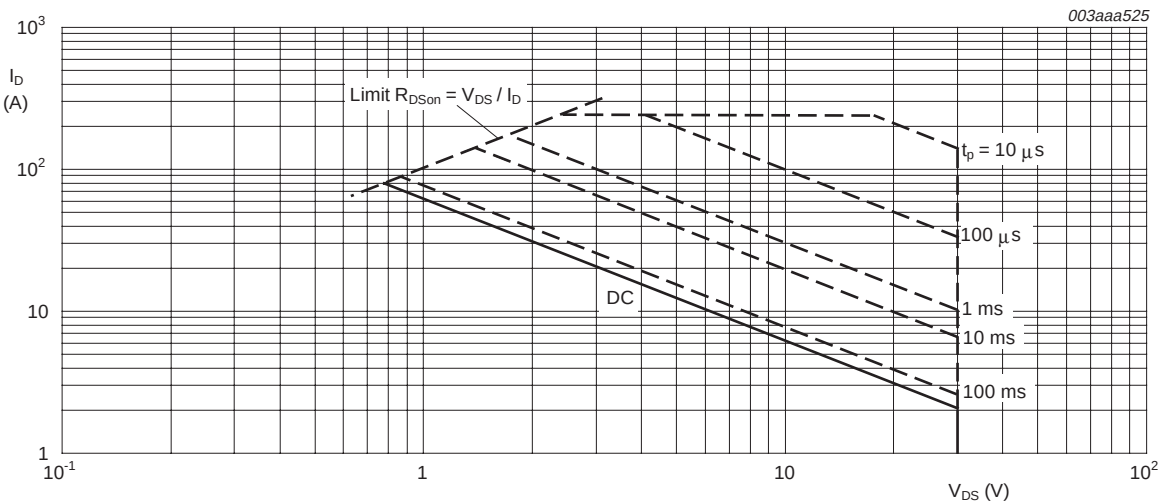
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



T<sub>mb</sub> = 25 °C; I<sub>DM</sub> is single pulse

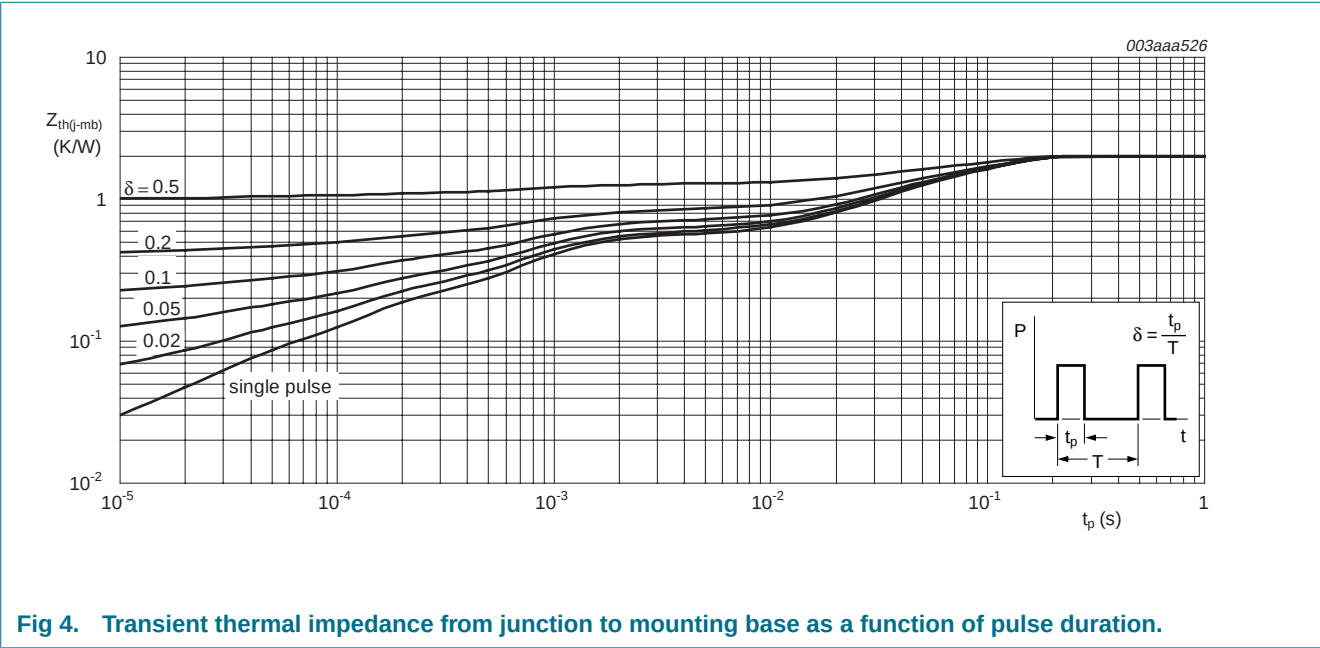
Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 4: Thermal characteristics

| Symbol         | Parameter                                         | Conditions | Min | Typ | Max | Unit |
|----------------|---------------------------------------------------|------------|-----|-----|-----|------|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | Figure 4   | -   | -   | 2   | K/W  |

5.1 Transient thermal impedance

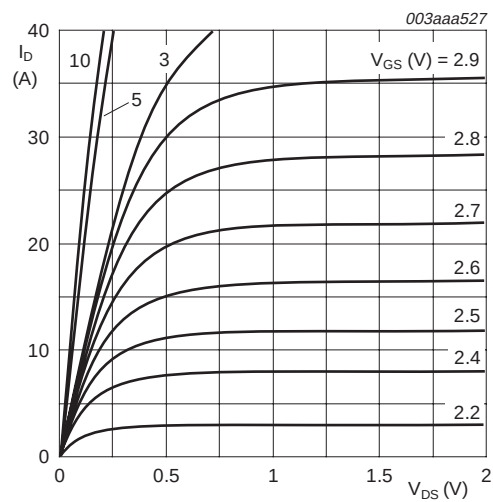


## 6. Characteristics

**Table 5: Characteristics**

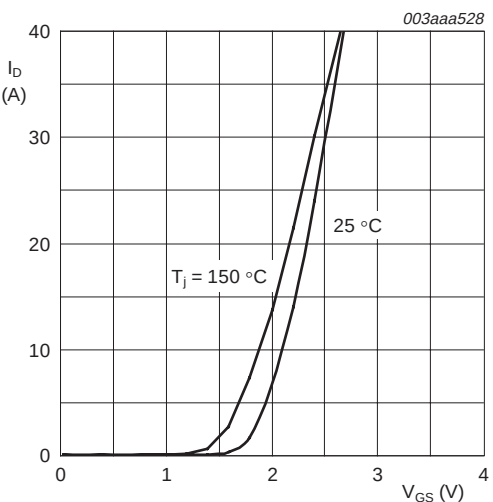
$T_j = 25\text{ °C}$  unless otherwise specified.

| Symbol                  | Parameter                            | Conditions                                                                                         | Min | Typ  | Max | Unit |
|-------------------------|--------------------------------------|----------------------------------------------------------------------------------------------------|-----|------|-----|------|
| Static characteristics  |                                      |                                                                                                    |     |      |     |      |
| V <sub>(BR)DSS</sub>    | drain-source breakdown voltage       | I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V                                                     | 30  | -    | -   | V    |
| V <sub>GS(th)</sub>     | gate-source threshold voltage        | I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; <a href="#">Figure 9</a>                | 1   | 1.5  | 2   | V    |
| I <sub>DSS</sub>        | drain-source leakage current         | V <sub>DS</sub> = 30 V; V <sub>GS</sub> = 0 V                                                      |     |      |     |      |
|                         |                                      | T <sub>j</sub> = 25 °C                                                                             | -   | 0.06 | 1   | μA   |
|                         |                                      | T <sub>j</sub> = 150 °C                                                                            | -   | -    | 500 | μA   |
| I <sub>GSS</sub>        | gate-source leakage current          | V <sub>GS</sub> = ±15 V; V <sub>DS</sub> = 0 V                                                     | -   | 2    | 100 | nA   |
| R <sub>DSon</sub>       | drain-source on-state resistance     | V <sub>GS</sub> = 10 V; I <sub>D</sub> = 15 A; <a href="#">Figure 7</a> and <a href="#">8</a>      |     |      |     |      |
|                         |                                      | T <sub>j</sub> = 25 °C                                                                             | -   | 4.8  | 5.7 | mΩ   |
|                         |                                      | T <sub>j</sub> = 150 °C                                                                            | -   | 8.2  | 9.7 | mΩ   |
|                         |                                      | V <sub>GS</sub> = 5 V; I <sub>D</sub> = 15 A; <a href="#">Figure 7</a> and <a href="#">8</a>       | -   | 5.8  | 7.2 | mΩ   |
| Dynamic characteristics |                                      |                                                                                                    |     |      |     |      |
| Q <sub>g(tot)</sub>     | total gate charge                    | I <sub>D</sub> = 25 A; V <sub>DS</sub> = 10 V; V <sub>GS</sub> = 5 V;<br><a href="#">Figure 13</a> | -   | 23.5 | -   | nC   |
| Q <sub>gs</sub>         | gate-source charge                   |                                                                                                    | -   | 5.8  | -   | nC   |
| Q <sub>gd</sub>         | gate-drain (Miller) charge           |                                                                                                    | -   | 6.5  | -   | nC   |
| C <sub>iss</sub>        | input capacitance                    | V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 10 V; f = 1 MHz;<br><a href="#">Figure 11</a>             | -   | 1972 | -   | pF   |
| C <sub>oss</sub>        | output capacitance                   |                                                                                                    | -   | 769  | -   | pF   |
| C <sub>rss</sub>        | reverse transfer capacitance         |                                                                                                    | -   | 304  | -   | pF   |
| t <sub>d(on)</sub>      | turn-on delay time                   | V <sub>DS</sub> = 10 V; I <sub>D</sub> = 25 A;                                                     | -   | 22   | -   | ns   |
| t <sub>r</sub>          | rise time                            | V <sub>GS</sub> = 5 V; R <sub>G</sub> = 4.7 Ω                                                      | -   | 40   | -   | ns   |
| t <sub>d(off)</sub>     | turn-off delay time                  |                                                                                                    | -   | 48   | -   | ns   |
| t <sub>f</sub>          | fall time                            |                                                                                                    | -   | 18   | -   | ns   |
| Source-drain diode      |                                      |                                                                                                    |     |      |     |      |
| V <sub>SD</sub>         | source-drain (diode forward) voltage | I <sub>S</sub> = 15 A; V <sub>GS</sub> = 0 V; <a href="#">Figure 12</a>                            | -   | 0.85 | 1.2 | V    |
| t <sub>rr</sub>         | reverse recovery time                | I <sub>S</sub> = 20 A; dI <sub>S</sub> /dt = −100 A/μs; V <sub>GS</sub> = 0 V                      | -   | 38   | -   | ns   |



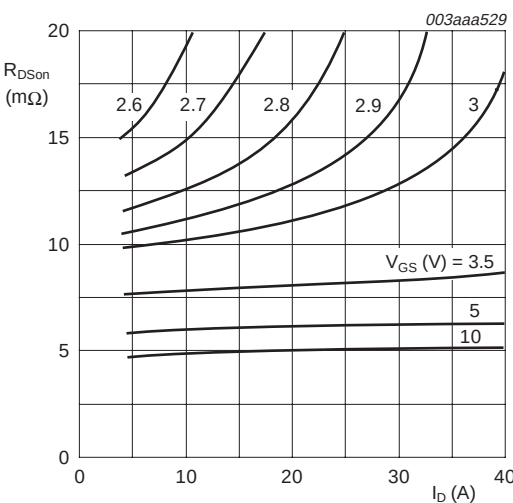
$T_j = 25^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



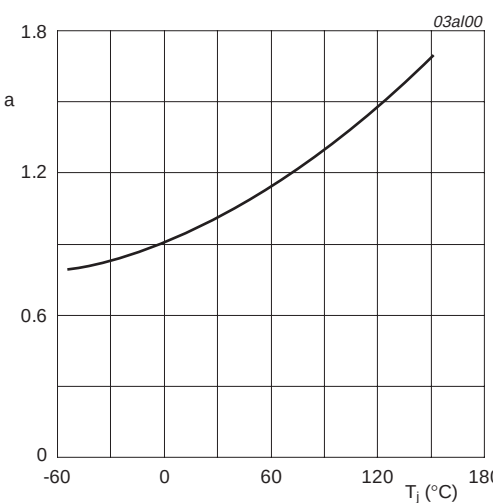
$T_j = 25^\circ\text{C}$  and  $150^\circ\text{C}$ ;  $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



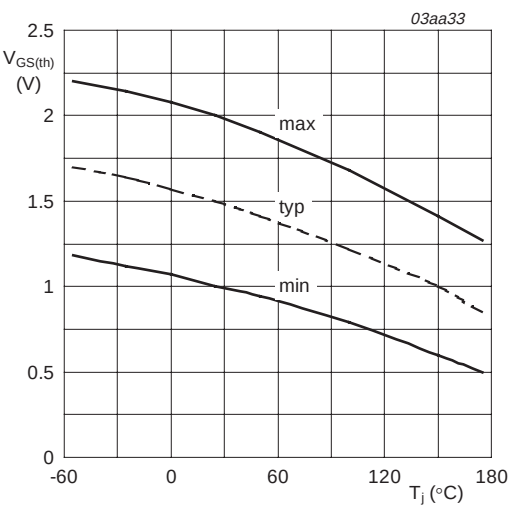
$T_j = 25^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



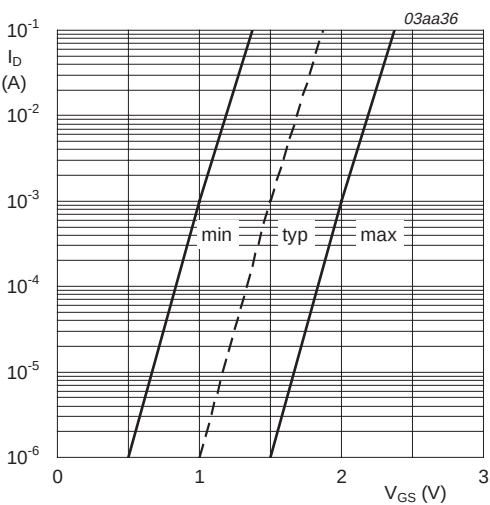
$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



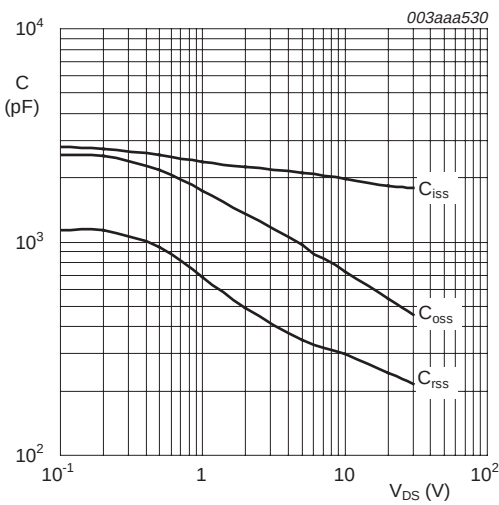
$I_D = 1\text{ mA}$ ;  $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



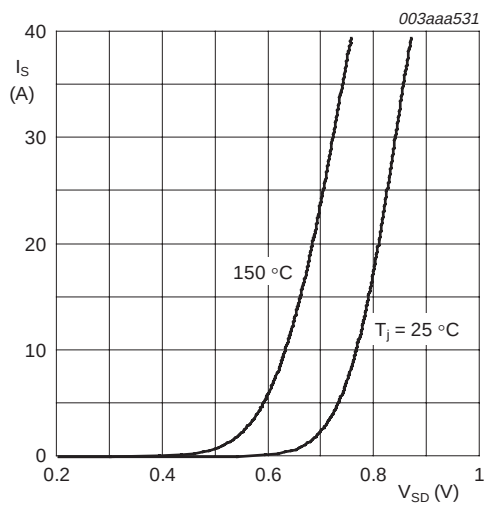
$T_j = 25\text{ °C}$ ;  $V_{DS} = 5\text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



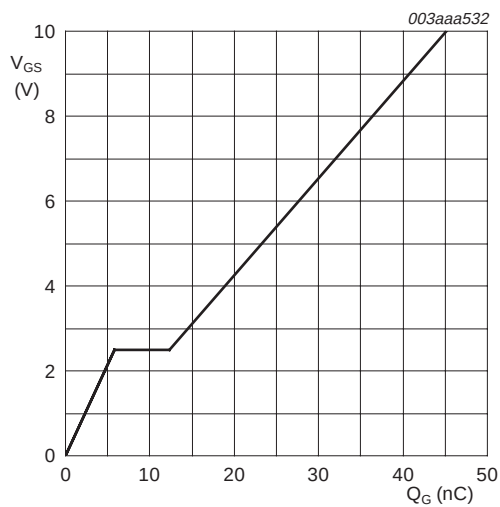
$V_{GS} = 0\text{ V}$ ;  $f = 1\text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



Tj = 25 °C and 150 °C; VGS = 0 V

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



ID = 25 A; VDD = 10 V

Fig 13. Gate-source voltage as a function of gate charge; typical values.



7. Package outline

Plastic single-ended surface mounted package (LPAK); 4 leads

SOT669

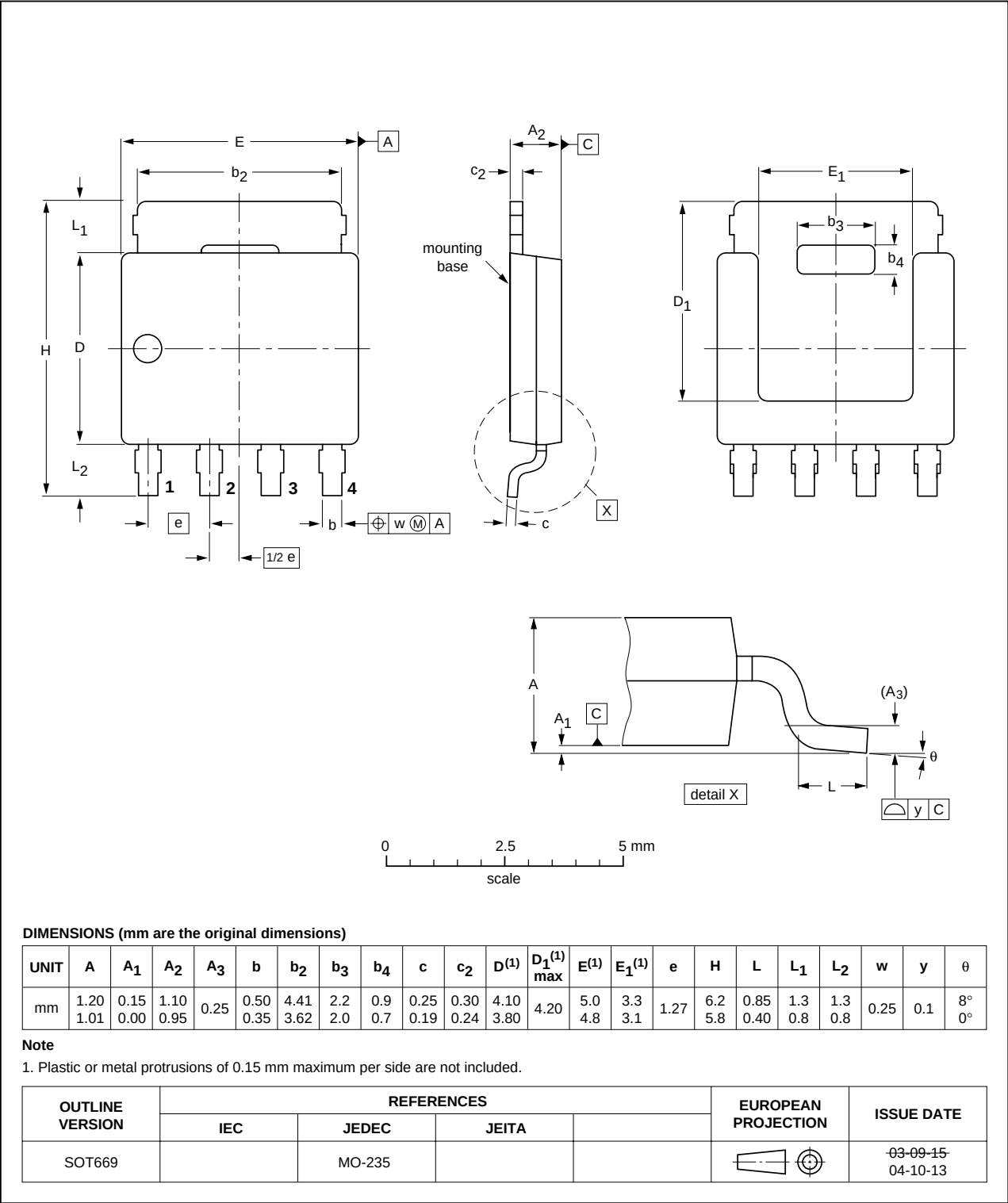


Fig 14. SOT669 (LPAK) package outline.

8. Revision history

Table 6: Revision history

| Document ID    | Release date                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | Data sheet status      | Change notice | Doc. number    | Supersedes |
|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------|---------------|----------------|------------|
| PH4530L_2      | 20050126                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | Product data sheet     | -             | 9397 750 14031 | PH4530L_1  |
| Modifications: | <ul style="list-style-type: none"><li>• <a href="#">Section 1.4 "Quick reference data"</a> <math>I_D</math> and <math>R_{DSon}</math> values updated</li><li>• <a href="#">Table 3 "Limiting values"</a> <math>I_D</math> and <math>I_{DM}</math> values updated</li><li>• <a href="#">Figure 3</a>, <a href="#">Figure 6</a>, <a href="#">Figure 11</a> and <a href="#">Figure 13</a> updated</li><li>• <a href="#">Table 5 "Characteristics"</a> <math>R_{DSon}</math>, <math>Q_{g(tot)}</math>, <math>Q_{gs}</math>, <math>Q_{gd}</math>, <math>C_{iss}</math>, <math>C_{oss}</math> and <math>C_{rss}</math> values updated.</li></ul> |                        |               |                |            |
| PH4530L_1      | 20040304                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | Preliminary data sheet | -             | 9397 750 12813 | -          |

## 9. Data sheet status

| Level | Data sheet status <sup>[1]</sup> | Product status <sup>[2] [3]</sup> | Definition                                                                                                                                                                                                                                                                                     |
|-------|----------------------------------|-----------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| I     | Objective data                   | Development                       | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.                                                                                                    |
| II    | Preliminary data                 | Qualification                     | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.             |
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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