# Frequency Multiplying, Peak Reducing EMI Solution

## Features

- **Cypress PREMIS™ family offering**
- **Generates an EMI optimized clocking signal at the output**
- **Selectable frequency range and multiplication factor**
- **Single 1.25%, 2.5%, 5%, or 10%, down or center spread output**
- **Integrated loop filter components**
- **Operates with a 3.3V or 5V supply**
- **Low power CMOS design**
- **Higher drive strength, higher frequency support than W530**
- **Available in 20-pin SSOP**

## Key Specifications

Supply Voltages: .....$V_{DD}$ = 3.3V ± 0.3V or $V_{DD}$ = 5V ± 10%

Frequency Range: .....13 MHz ≤ $F_{out}$ ≤ 166 MHz

Cycle to Cycle Jitter: ..... 250 ps (max.)

Output Duty Cycle: ..... 40/60% (worst case)

**Table 1. Output Frequency Range Selection**

| OR2 | OR1 | Output Range (Multiplication Factor Selection) |
|---|---|---|
| 0 | 0 | reserved |
| 0 | 1 | 13 MHz ≤ $F_{OUT}$ ≤ 30 MHz |
| 1 | 0 | 25 MHz ≤ $F_{OUT}$ ≤ 60 MHz |
| 1 | 1 | 50 MHz ≤ $F_{OUT}$ ≤ 166 MHz |

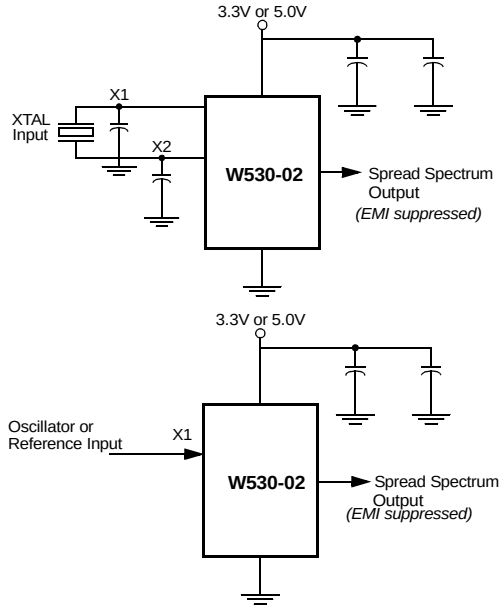
**Table 2. Modulation Width Selection**

| MW2 | MW1 | MW0 | Output |
|---|---|---|---|
| 0 | 0 | 0 | $F_{in} \geq F_{out} \geq F_{in} - 1.25\%$ |
| 0 | 0 | 1 | $F_{avg} + 0.625\% \geq F_{out} \geq F_{avg} - 0.625\%$ |
| 0 | 1 | 0 | $F_{in} \geq F_{out} \geq F_{in} - 2.5\%$ |
| 0 | 1 | 1 | $F_{avg} + 1.25\% \geq F_{out} \geq F_{avg} - 1.25\%$ |
| 1 | 0 | 0 | $F_{in} \geq F_{out} \geq F_{in} - 5\%$ |
| 1 | 0 | 1 | $F_{avg} + 2.5\% \geq F_{out} \geq F_{avg} - 2.5\%$ |
| 1 | 1 | 0 | $F_{in} \geq F_{out} \geq F_{in} - 10\%$ |
| 1 | 1 | 1 | $F_{avg} + 5\% \geq F_{out} \geq F_{avg} - 5\%$ |

**Table 3. Input Frequency Range Selection**

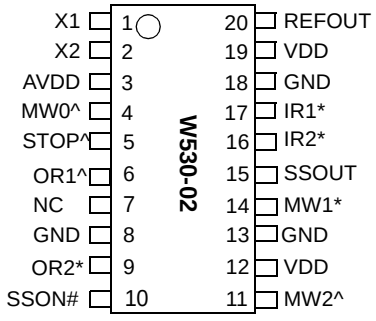
| IR2 | IR1 | Input Range |
|---|---|---|
| 0 | 0 | reserved |
| 0 | 1 | 13 MHz ≤ $F_{IN}$ ≤ 30 MHz |
| 1 | 0 | 25 MHz ≤ $F_{IN}$ ≤ 60 MHz |
| 1 | 1 | 50 MHz ≤ $F_{IN}$ ≤ 166 MHz |

## Simplified Block Diagram




## Pin Configuration[1]

**SSOP**




**Note:**

1. Pins that are marked with [*] have internal pull-up resistors. Pins that are marked with [^] have internal pull-down resistors.

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## Pin Definitions

| Pin Name | Pin No. | Pin Type | Pin Description |
|---|---|---|---|
| SSOUT | 15 | O | ***Output Modulated Frequency***: Frequency modulated signal. Frequency of the output is selected as shown in *Table 1*. |
| REFOUT | 20 | O | ***Non-Modulated Output:*** This pin provides a copy of the reference frequency. This output will not have the Spread Spectrum feature regardless of the state of logic input SSON#. |
| CLKIN or X1 | 1 | I | ***Crystal Connection or External Reference Frequency Input:*** This pin has dual functions. It may either be connected to an external crystal, or to an external reference clock. |
| NC or X2 | 2 | I | ***Crystal Connection:*** Input connection for an external crystal. If using an external reference signal, this pin must be left unconnected. |
| SSON# | 10 | I | ***Spread Spectrum Control (Active LOW):*** Asserting this signal (active LOW) turns the internal modulation waveform on. This pin has an internal pull-down resistor. |
| MW0:2 | 4, 14, 11 | I | ***Modulation Width Selection:*** When the Spread Spectrum feature is turned on, these pins are used to select the amount of variation and peak EMI reduction that is desired on the output signal (see *Table 2*). MW0: DOWN, MW1: UP, MW2: DOWN. |
| IR1:2 | 17,16 | I | ***Reference Frequency Selector:*** The logic level provided at this input indicates to the internal logic what range the reference frequency is in and determines the factor by which the device multiplies the input frequency. Refer to *Table 3*. These pins have internal pull-up resistors. |
| NC | 7 | NC | ***No Connection:*** Leave this pin unconnected. |
| STOP | 5 | I | ***Output Disable:*** When pulled HIGH, stops all outputs at logic low voltage level. This pin has an internal pull-down. |
| OR1:2 | 6,9 | I | ***Output Frequency Selection Bits:*** These pins select the frequency of operation for the output. Refer to *Table 1*. OR1: DOWN, OR2: UP. |
| VDD | 3, 12, 19 | P | ***Power Connection:*** Connected to 3.3V or 5V power supply. |
| GND | 8, 13, 18 | G | ***Ground Connection:*** Connect all ground pins to the common ground plane. |

## Overview

The W530-02 product is one of a series of devices in the Cypress PREMIS family. The PREMIS family incorporates the latest advances in PLL spread spectrum frequency synthesizer techniques. By frequency modulating the output with a low frequency carrier, peak EMI is greatly reduced. Use of this technology allows systems to pass increasingly difficult EMI testing without resorting to costly shielding or redesign.

In a system, not only is EMI reduced in the various clock lines, but also in all signals which are synchronized to the clock. Therefore, the benefits of using this technology increase with the number of address and data lines in the system. The Simplified Block Diagram on page 1 shows a simple implementation.

The W530-02 also allows for frequency multiplication in order to determine the relationship between the input and output frequencies. Simply compare the min. frequency of the input and output ranges selected (use 12.5 instead of 13 for this calculation, though). The multiplication options are: 0.25, 0.5,1.0, 2.0 and 4.0.

## Functional Description

The W530-02 uses a phase-locked loop (PLL) to frequency modulate an input clock. The result is an output clock whose frequency is slowly swept over a narrow band near the input signal. The basic circuit topology is shown in *Figure 1*. The input reference signal is divided by Q and fed to the phase detector. A signal from the VCO is divided by P and fed back to the phase detector also. The PLL will force the frequency of the VCO output signal to change until the divided output signal and the divided reference signal match at the phase detector input. The output frequency is then equal to the ratio of P/Q times the reference frequency. The unique feature of the Spread Spectrum Frequency Timing Generator is that a modulating waveform is superimposed at the input to the VCO. This causes the VCO output to be slowly swept across a predetermined frequency band.

Because the modulating frequency is typically 1000 times slower than the fundamental clock, the spread spectrum process has little impact on system performance.

## Frequency Selection With SSFTG

In Spread Spectrum Frequency Timing Generation, EMI reduction depends on the shape, modulation percentage, and frequency of the modulating waveform. While the shape and frequency of the modulating waveform are fixed for a given frequency, the modulation percentage may be varied.

Using frequency select bits (IR1:2, OR1:2 pins), the frequency range can be set (see *Tables 1* and *3*). Spreading percentage is set with pins MW0:2 as shown in *Table 2*.

A larger spreading percentage improves EMI reduction. However, large spread percentages may either exceed system maximum frequency ratings or lower the average frequency to a point where performance is affected. For these reasons, spreading percentages between 0.5% and 2.5% are most common.

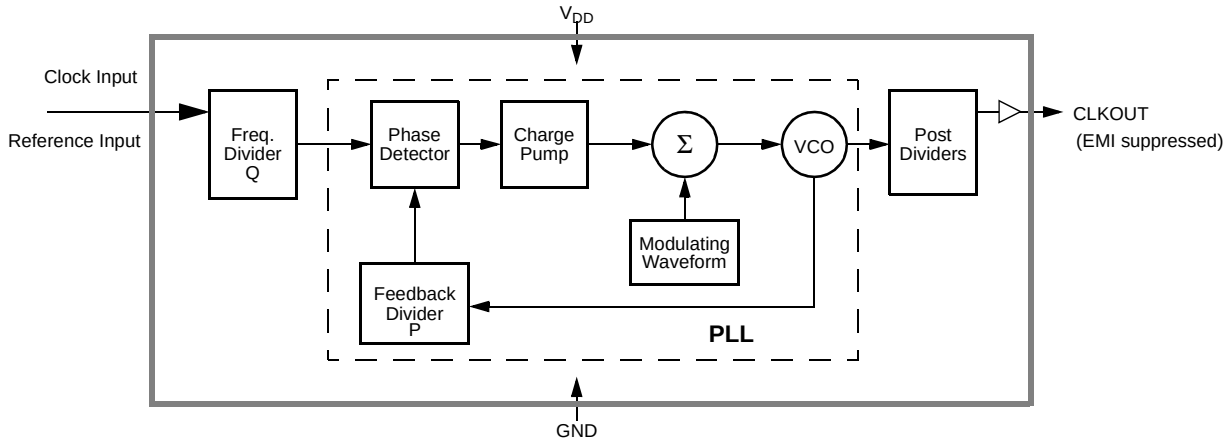



**Figure 1. Conceptual Block Diagram**

## Spread Spectrum Frequency Timing Generation

The benefits of using Spread Spectrum Frequency Timing Generation are depicted in *Figure 2*. An EMI emission profile of a clock harmonic is shown.

Contrast the typical clock EMI with the Cypress Spread Spectrum Frequency Timing Generation EMI. Notice the spike in the typical clock. This spike can make systems fail quasi-peak EMI testing. The FCC and other regulatory agencies test for peak emissions. With spread spectrum enabled, the peak energy is much lower (at least 8 dB) because the energy is spread out across a wider bandwidth.

## Modulating Waveform

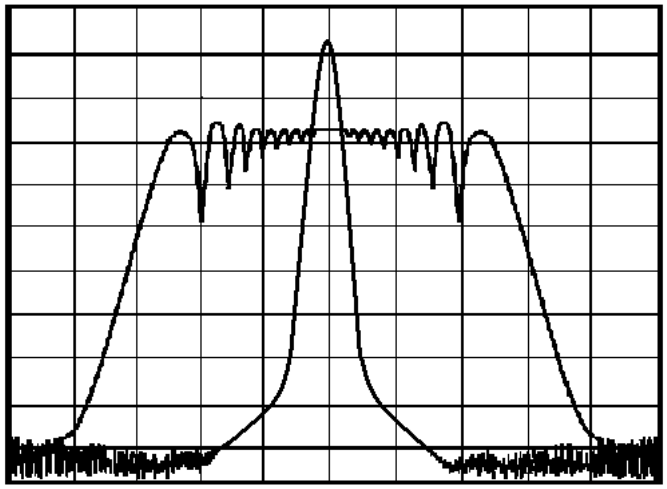
The shape of the modulating waveform is critical to EMI reduction. The modulation scheme used to accomplish the maximum reduction in EMI is shown in *Figure 3*. The period of the modulation is shown as a percentage of the period length along the X axis. The amount that the frequency is varied is shown along the Y axis, also shown as a percentage of the total frequency spread.

Cypress frequency selection tables express the modulation percentage in two ways. The first method displays the spreading frequency band as a percent of the programmed average output frequency, symmetric about the programmed average frequency. This method is always shown using the expression $f_{Center} \pm X_{MOD}\%$ in the frequency spread selection table.

The second approach is to specify the maximum operating frequency and the spreading band as a percentage of this frequency. The output signal is swept from the lower edge of the band to the maximum frequency. The expression for this approach is $f_{MAX} - X_{MOD}\%$. Whenever this expression is used, Cypress has taken care to ensure that $f_{MAX}$ will never be exceeded. This is important in applications where the clock drives components with tight maximum clock speed specifications.

## SSON# Pin

An internal pull-down resistor defaults the chip into spread spectrum mode. When the SSON# pin is asserted (active LOW) the spreading feature is enabled. Spreading feature is disabled when SSON# is set HIGH ($V_{DD}$).



Frequency Span (MHz)
Center Spread

**Figure 2. Typical Clock and SSFTG Comparison**

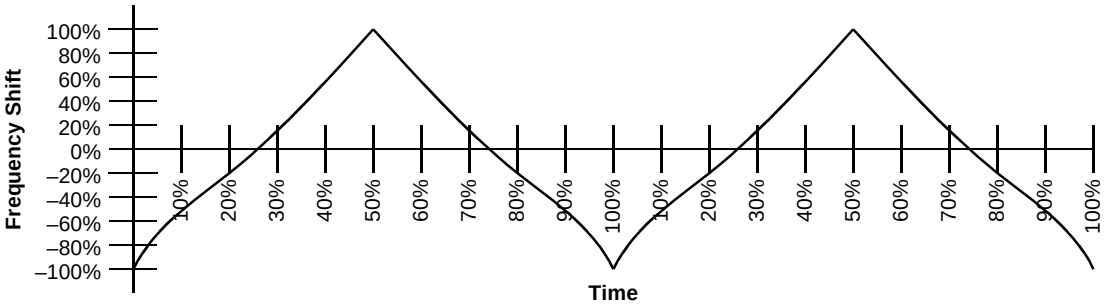



**Figure 3. Modulation Waveform Profile**

## Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

| Parameter | Description | Rating | Unit |
|---|---|---|---|
| $V_{DD}$, $V_{IN}$ | Voltage on any Pin with Respect to GND | –0.5 to +7.0 | V |
| $T_{STG}$ | Storage Temperature | –65 to +150 | °C |
| $T_A$ | Operating Temperature | 0 to +70 | °C |
| $T_B$ | Ambient Temperature under Bias | –55 to +125 | °C |
| $P_D$ | Power Dissipation | 0.5 | W |

## DC Electrical Characteristics: $0°C < T_A < 70°C$, $V_{DD} = 3.3V \pm 0.3V$

| Parameter | Description | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Supply Current | | | 18 | 32 | mA |
| $t_{ON}$ | Power-Up Time | First locked clock cycle after Power Good | | | 5 | ms |
| $V_{IL}$ | Input Low Voltage | | | | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | 2.4 | | | V |
| $V_{OL}$ | Output Low Voltage | | | | 0.4 | V |
| $V_{OH}$ | Output High Voltage | | 2.4 | | | V |
| $I_{IL}$ | Input Low Current | Note 2 | | | –100 | µA |
| $I_{IH}$ | Input High Current | Note 2 | | | 10 | µA |
| $I_{OL}$ | Output Low Current | @ 0.4V, $V_{DD} = 3.3V$ | | 15 | | mA |
| $I_{OH}$ | Output High Current | @ 2.4V, $V_{DD} = 3.3V$ | | 15 | | mA |
| $C_I$ | Input Capacitance | | | | 7 | pF |
| $R_P$ | Input Pull-Up Resistor | | | 80 | | kΩ |
| $Z_{OUT}$ | Clock Output Impedance | | | 25 | | Ω |

**Note:**
2. Inputs OR1:2 and IR1:2 have a pull-up resistor, Input SSON# has a pull-down resistor.

## DC Electrical Characteristics: $0°C < T_A < 70°C$, $V_{DD} = 5V \pm 10\%$

| Parameter | Description | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Supply Current | | | 30 | 50 | mA |
| $t_{ON}$ | Power-Up Time | First locked clock cycle after Power Good | | | 5 | ms |
| $V_{IL}$ | Input Low Voltage | | | | $0.15V_{DD}$ | V |
| $V_{IH}$ | Input High Voltage | | $0.7V_{DD}$ | | | V |
| $V_{OL}$ | Output Low Voltage | | | | 0.4 | V |
| $V_{OH}$ | Output High Voltage | | 2.4 | | | V |
| $I_{IL}$ | Input Low Current | Note 2 | | | –100 | µA |
| $I_{IH}$ | Input High Current | Note 2 | | | 10 | µA |
| $I_{OL}$ | Output Low Current | @ 0.4V, $V_{DD} = 5V$ | | 24 | | mA |
| $I_{OH}$ | Output High Current | @ 2.4V, $V_{DD} = 5V$ | | 24 | | mA |
| $C_I$ | Input Capacitance | | | | 7 | pF |
| $R_P$ | Input Pull-Up Resistor | | | 80 | | kΩ |
| $Z_{OUT}$ | Clock Output Impedance | | | 25 | | Ω |

## AC Electrical Characteristics: $T_A = 0°C$ to $+70°C$, $V_{DD} = 3.3V \pm 0.3V$

| Parameter | Description | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $f_{IN}$ | Input Frequency | Input Clock | 14 | | 166 | MHz |
| $f_{OUT}$ | Output Frequency | Spread Off | 13 | | 166 | MHz |
| $t_R$ | Output Rise Time | $V_{DD}$, 15-pF load, 0.8V–2.4V | | 2 | 5 | ns |
| $t_F$ | Output Fall Time | $V_{DD}$, 15-pF load, 2.4V–0.8V | | 2 | 5 | ns |
| $t_{OD}$ | Output Duty Cycle | 15-pF load | 40 | | 60 | % |
| $t_{ID}$ | Input Duty Cycle | | 40 | | 60 | % |
| $t_{JCYC}$ | Jitter, Cycle-to-Cycle | | | 250 | 300 | ps |

## AC Electrical Characteristics: $T_A = 0°C$ to $+70°C$, $V_{DD} = 5V \pm 10\%$

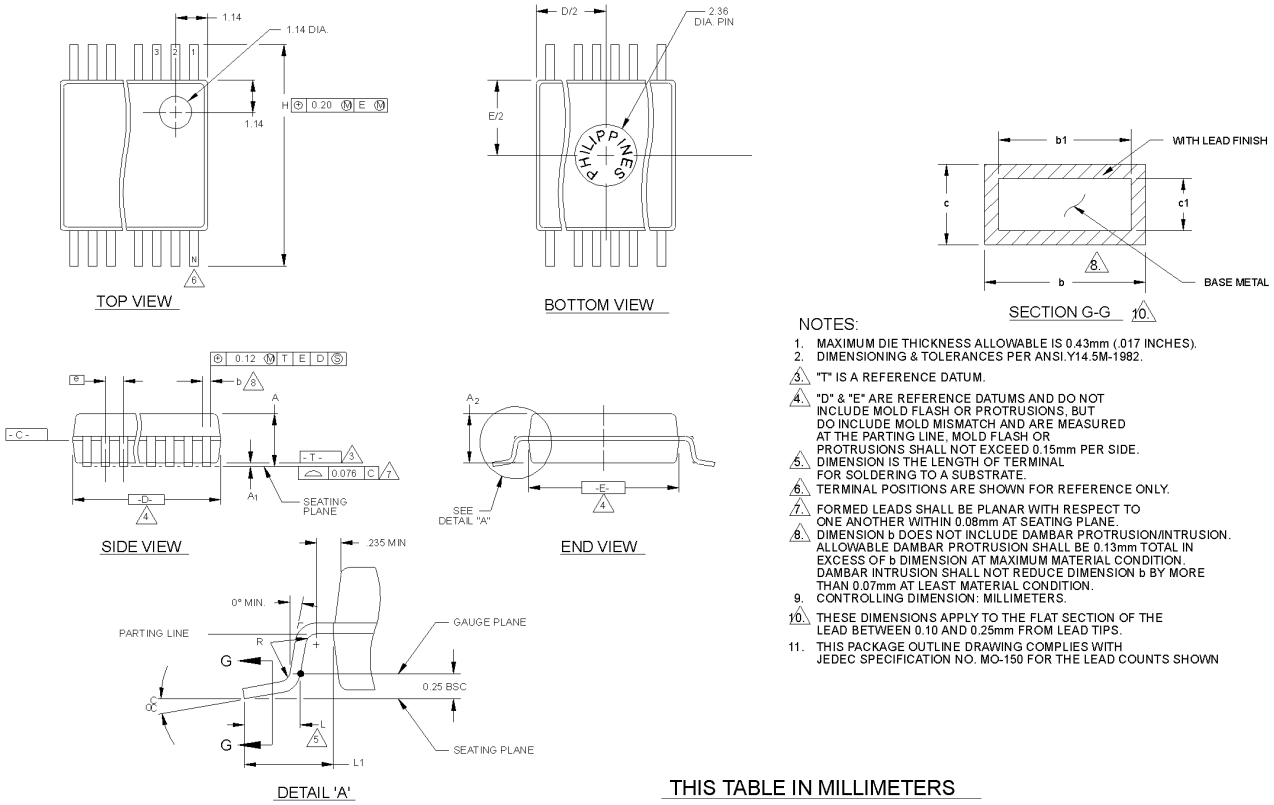
| Parameter | Description | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $f_{IN}$ | Input Frequency | Input Clock | 14 | | 166 | MHz |
| $f_{OUT}$ | Output Frequency | Spread Off | 13 | | 166 | MHz |
| $t_R$ | Output Rise Time | $V_{DD}$, 15-pF load, 0.8V–2.4V | | 2 | 5 | ns |
| $t_F$ | Output Fall Time | $V_{DD}$, 15-pF load, 2.4V–0.8V | | 2 | 5 | ns |
| $t_{OD}$ | Output Duty Cycle | 15-pF load | 45 | | 55 | % |
| $t_{ID}$ | Input Duty Cycle | | 40 | | 60 | % |
| $t_{JCYC}$ | Jitter, Cycle-to-Cycle | | | 100 | 200 | ps |

## Ordering Information

| Ordering Code | Package Name | Package Type |
|---|---|---|
| W530-02 | H | 20-Pin Plastic SSOP (209-mil) |

## Package Diagram

**20-Pin Small Shrink Outline Package (SSOP, 209-mil)**




NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS 0.43mm (.017 INCHES).
2. DIMENSIONING & TOLERANCES PER ANSI.Y14.5M-1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DO INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE PARTING LINE, MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSION IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
7. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.08mm AT SEATING PLANE.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13mm TOTAL IN EXCESS OF b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION b BY MORE THAN 0.07mm AT LEAST MATERIAL CONDITION.
9. CONTROLLING DIMENSION: MILLIMETERS.
10. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 AND 0.25mm FROM LEAD TIPS.
11. THIS PACKAGE OUTLINE DRAWING COMPLIES WITH JEDEC SPECIFICATION NO. MO-150 FOR THE LEAD COUNTS SHOWN

THIS TABLE IN MILLIMETERS

| SYMBOL | COMMON DIMENSIONS | | | NOTE | NOTE | 4 | | | 6 |
|---|---|---|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | | VARIATIONS | D MIN. | D NOM. | D MAX. | N |
| A | 1.73 | 1.86 | 1.99 | | AA | 6.07 | 6.20 | 6.33 | 14 |
| $A_1$ | 0.05 | 0.13 | 0.21 | | AB | 6.07 | 6.20 | 6.33 | 16 |
| $A_2$ | 1.68 | 1.73 | 1.78 | | AC | 7.07 | 7.20 | 7.33 | 20 |
| b | 0.25 | - | 0.38 | 8,10 | AD | 8.07 | 8.20 | 8.33 | 24 |
| b1 | 0.25 | 0.30 | 0.33 | 10 | AE | 10.07 | 10.20 | 10.33 | 28 |
| c | 0.09 | - | 0.20 | 10 | AF | 10.07 | 10.20 | 10.33 | 30 |
| c1 | 0.09 | 0.15 | 0.16 | 10 | | | | | |
| D | SEE VARIATIONS | | | 4 | | | | | |
| E | 5.20 | 5.30 | 5.38 | 4 | | | | | |
| e | 0.65 BSC | | | | | | | | |
| H | 7.65 | 7.80 | 7.90 | | | | | | |
| L | 0.63 | 0.75 | 0.95 | 5 | | | | | |
| L1 | 1.25 REF. | | | | | | | | |
| N | SEE VARIATIONS | | | 6 | | | | | |
| cc | 0° | 4° | 8° | | | | | | |
| R | 0.09 | 0.15 | | | | | | | |

VARIATION AF
IS DESIGNED BUT NOT TOOLED

THIS TABLE IN INCHES

| SYMBOL | COMMON DIMENSIONS | | | NOTE | NOTE | 4 | | | 6 |
|---|---|---|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | | VARIATIONS | D MIN. | D NOM. | D MAX. | N |
| A | .068 | .073 | .078 | | AA | .239 | .244 | .249 | 14 |
| $A_1$ | .002 | .005 | .008 | | AB | .239 | .244 | .249 | 16 |
| $A_2$ | .066 | .068 | .070 | | AC | .278 | .284 | .289 | 20 |
| b | .010 | - | .015 | 8,10 | AD | .318 | .323 | .328 | 24 |
| b1 | .010 | .012 | .013 | 10 | AE | .397 | .402 | .407 | 28 |
| c | .004 | - | .008 | 10 | AF | .397 | .402 | .407 | 30 |
| c1 | .004 | .006 | .006 | 10 | | | | | |
| D | SEE VARIATIONS | | | 4 | | | | | |
| E | .205 | .209 | .212 | 4 | | | | | |
| e | .0256 BSC | | | | | | | | |
| H | .301 | .307 | .311 | | | | | | |
| L | .025 | .030 | .037 | 5 | | | | | |
| L1 | .049 REF. | | | | | | | | |
| N | SEE VARIATIONS | | | 6 | | | | | |
| cc | 0° | 4° | 8° | | | | | | |
| R | .004 | .006 | | | | | | | |

| Document Title: W530-02 Frequency Multiplying, Peak Reducing EMI Solution<br>Document Number: 38-07190 | | | | |
|---|---|---|---|---|
| **REV.** | **ECN NO.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 110591 | 01/07/02 | DSG | Change from Spec number: 38-01062 to 38-07190 |