

Features

- Single-pin or complementary CMOS logic control inputs
- +3.0V power supply needed for single-pin control mode
- Low insertion loss: 0.7 dB at 1.0 GHz, 0.9 dB at 2.0 GHz
- Isolation of 32 dB at 1.0 GHz, 23 dB at 2.0 GHz
- Typical input 1 dB compression point of +25 dBm

Product Description

The PE4239 UltraCMOS® RF switch is designed to cover a broad range of applications from DC through 3.0 GHz. This reflective switch integrates on-board CMOS control logic with a low voltage CMOS-compatible control interface, and can be controlled using either single-pin or complementary control inputs. Using a nominal +3V power supply voltage, a typical input 1 dB compression point of +25 dBm can be achieved.

The PE4239 UltraCMOS RF switch is manufactured on pSemi's UltraCMOS process, a patented variation of silicon-on-insulator (SOI) technology.

Figure 1. Functional Diagram

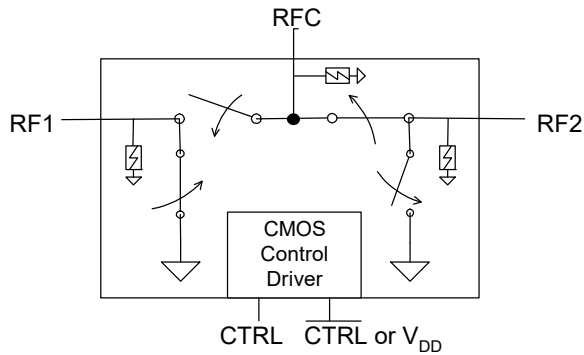


Figure 2. Package Type SC-70

6-lead SC-70

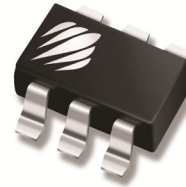


Table 1. Electrical Specifications @ +25 °C, V_{DD} = 3V (Z_S = Z_L = 50Ω)

| Parameter | Conditions | Minimum | Typical | Maximum | Units |
|----------------------------------|--|----------|------------|--------------|------------------|
| Operation Frequency ¹ | | DC | | 3000 | MHz |
| Insertion Loss | 1000 MHz 2000 MHz | | 0.7 0.9 | 0.85 1.05 | dB dB |
| Isolation | 1000 MHz 2000 MHz | 30 21 | 32 23 | | dB dB |
| Return Loss | 1000 MHz 2000 MHz | 18 16 | 20 18 | | dB dB |
| 'ON' Switching Time | 50% CTRL to 0.1 dB of final value, 1 GHz | | 300 | | ns |
| 'OFF' Switching Time | 50% CTRL to 25 dB isolation, 1 GHz | | 200 | | ns |
| Video Feedthrough ² | | | 15 | | mV _{pp} |
| Input 1 dB Compression | 2000 MHz | 23 | 25 | | dBm |
| Input IP3 | 2000 MHz, 14 dBm input power | 43 | 45 | | dBm |

Notes: 1. Device linearity will begin to degrade below 10 MHz.

2. The DC transient at the output of any port of the switch when the control voltage is switched from low to high or high to low in a 50Ω test set-up, measured with 1ns risetime pulses and 500 MHz bandwidth.

Figure 3. Pin Configuration (Top View)

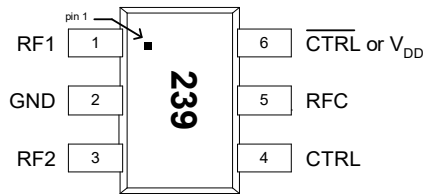


Table 2. Pin Descriptions

| Pin No. | Pin Name | Description |
|---------|-------------------------|--|
| 1 | RF1 | RF1 port (Note 1) |
| 2 | GND | Ground connection. Traces should be physically short and connected to ground plane for best performance. |
| 3 | RF2 | RF2 port (Note 1) |
| 4 | CTRL | Switch control input, CMOS logic level. |
| 5 | RFC | Common RF port for switch (Note 1) |
| 6 | CTRL or V _{DD} | This pin supports two interface options: <i>Single-pin control mode.</i> A nominal 3V supply connection is required. <i>Complementary-pin control mode.</i> A complementary CMOS control signal to CTRL is supplied to this pin. Bypassing on this pin is not required in this mode. |

Note 1: All RF pins must be DC blocked with an external series capacitor or held at 0 V_{DC}.

Table 3. Absolute Maximum Ratings

| Symbol | Parameter/Conditions | Min | Max | Units |
|------------------|--------------------------------|------|-----------------------|-------|
| V _{DD} | Power supply voltage | -0.3 | 4.0 | V |
| V _I | Voltage on any input | -0.3 | V _{DD} + 0.3 | V |
| T _{ST} | Storage temperature range | -65 | 150 | °C |
| T _{OP} | Operating temperature range | -55 | 85 | °C |
| P _{IN} | Input power (50Ω) | | 30 | dBm |
| V _{ESD} | ESD voltage (Human Body Model) | | 1000 | V |

Table 4. DC Electrical Specifications

| Parameter | Min | Typ | Max | Units |
|---|----------------------|-----|----------------------|-------|
| V _{DD} Power Supply Voltage | 2.7 | 3.0 | 3.3 | V |
| I _{DD} Power Supply Current (V _{DD} = 3V, V _{CTRL} = 3V) | | 250 | 500 | nA |
| Control Voltage High | 0.7x V _{DD} | | | V |
| Control Voltage Low | | | 0.3x V _{DD} | V |

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 5. Single-pin Control Logic Truth Table

| Control Voltages | Signal Path |
|--|-------------|
| Pin 6 ($\overline{\text{CTRL}}$ or V_{DD}) = V_{DD} Pin 4 (CTRL) = High | RFC to RF1 |
| Pin 6 ($\overline{\text{CTRL}}$ or V_{DD}) = V_{DD} Pin 4 (CTRL) = Low | RFC to RF2 |

Table 6. Complementary-pin Control Logic Truth Table

| Control Voltages | Signal Path |
|---|-------------|
| Pin 6 ($\overline{\text{CTRL}}$ or V_{DD}) = Low Pin 4 (CTRL) = High | RFC to RF1 |
| Pin 6 ($\overline{\text{CTRL}}$ or V_{DD}) = High Pin 4 (CTRL) = Low | RFC to RF2 |

Control Logic Input

The PE4239 is a versatile RF switch that supports two operating control modes; single-pin control mode and complementary-pin control mode.

Single-pin control mode enables the switch to operate with a single control pin (pin 4) supporting a +3V CMOS logic input, and requires a dedicated +3V power supply connection on pin 6 (V_{DD}). This mode of operation reduces the number of control lines required and simplifies the switch control interface typically derived from a CMOS μ Processor I/O port.

Complementary-pin control mode allows the switch to operate using complementary control pins CTRL and $\overline{\text{CTRL}}$ (pins 4 & 6), that can be directly driven by +3V CMOS logic or a suitable μ Processor I/O port. This enables the PE4239 to be used as a potential alternate source for SPDT RF switch products used in positive control voltage mode and operating within the PE4239 operating limits.

Evaluation Kit

The SPDT switch Evaluation Kit board was designed to ease customer evaluation of the PE4239 SPDT switch. The RF common port is connected through a 50Ω transmission line to the top left SMA connector, J1. Port 1 and Port 2 are connected through 50Ω transmission lines to the top two SMA connectors on the right side of the board, J3 and J2, respectively. A through transmission line connects SMA connectors J4 and J5. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

The board is constructed of a two metal layer FR4 material with a total thickness of 0.031". The bottom layer provides ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 0.0476", trace gaps of 0.030", dielectric thickness of 0.028", metal thickness of 0.0021" and ϵ_r of 4.4.

J6 provides a means for controlling DC and digital inputs to the device. Starting from the lower left pin, the second pin to the right (J6-3) is connected to the device V1 or CTRL input. The fourth pin to the right (J6-7) is connected to the device V2 or CTRL/V_{DD} input.

Figure 4. Evaluation Board Layout

PSemi Specification 101/0083

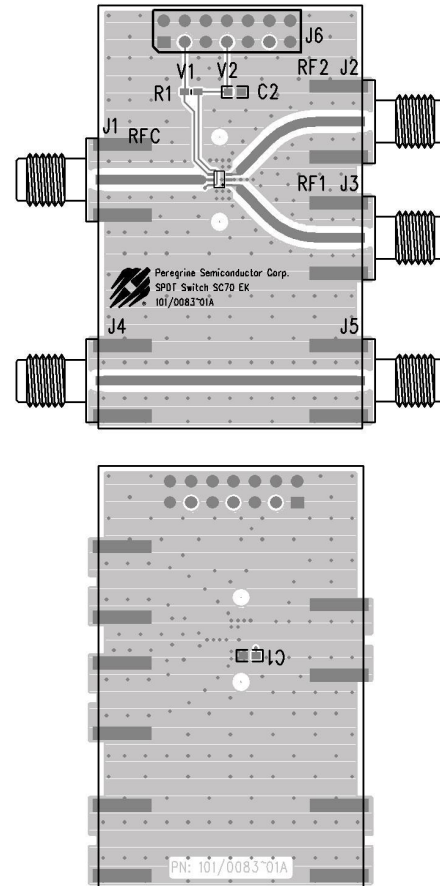
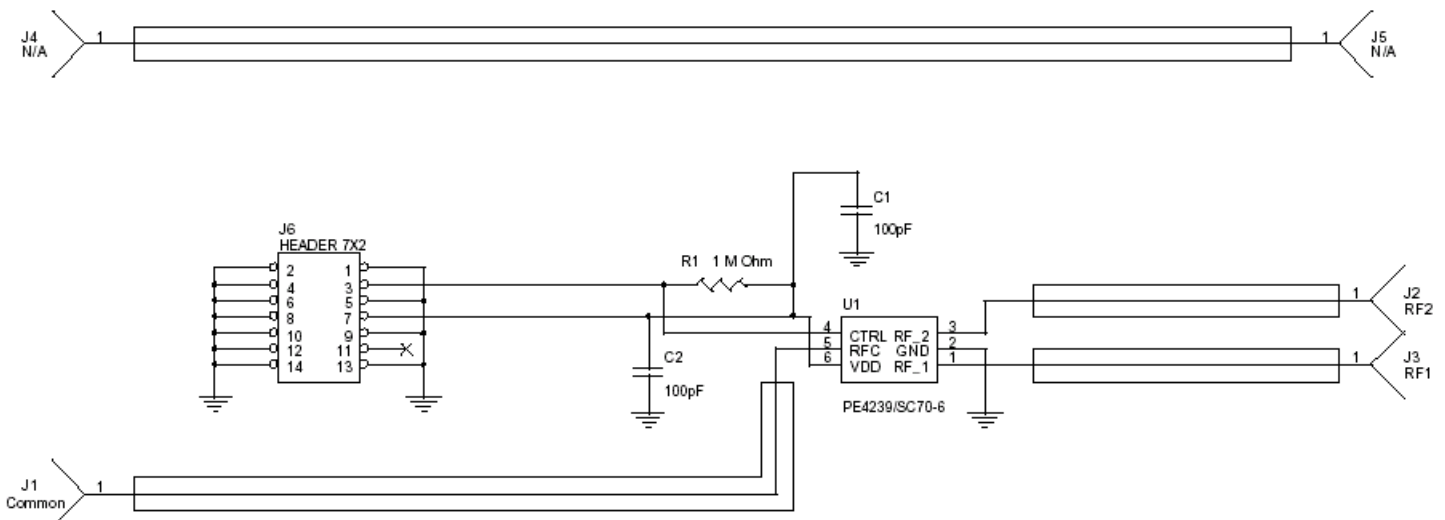


Figure 5. Evaluation Board Schematic

PSemi Specification 102/0104



Typical Performance Data @ -40 °C to 85 °C (Unless otherwise noted)

Figure 6. Insertion Loss – RFC to RF1

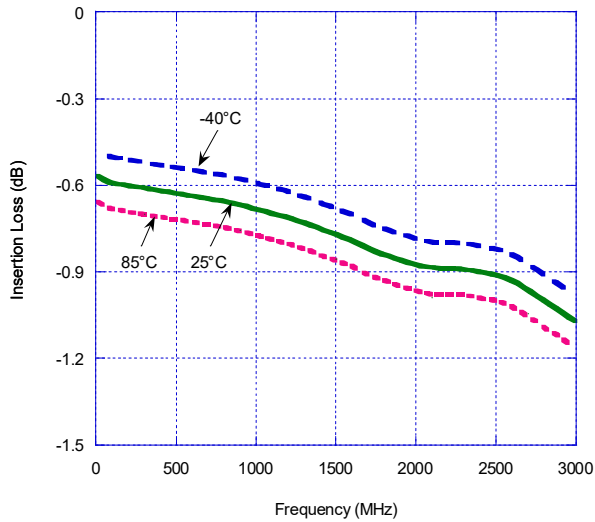


Figure 7. Insertion Loss – RFC to RF2

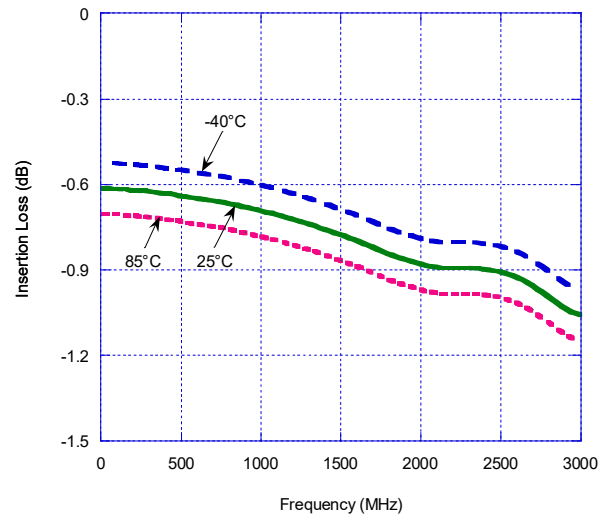


Figure 8. Isolation – RFC to RF1

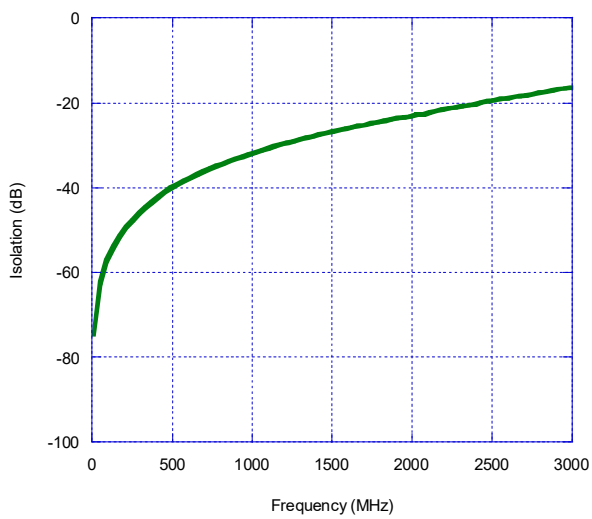
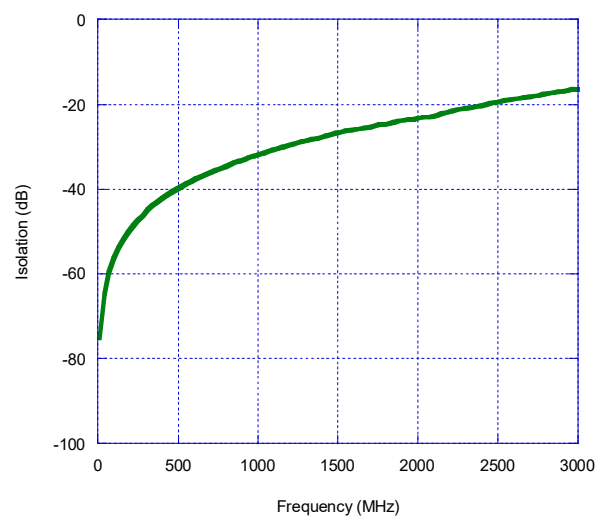


Figure 9. Isolation – RFC to RF2



Typical Performance Data @ -40 °C to 85 °C (Unless otherwise noted)

Figure 10. Isolation – RF1 to RF2, RF2 to RF1

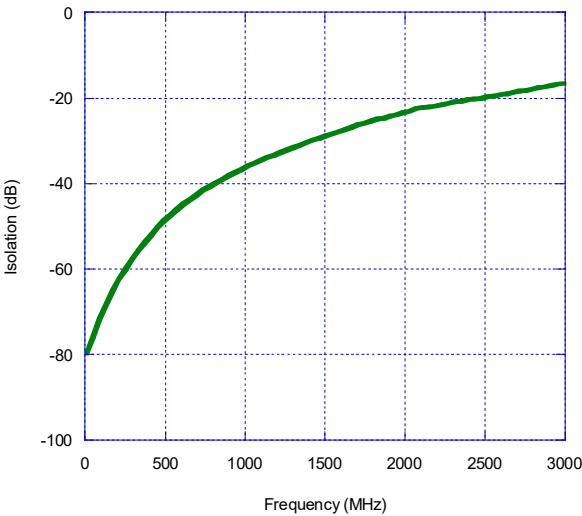


Figure 11. Return Loss – RFC to RF1, RF2

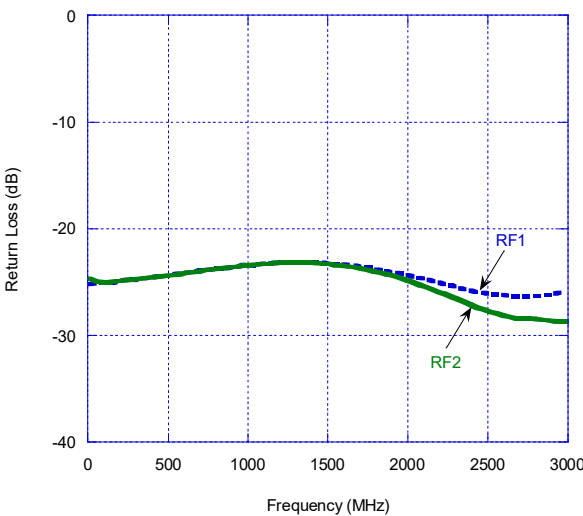


Figure 12. Return Loss – RF1, RF2

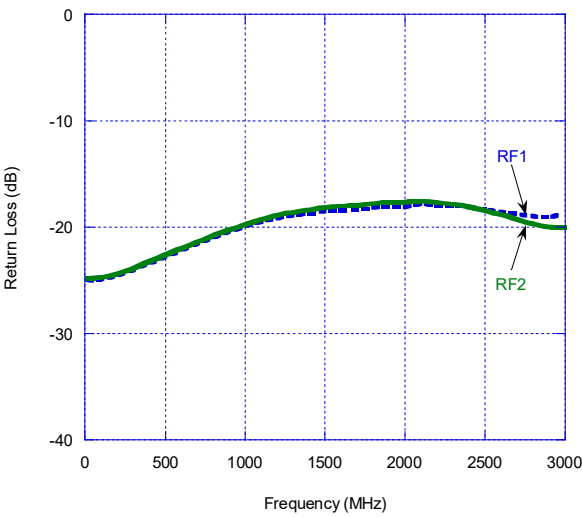


Figure 14. Package Drawing

6-lead SC-70

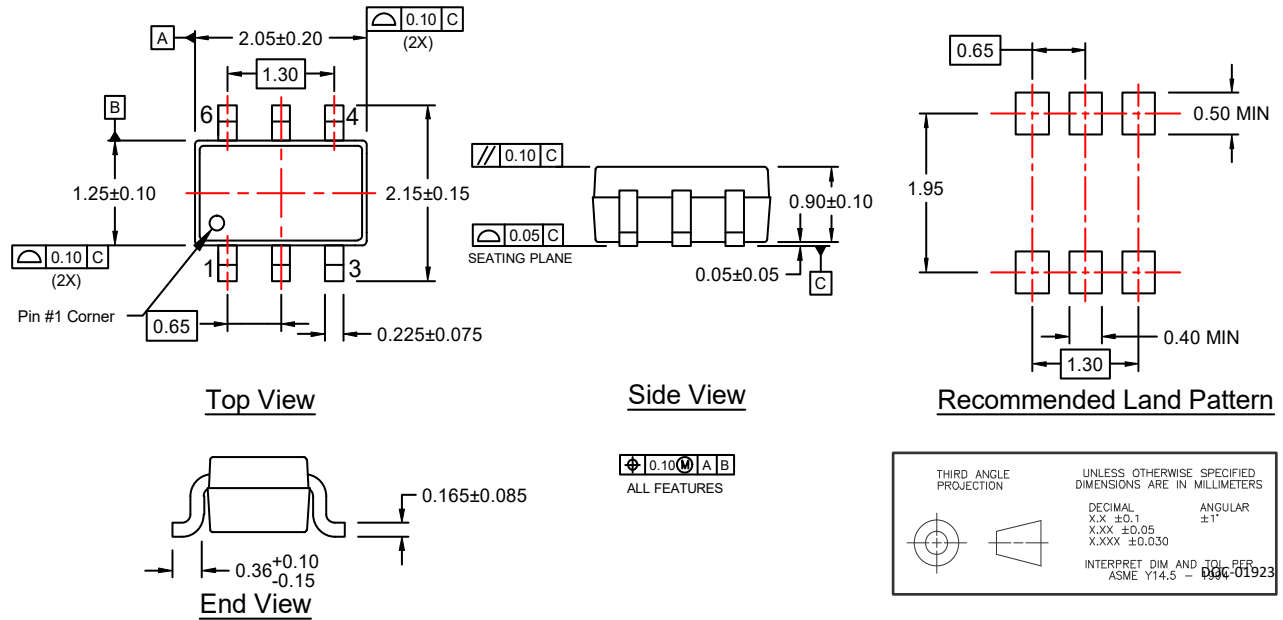


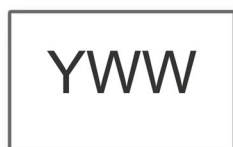
Figure 15. Top-Marking Specification

Top Mark



• = Pin 1 indicator
PPP = Last three digits of product part number (PE4239 = 239)

Bottom Mark



Y = Last digit of assembly year (2022 = 2)
WW = Work week number (01,02,03...52)

Technical drawing of a 6-pin connector. The drawing includes a side view (Section A-A) and a top view. Key dimensions and features are labeled:

- Section A-A:** Shows a cross-section of the connector with dimensions 0.30 ± 0.05 and $R0.3 \text{ MAX}$.
- Top View:** Shows the connector with 6 pins. Dimensions include:
 - 2.0 ± 0.05 (Pin pitch)
 - 4.0 (Overall width)
 - $\varnothing 1.5 +0.1/-0.0$ (Pin diameter)
 - $\varnothing 1.0 \text{ MIN}$ (Pin hole diameter)
 - 1.75 (Pin length)
 - 3.5 ± 0.05 (Pin spacing from center)
 - 8.0 ± 0.3 (Overall length)
 - $R0.5 \text{ TYP}$ (Radius of the connector body)
- Notes:**
 - See Note 1
 - See Note 6
- Labels:** Pin 1, A, A, Ko, Ao, Bo.
- Direction:** Tape Feed Direction (indicated by a dashed arrow).

1. 10 sprocket hole pitch cumulative tolerance $\pm .02$.
2. Camber not to exceed 1mm in 100mm.
3. Material: Black Conductive Advantek Polystyrene.
4. Ao and Bo measured on a plane 0.3mm above the bottom of the pocket
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

$A_o = 2.25 \text{ mm}$
 $B_o = 2.4 \text{ mm}$
 $K_o = 1.2 \text{ mm}$

Table 7. Ordering Information

| Order Code | Description | Package | Shipping Method |
|------------|-----------------------|--------------------|-----------------|
| PE4239A-Z | PE4239 SPDT RF Switch | Green 6-lead SC-70 | 3000 unit / T&R |
| EK4239-01 | PE4239 Evaluation Kit | Evaluation Kit | 1 / Box |

Sales Contact and Information

For sales and contact information please visit www.psemi.com.

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