

N-Channel 20 V (D-S) 175 °C MOSFET

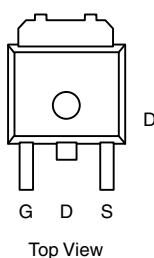
PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^a
20	0.0043 at $V_{GS} = 10$ V	34
	0.006 at $V_{GS} = 4.5$ V	28

FEATURES

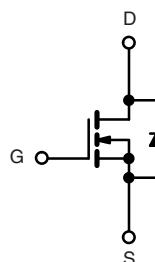
- TrenchFET® Power MOSFET
- 175 °C Junction Temperature
- PWM Optimized for High Efficiency
- Material categorization:
For definitions of compliance please see www.vishay.com/doc?99912


RoHS
COMPLIANT

TO-252



Drain Connected to Tab



Top View

N-Channel MOSFET

Ordering Information:
SUD50N02-04P-E3 (Lead (Pb)-free)

APPLICATIONS

- Synchronous Buck Converter
 - Low-Side
 - Desktop, Servers, Desknote
- Synchronous Rectification
 - POL

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V_{DS}	20	V	
Gate-Source Voltage	V_{GS}	± 20		
Continuous Drain Current ^a	I_D	34 ^a	A	
		50 ^b		
Pulsed Drain Current	I_{DM}	100		
Continuous Source Current (Diode Conduction) ^a	I_S	8.3 ^a		
Avalanche Current ^c	I_{AS}	50		
Avalanche Energy ^c	E_{AS}	125		mJ
Maximum Power Dissipation	P_D	8.3 ^a	W	
		136		
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 175		°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	15	18	°C/W
		40	50	
Maximum Junction-to-Case	R_{thJC}	0.85	1.1	

Notes:

- Surface mounted on FR4 board, $t \leq 10$ s.
- Limited by package.
- Single pulse.

SPECIFICATIONS ($T_J = 25^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ. ^a	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0 \text{ V}$, $I_D = 250 \mu\text{A}$	20			V
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}} = V_{\text{GS}}$, $I_D = 250 \mu\text{A}$	0.8		3.0	
Gate-Body Leakage	I_{GSS}	$V_{\text{DS}} = 0 \text{ V}$, $V_{\text{GS}} = \pm 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}} = 20 \text{ V}$, $V_{\text{GS}} = 0 \text{ V}$		1		μA
		$V_{\text{DS}} = 20 \text{ V}$, $V_{\text{GS}} = 0 \text{ V}$, $T_J = 125^\circ\text{C}$		50		
On-State Drain Current ^b	$I_{\text{D}(\text{on})}$	$V_{\text{DS}} = 5 \text{ V}$, $V_{\text{GS}} = 10 \text{ V}$	50			A
Drain-Source On-State Resistance ^b	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = 10 \text{ V}$, $I_D = 20 \text{ A}$		0.0035	0.0043	Ω
		$V_{\text{GS}} = 10 \text{ V}$, $I_D = 20 \text{ A}$, $T_J = 125^\circ\text{C}$			0.0061	
		$V_{\text{GS}} = 4.5 \text{ V}$, $I_D = 20 \text{ A}$		0.0048	0.006	
Forward Transconductance ^b	g_{fs}	$V_{\text{DS}} = 15 \text{ V}$, $I_D = 20 \text{ A}$	15			S
Dynamic^a						
Input Capacitance	C_{iss}	$V_{\text{GS}} = 0 \text{ V}$, $V_{\text{DS}} = 10 \text{ V}$, $f = 1 \text{ MHz}$		5000		pF
Output Capacitance	C_{oss}			1650		
Reverse Transfer Capacitance	C_{rss}			770		
Gate Resistance	R_g	$f = 1 \text{ MHz}$		1.6		Ω
Total Gate Charge ^c	Q_g	$V_{\text{DS}} = 10 \text{ V}$, $V_{\text{GS}} = 4.5 \text{ V}$, $I_D = 50 \text{ A}$		40	60	nC
Gate-Source Charge ^c	Q_{gs}			14		
Gate-Drain Charge ^c	Q_{gd}			13		
Turn-On Delay Time ^c	$t_{\text{d}(\text{on})}$	$V_{\text{DD}} = 10 \text{ V}$, $R_L = 0.2 \Omega$ $I_D \cong 50 \text{ A}$, $V_{\text{GEN}} = 10 \text{ V}$, $R_g = 2.5 \Omega$		20	30	ns
Rise Time ^c	t_r			20	30	
Turn-Off Delay Time ^c	$t_{\text{d}(\text{off})}$			50	75	
Fall Time ^c	t_f			15	25	
Source-Drain Diode Ratings and Characteristics $T_C = 25^\circ\text{C}$						
Pulsed Current	I_{SM}				100	A
Diode Forward Voltage ^b	V_{SD}	$I_F = 50 \text{ A}$, $V_{\text{GS}} = 0 \text{ V}$		0.9	1.5	V
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 50 \text{ A}$, $dl/dt = 100 \text{ A}/\mu\text{s}$		45	70	ns

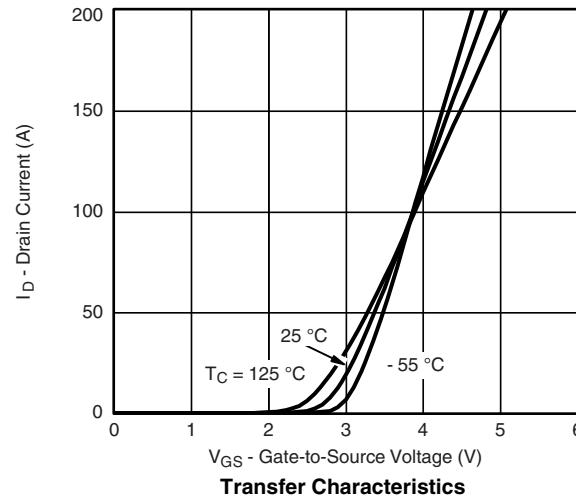
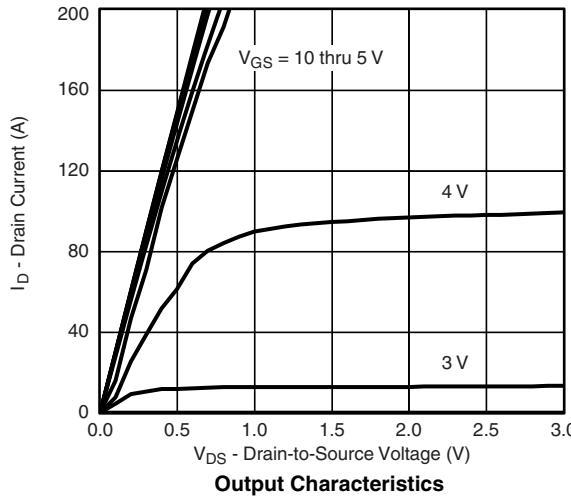
Notes:

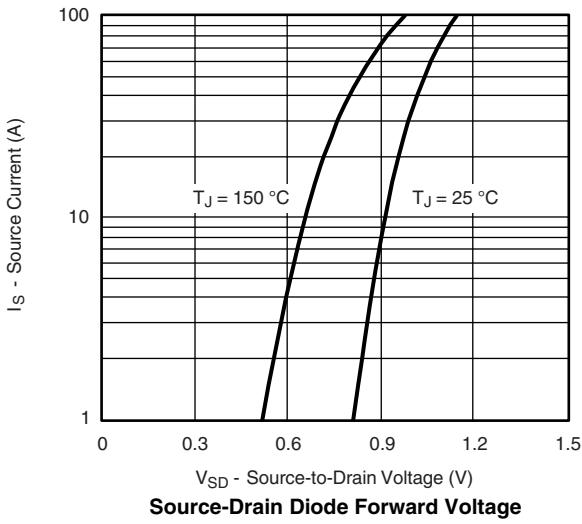
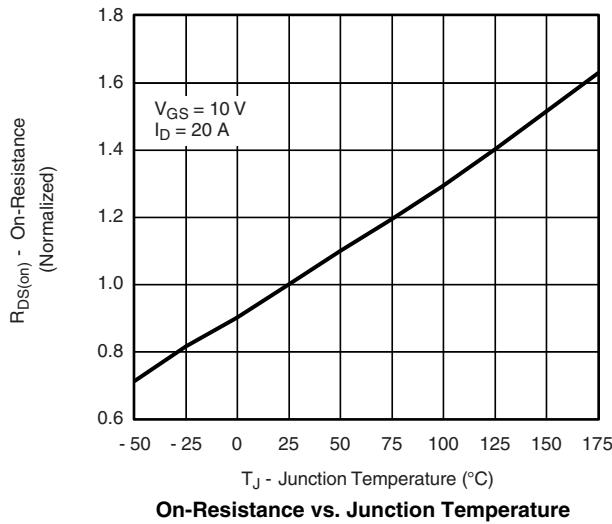
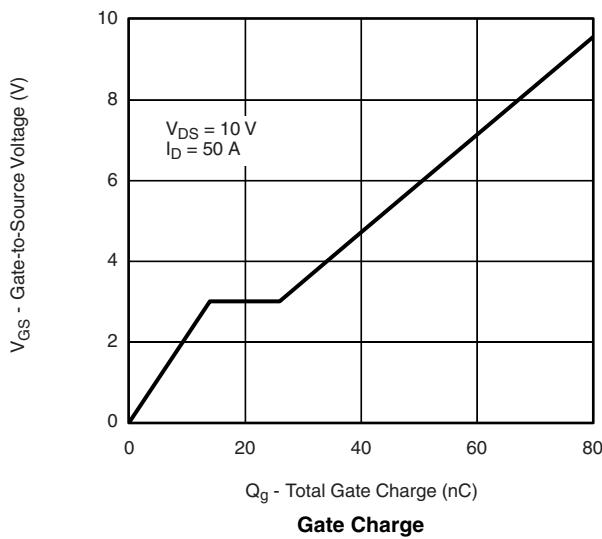
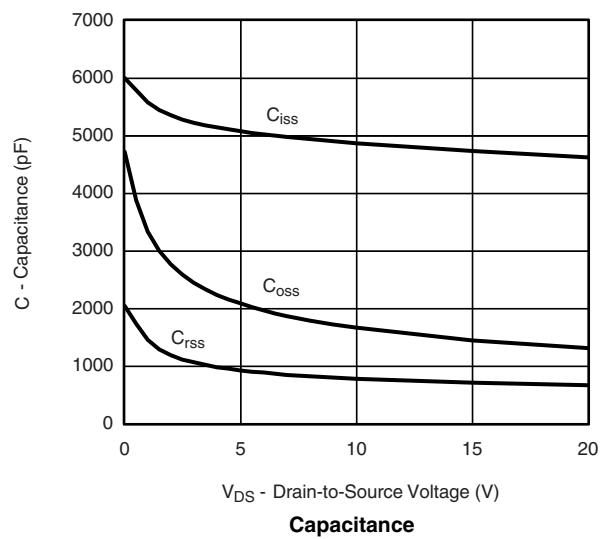
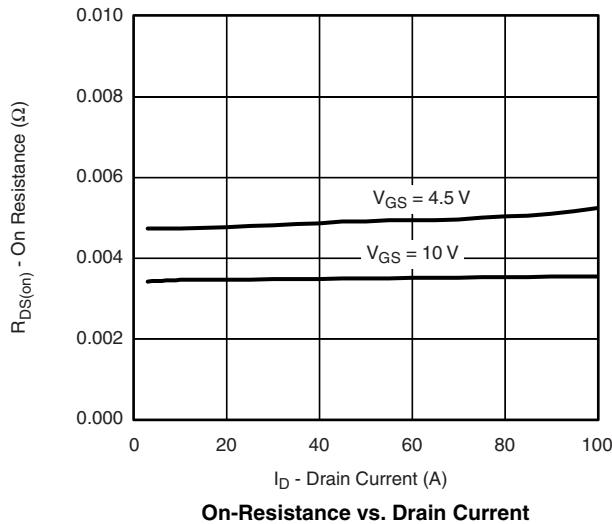
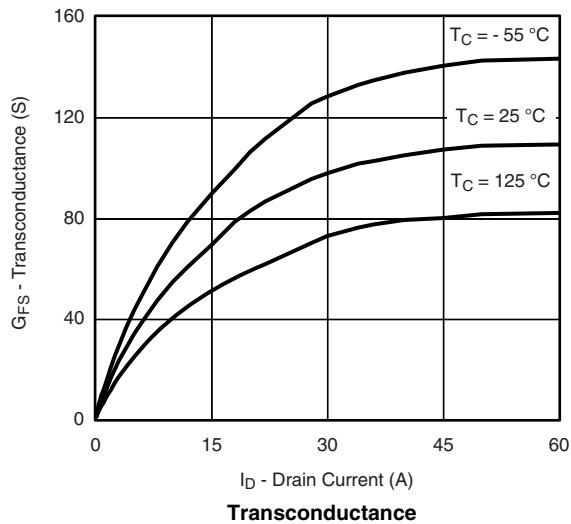
a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.

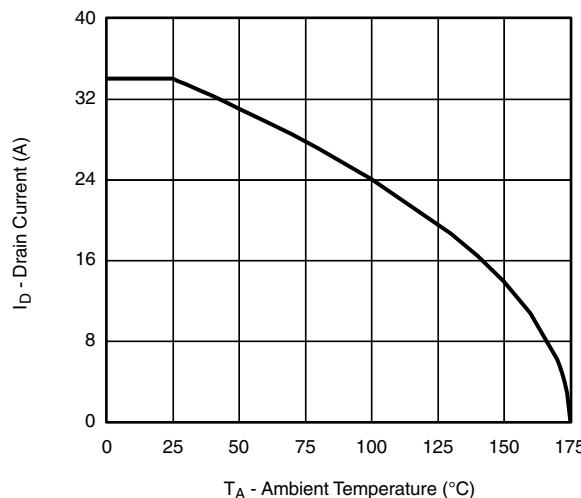
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

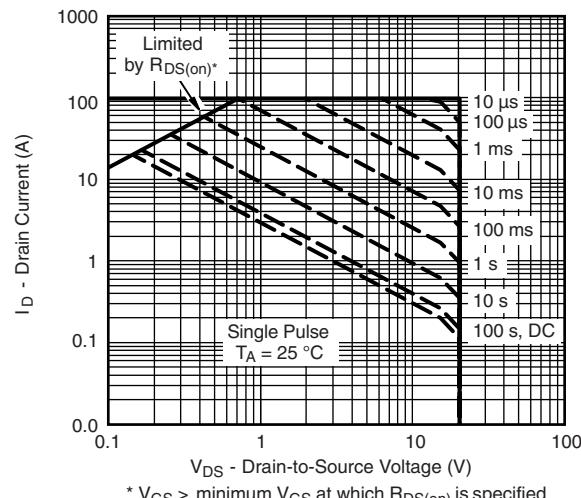
TYPICAL CHARACTERISTICS (25°C , unless otherwise noted)


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


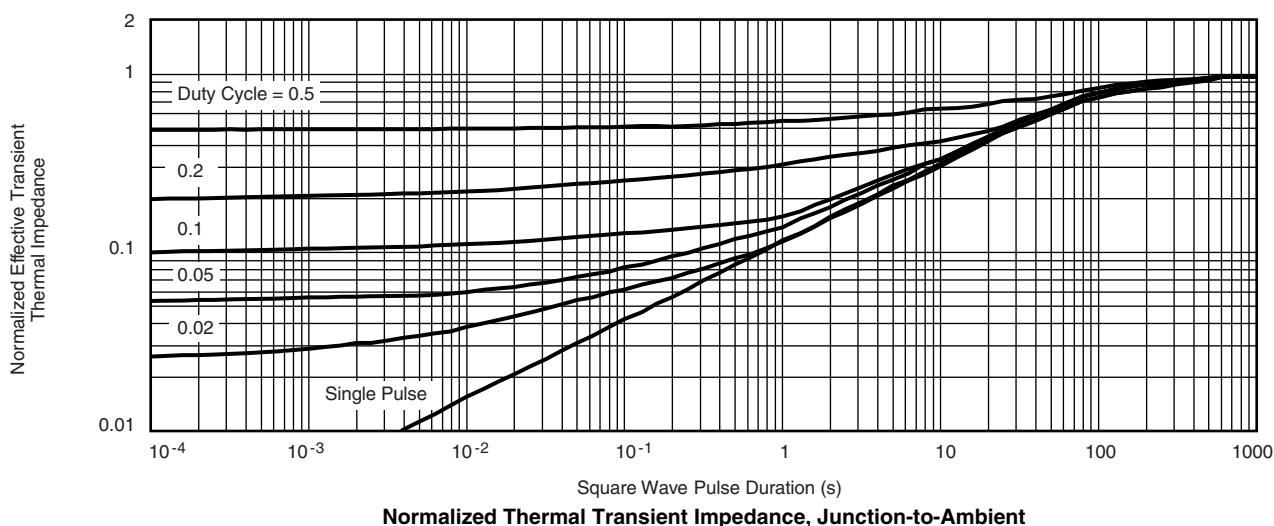
THERMAL RATINGS



Max. Avalanche and Drain Current vs.
Ambient Temperature



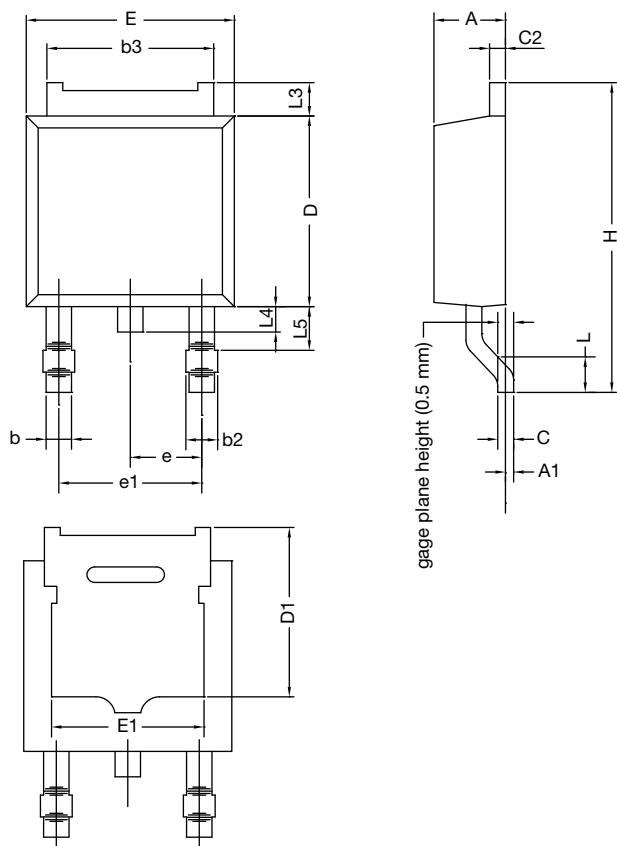
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?72216.

TO-252AA Case Outline

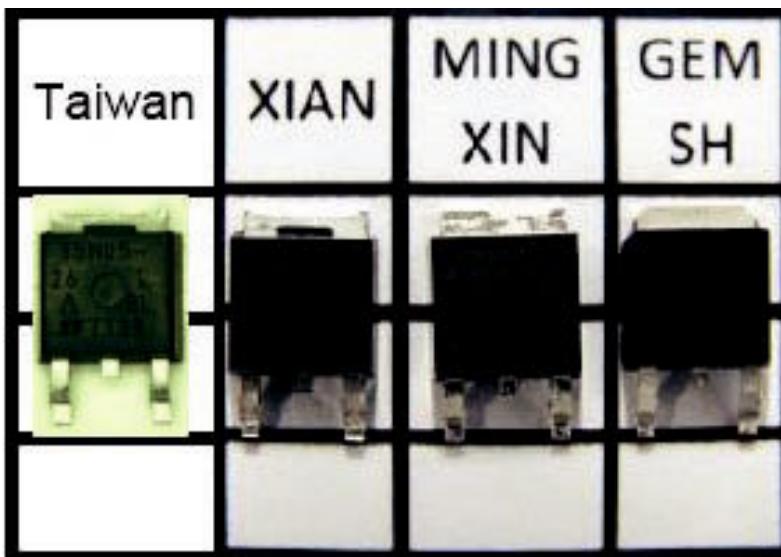


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060

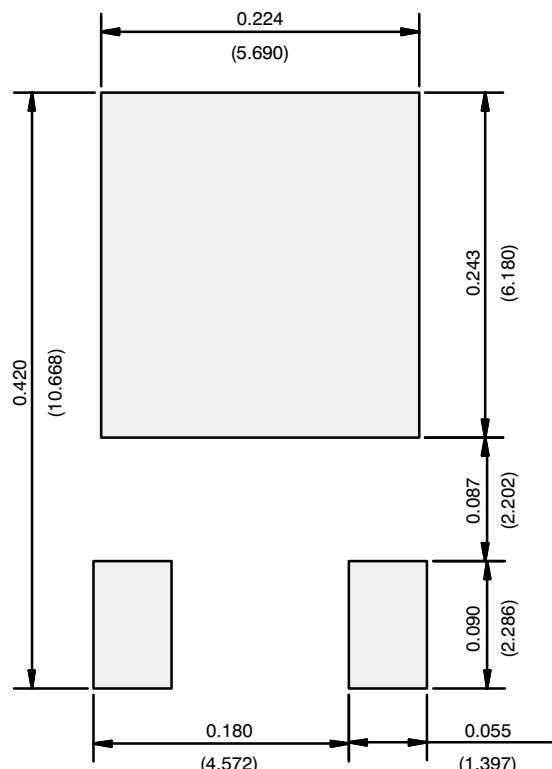
ECN: T13-0359-Rev. O, 03-Jun-13
DWG: 5347

Notes

- Dimension L3 is for reference only.
- Xi'an, Mingxin, and GEM SH actual photo.



RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



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APPLICATION NOTE

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