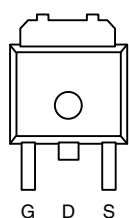


N-Channel 20 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY

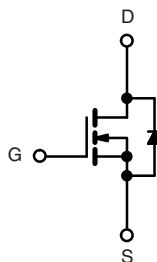
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a
20	0.0043 at V _{GS} = 10 V	34
	0.006 at V _{GS} = 4.5 V	28

TO-252



Top View

Drain Connected to Tab



N-Channel MOSFET

Ordering Information:
SUD50N02-04P-E3 (Lead (Pb)-free)

FEATURES

- TrenchFET® Power MOSFET
- 175 °C Junction Temperature
- PWM Optimized for High Efficiency
- Material categorization:
For definitions of compliance please see www.vishay.com/doc?99912


RoHS
COMPLIANT

APPLICATIONS

- Synchronous Buck Converter
 - Low-Side
 - Desktop, Servers, Desknote
- Synchronous Rectification
 - POL

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	20	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current ^a	I _D	34 ^a	A
		50 ^b	
Pulsed Drain Current	I _{DM}	100	
Continuous Source Current (Diode Conduction) ^a	I _S	8.3 ^a	
Avalanche Current ^c	I _{AS}	50	
Avalanche Energy ^c	E _{AS}	125	mJ
Maximum Power Dissipation	P _D	8.3 ^a	W
		136	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	R _{thJA}	15	18	°C/W
		40	50	
Maximum Junction-to-Case	R _{thJC}	0.85	1.1	

Notes:

- Surface mounted on FR4 board, t ≤ 10 s.
- Limited by package.
- Single pulse.

SPECIFICATIONS ($T_J = 25^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ. ^a	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	20			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	0.8		3.0	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V			1	μA
		V _{DS} = 20 V, V _{GS} = 0 V, T _J = 125 °C			50	
On-State Drain Current ^b	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	50			A
Drain-Source On-State Resistance ^b	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A		0.0035	0.0043	Ω
		V _{GS} = 10 V, I _D = 20 A, T _J = 125 °C			0.0061	
		V _{GS} = 4.5 V, I _D = 20 A		0.0048	0.006	
Forward Transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 20 A	15			S
Dynamic ^a						
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 10 V, f = 1 MHz		5000		pF
Output Capacitance	C _{oss}			1650		
Reverse Transfer Capacitance	C _{rss}			770		
Gate Resistance	R _g	f = 1 MHz		1.6		Ω
Total Gate Charge ^c	Q _g	V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 50 A		40	60	nC
Gate-Source Charge ^c	Q _{gs}			14		
Gate-Drain Charge ^c	Q _{gd}			13		
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = 10 V, R _L = 0.2 Ω I _D ≅ 50 A, V _{GEN} = 10 V, R _g = 2.5 Ω		20	30	ns
Rise Time ^c	t _r			20	30	
Turn-Off Delay Time ^c	t _{d(off)}			50	75	
Fall Time ^c	t _f			15	25	
Source-Drain Diode Ratings and Characteristics T _C = 25 °C						
Pulsed Current	I _{SM}				100	A
Diode Forward Voltage ^b	V _{SD}	I _F = 50 A, V _{GS} = 0 V		0.9	1.5	V
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 50 A, dI/dt = 100 A/μs		45	70	ns

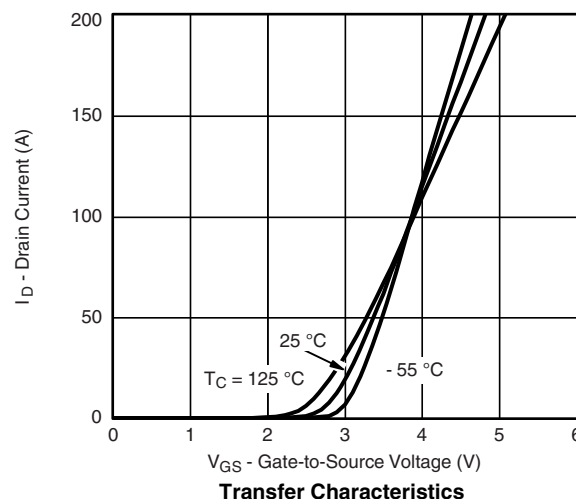
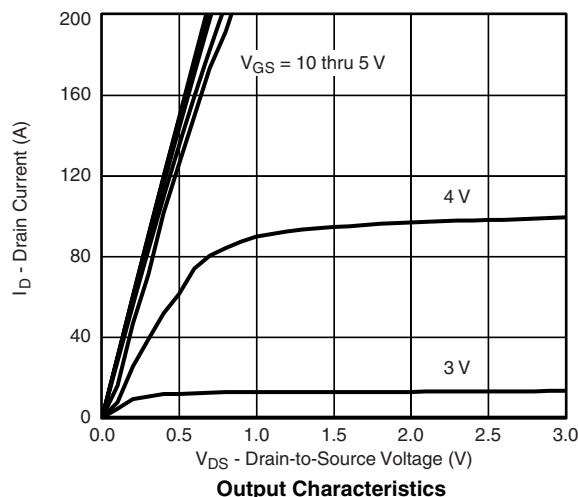
Notes:

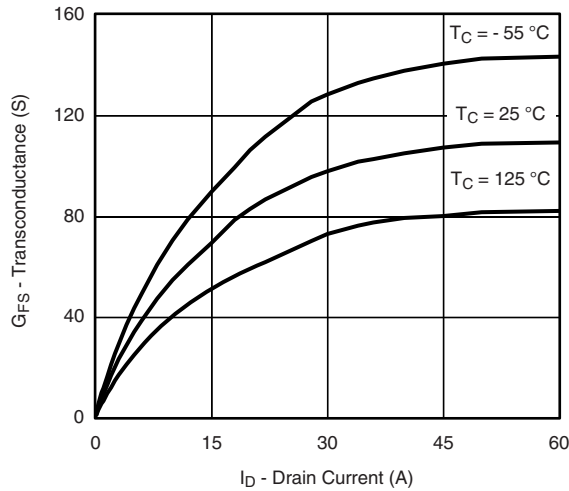
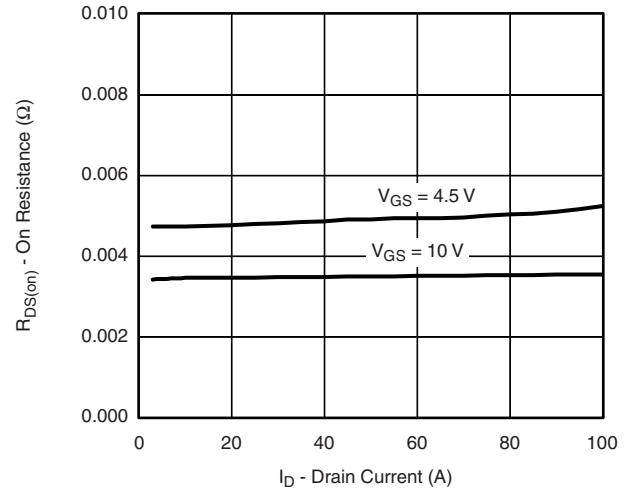
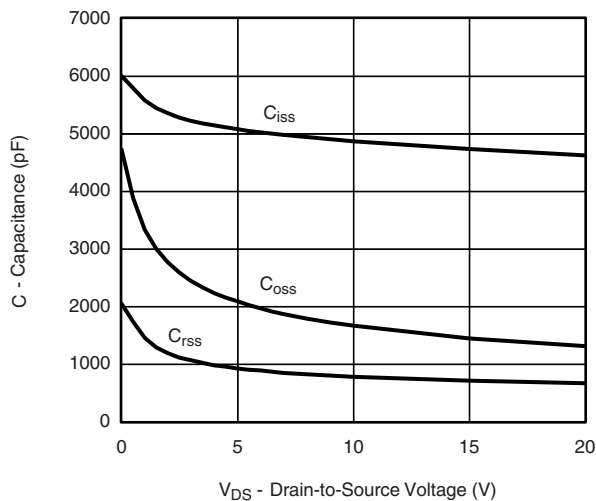
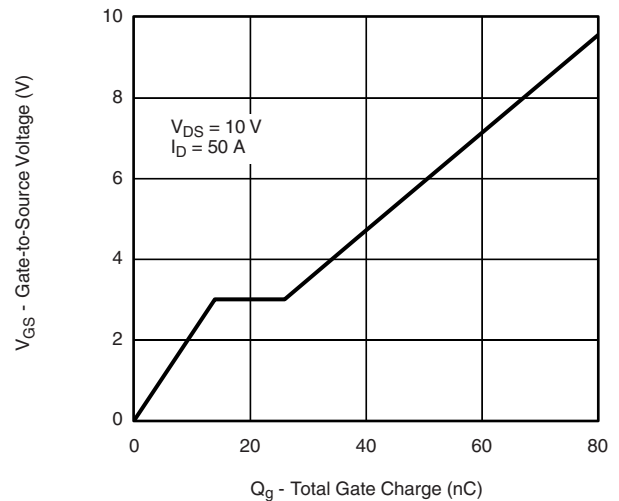
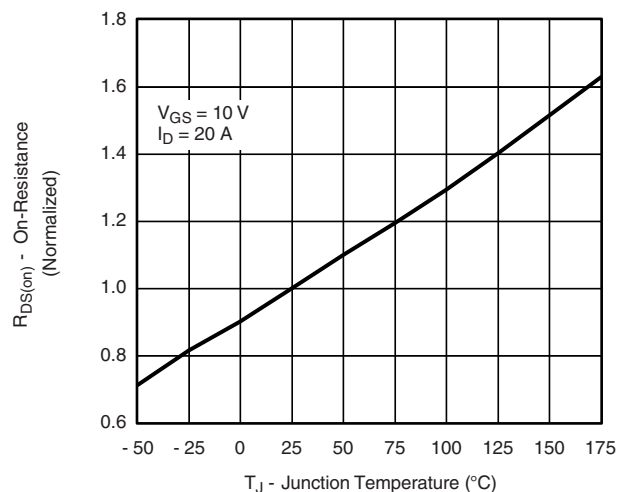
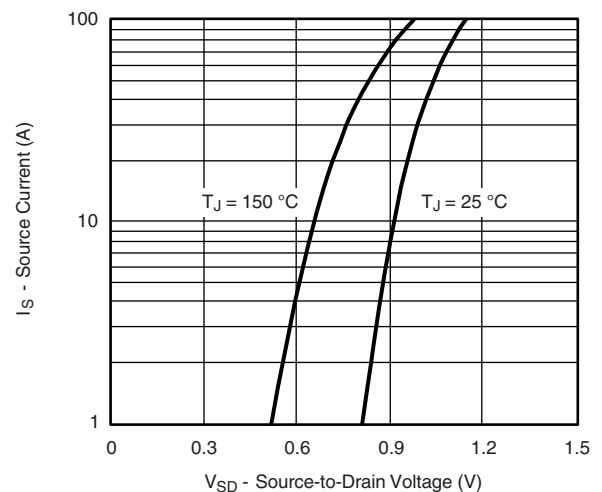
a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

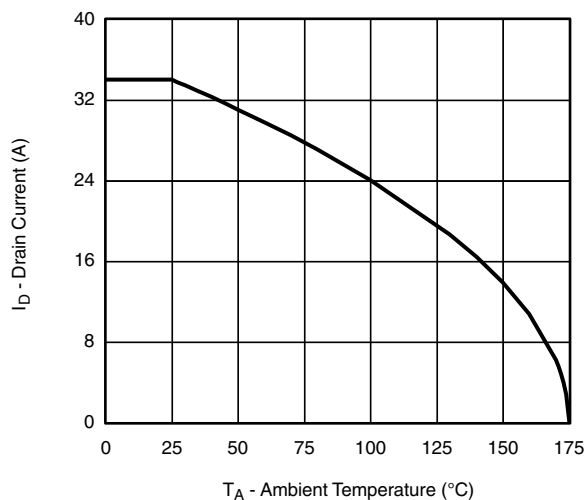
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

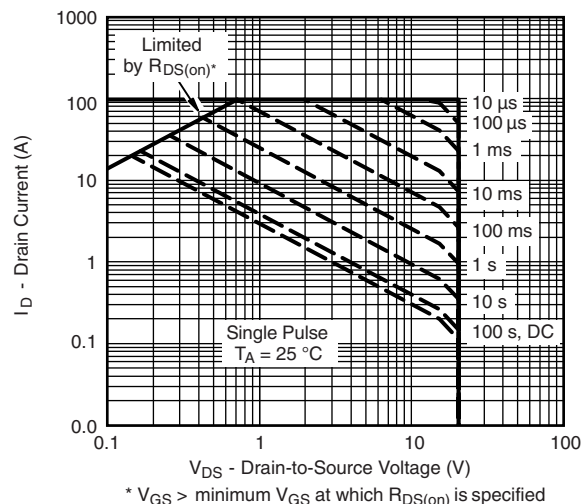
TYPICAL CHARACTERISTICS (25°C , unless otherwise noted)

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Transconductance

On-Resistance vs. Drain Current

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature

Source-Drain Diode Forward Voltage

THERMAL RATINGS

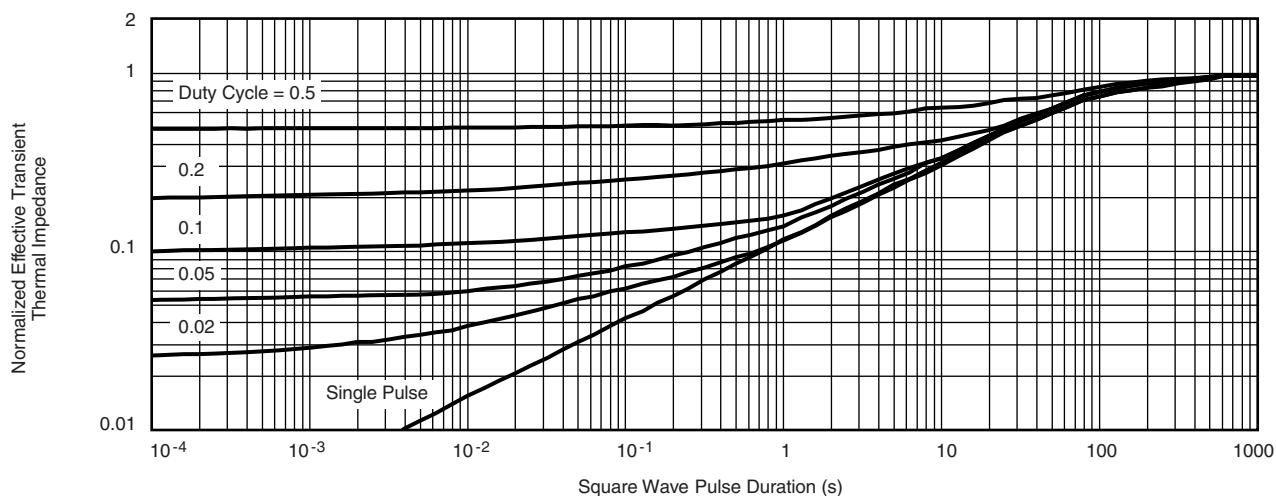


Max. Avalanche and Drain Current vs. Ambient Temperature



* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area

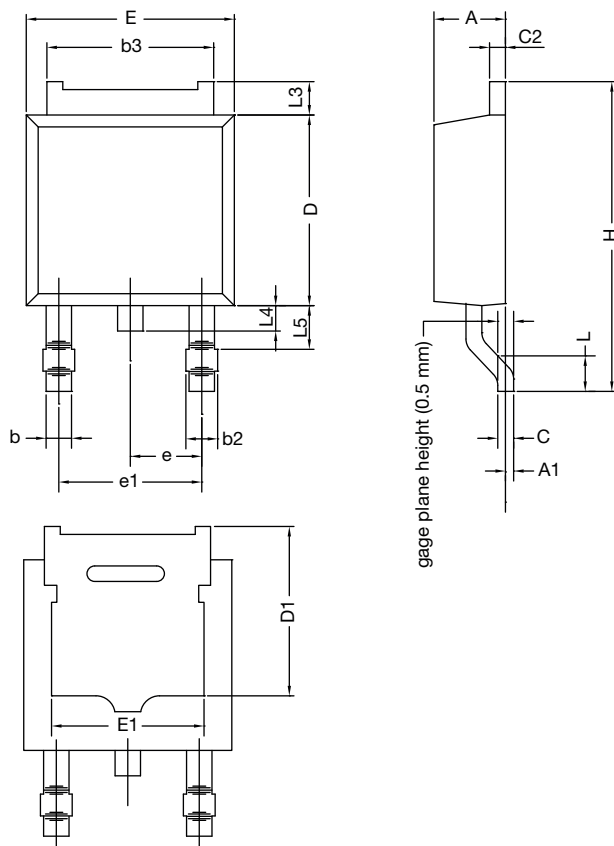


Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?72216.



TO-252AA Case Outline

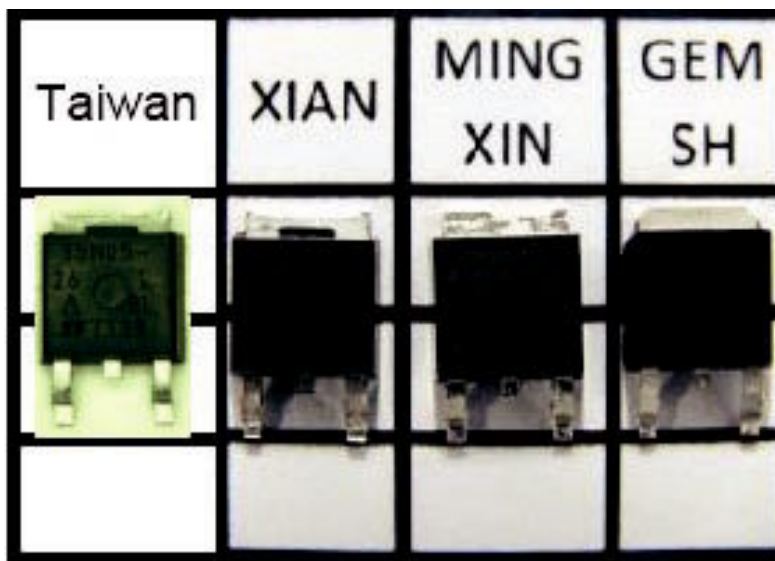


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060

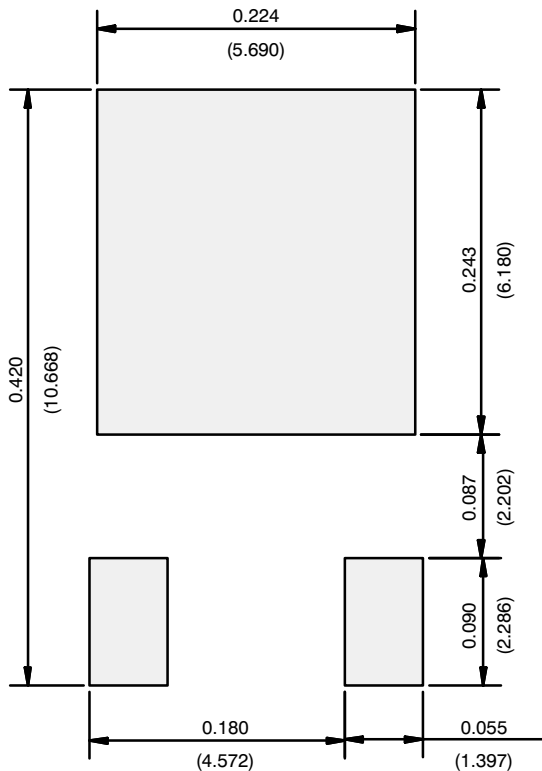
ECN: T13-0359-Rev. O, 03-Jun-13
DWG: 5347

Notes

- Dimension L3 is for reference only.
- Xi'an, Mingxin, and GEM SH actual photo.



RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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