ZL30138

OC-192/STM-64 SONET/SDH/10GbE Stratum 2/3/3E System Synchronizer/SETS

Short Form Data Sheet

July 2009

Features

- Supports the requirements of ITU-T G.8262 for synchronous Ethernet Equipment slave Clocks (EEC option 1 and 2)
- Supports the requirements of Telcordia GR-1244 Stratum 2/3/3E and GR-253, ITU-T G.812, G.813, and G.781 SETS
- Supports ITU-T G.823, G.824 and G.8261 for 2048 kbits/s and 1544 kbits.s interfaces
- Meets the SONET/SDH jitter generation requirements up to OC-192/STM-64
- Synchronizes to telecom reference clocks (2 kHz, N*8 kHz up to 77.76 MHz, 155.52 MHz) or to Ethernet reference clocks (25 MHz, 50 MHz, 62.5 MHz, 125 MHz)
- Supports composite clock inputs (64 kHz, 64 kHz + 8 kHz, 64kHz + 8 kHz + 400 Hz)
- Generates standard SONET/SDH clock rates (e.g. 19.44 MHz, 38.88 MHz, 77.76 MHz, 155.52 MHz, 622.08 MHz) or Ethernet clock rates (e.g. 25 MHz, 50 MHz, 125 MHz, 156.25 MHz, 312.5 MHz) for synchronizing Gigabit Ethernet PHYs
- Programmable output synthesizers (P0, P1) generate telecom clock frequencies from any multiple of 8 kHz up to 100 MHz
- Generates several styles of telecom frame pulses with selectable pulse width, polarity and frequency

Ordering Information

ZL30138GGG	100 Pin CABGA	Trays
ZL30138GGG2	100 Pin CABGA*	Trays

*Pb Free Tin/Silver/Copper

-40°C to +85°C

- Provides two DPLLs which are independently configurable through a serial interface
- Internal state machine automatically controls mode of operation (free-run, locked, holdover)
- Flexible input reference monitoring automatically disqualifies references based on frequency and phase irregularities
- Provides automatic reference switching and holdover during loss of reference input
- Supports master/slave configuration and dynamic input to output delay compensation for AdvancedTCA™
- Configurable input to output delay and output to output phase alignment

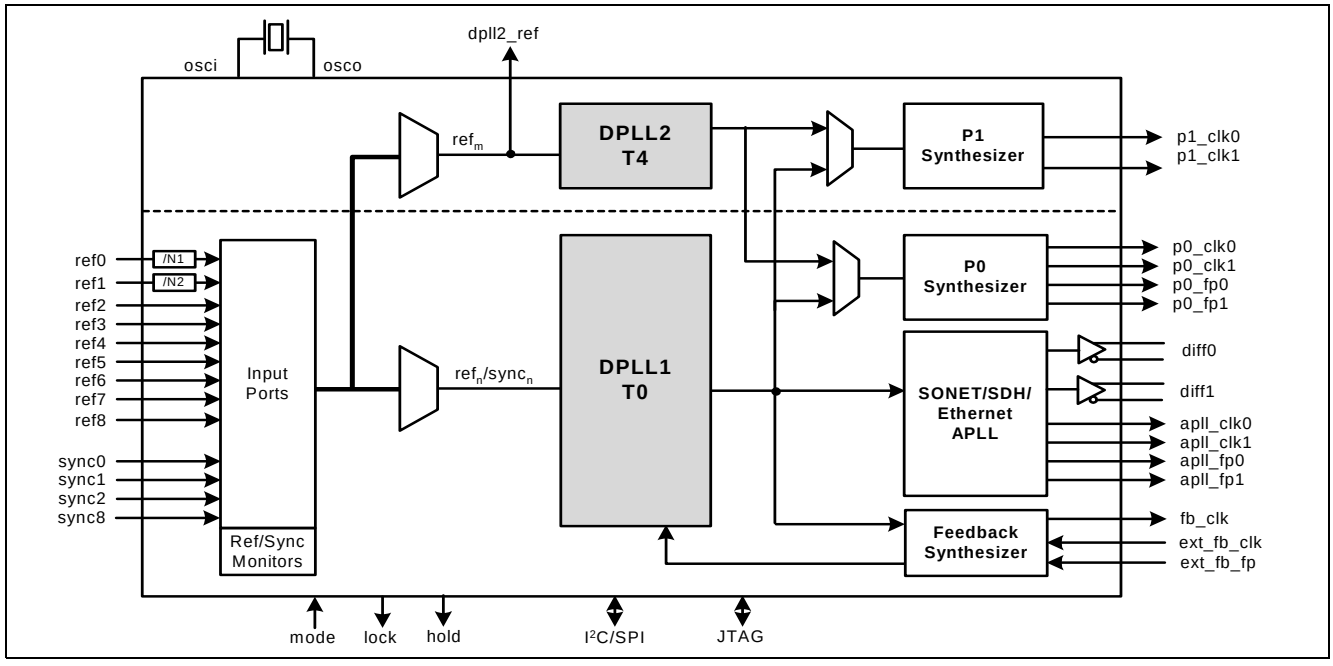


Figure 1 - Functional Block Diagram

Applications

- ITU-T G.8262 System Timing Cards which support 1 GbE and 10 GbE interfaces
- Telcordia GR-253 Carrier Grade SONET/SDH Stratum 2/3E/3 System Timing Cards
- System Timing Cards which supports ITU-T G.781 SETS (SDH Equipment Timing Source)

Change Summary

The following table captures the changes from the February 2008 issue.

Page	Item	Change
1	Feature list	Added support for G.823, G.824 and G.8261
6	p0_clkn and p1_clkn maximum clock frequency	Changed max frequency of the P0 and P1 clocks from 77.76 MHz to 100 MHz.

Pin Description

Pin #	Name	I/O Type	Description
Input Reference			
C1 B2 A3 C3 B3 B4 C4 A4	ref0 ref1 ref2 ref3 ref4 ref5 ref6 ref7	I_u	**Input References 7:0 (LVCMOS, Schmitt Trigger).** These input references are available to both DPLL1 and DPLL2 for synchronizing output clocks. All eight input references can lock to any multiple of 8 kHz up to 77.76 MHz including 25 MHz and 50 MHz. Input ref0 and ref1 have additional configurable pre-dividers allowing input frequencies of 62.5 MHz, 125 MHz, and 155.52 MHz. These pins are internally pulled up to V_{dd}.
B1 A1 A2	sync0 sync1 sync2	I_u	**Frame Pulse Synchronization References 2:0 (LVCMOS, Schmitt Trigger).** These are optional frame pulse synchronization inputs associated with input references 0, 1 and 2. These inputs accept frame pulses in a clock format (50% duty cycle) or a basic frame pulse format with minimum pulse width of 5 ns. These pins are internally pulled up to $V_{dd.}$
C5	ref8/ext_fb_clk	I_u	**Input Reference 8/External DPLL Feedback Clock (LVCMOS, Schmitt Trigger).** This pin acts as either an ext_fb_clk input or as the ref8 input. The desired function for the pin is selectable through the software interface with a programmable register bit. This pin is internally pulled up to $V_{dd.}$ Leave open when not in use.
B5	sync8/ext_fb_fp	I_u	**Frame Pulse Synchronization Reference 8/External DPLL Feedback Frame Pulse (LVCMOS, Schmitt Trigger).** This pin acts as either an ext_fb_fp input or as the sync8 input. The desired function for the pin is selectable through the software interface with a programmable register bit. This pin is internally pulled up to $V_{dd.}$ Leave open when not in use.
Output Clocks and Frame Pulses			
A9 B10	diff0_p diff0_n	O	**Differential Output Clock 0 (LVPECL).** When in SONET/SDH mode, this output can be configured to provide any one of the available SONET/SDH clocks (6.48 MHz, 19.44 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 311.04 MHz, 622.08 MHz). When in Ethernet mode, this output can be configured to provide any of the Ethernet clocks (25 MHz, 50 MHz, 62.5 MHz, 125 MHz, 156.25 MHz, 312.5 MHz). See “Output Clocks and Frame Pulses” on page 31 for more details on clock frequency settings.
A10 B9	diff1_p diff1_n	O	**Differential Output Clock 1 (LVPECL).** When in SONET/SDH mode, this output can be configured to provide any one of the available SONET/SDH clocks (6.48 MHz, 19.44 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 311.04 MHz, 622.08 MHz). When in Ethernet mode, this output can be configured to provide any of the Ethernet clocks (25 MHz, 50 MHz, 62.5 MHz, 125 MHz, 156.25 MHz, 312.5 MHz). See “Output Clocks and Frame Pulses” on page 31 for more details on clock frequency settings.
D10	apll_clk0	O	**APLL Output Clock 0 (LVCMOS).** This output can be configured to provide any one of the SONET/SDH clock outputs up to 77.76 MHz or any of the Ethernet clock rates up to 125 MHz. The default frequency for this output is 77.76 MHz.
G10	apll_clk1	O	**APLL Output Clock 1 (LVCMOS).** This output can be configured to provide any one of the SONET/SDH clock outputs up to 77.76 MHz or any of the Ethernet clock rates up to 125 MHz. The default frequency for this output is 19.44 MHz.

Pin #	Name	I/O Type	Description
E10	apll_fp0	O	**APLL Output Frame Pulse 0 (LVCMOS).** This output can be configured to provide virtually any style of output frame pulse synchronized with an associated SONET/SDH family output clock. The default frequency for this frame pulse output is 8 kHz.
F10	apll_fp1	O	**APLL Output Frame Pulse 1 (LVCMOS).** This output can be configured to provide virtually any style of output frame pulse synchronized with an associated SONET/SDH family output clock. The default frequency for this frame pulse output is 2 kHz.
K9	p0_clk0	O	**Programmable Synthesizer 0 - Output Clock 0 (LVCMOS).** This output can be configured to provide any frequency with a multiple of 8 kHz up to 77.76 MHz in addition to 2 kHz. The default frequency for this output is 2.048 MHz.
K7	p0_clk1	O	**Programmable Synthesizer 0 - Output Clock 1 (LVCMOS).** This is a programmable clock output configurable as a multiple or division of the p0_clk0 frequency within the range of 2 kHz to 77.76 MHz. The default frequency for this output is 8.192 MHz.
K8	p0_fp0	O	**Programmable Synthesizer 0 - Output Frame Pulse 0 (LVCMOS).** This output can be configured to provide virtually any style of output frame pulse associated with the p0 clocks. The default frequency for this frame pulse output is 8 kHz.
J7	p0_fp1	O	**Programmable Synthesizer 0 - Output Frame Pulse 1 (LVCMOS).** This output can be configured to provide virtually any style of output frame pulse associated with the p0 clocks. The default frequency for this frame pulse output is 8 kHz
J10	p1_clk0	O	**Programmable Synthesizer 1 - Output Clock 0 (LVCMOS).** This output can be configured to provide any frequency with a multiple of 8 kHz up to 100 MHz in addition to 2 kHz. The default frequency for this output is 1.544 MHz (DS1).
K10	p1_clk1	O	**Programmable Synthesizer1 - Output Clock 1 (LVCMOS).** This is a programmable clock output configurable as a multiple or division of the p1_clk0 frequency within the range of 2 kHz to 100 MHz. The default frequency for this output is 3.088 MHz (2x DS1).
H10	fb_clk	O	**Feedback Clock (LVCMOS).** This output is a buffered copy of the feedback clock for DPLL1. The frequency of this output always equals the frequency of the selected reference.
E1	dpll2_ref	O	**DPLL2 Selected Output Reference (LVCMOS).** This is a buffered copy of the output of the reference selector for DPLL2. Switching between input reference clocks at this output is not hitless.
Control			
H5	rst_b	I	**Reset (LVCMOS, Schmitt Trigger).** A logic low at this input resets the device. To ensure proper operation, the device must be reset after power-up. Reset should be asserted for a minimum of 300 ns.
J5	dpll1_hs_en	I_u	**DPLL1 Hitless Switching Enable (LVCMOS, Schmitt Trigger).** A logic high at this input enables hitless reference switching. A logic low disables hitless reference switching and re-aligns DPLL1's output phase to the phase of the selected reference input. This feature can also be controlled through software registers. This pin is internally pulled up to Vdd.

Pin #	Name	I/O Type	Description
C2 D2	dpll1_mod_sel0 dpll1_mod_sel1	I_u	**DPLL1 Mode Select 1:0 (LVCMOS, Schmitt Trigger).** During reset, the levels on these pins determine the default mode of operation for DPLL1 (Automatic, Normal, Holdover or Freerun). After reset, the mode of operation can be controlled directly with these pins, or by accessing the dpll1_modesel register (0x1F) through the serial interface. This pin is internally pulled up to Vdd.
D1	slave_en	I_u	**Master/Slave control (LVCMOS, Schmitt Trigger).** This pin selects the mode of operation for the device. If set high, slave mode is selected. If set low, master mode is selected. This feature can also be controlled through software registers. This pin is internally pulled up to Vdd.
K1	diff0_en	I_u	**Differential Output 0 Enable (LVCMOS, Schmitt Trigger).** When set high, the differential LVPECL output 0 driver is enabled. When set low, the differential driver is tristated reducing power consumption. This pin is internally pulled up to Vdd.
D3	diff1_en	I_u	**Differential Output 1 Enable (LVCMOS, Schmitt Trigger).** When set high, the differential LVPECL output 1 driver is enabled. When set low, the differential driver is tristated reducing power consumption.This pin is internally pulled up to Vdd.
Status			
H1	dpll1_lock	O	**Lock Indicator (LVCMOS).** This is the lock indicator pin for DPLL1. This output goes high when DPLL1's output is frequency and phase locked to the input reference.
J1	dpll1_holdover	O	**Holdover Indicator (LVCMOS).** This pin goes high when DPLL1 enters the holdover mode.
Serial Interface			
E2	sck_scl	I/B	**Clock for Serial Interface (LVCMOS).** Serial interface clock. When i2c_en = 0, this pin acts as the sck pin for the serial interface. When i2c_en = 1, this pin acts as the scl pin (bidirectional) for the I^2C interface.
F1	si_sda	I/B	**Serial Interface Input (LVCMOS).** Serial interface data pin. When i2c_en = 0, this pin acts as the si pin for the serial interface. When i2c_en = 1, this pin acts as the sda pin (bidirectional) for the I^2C interface.
G1	so	O	**Serial Interface Output (LVCMOS).** Serial interface data output. When i2c_en = 0, this pin acts as the so pin for the serial interface. When i2c_en = 1, this pin is unused and should be left unconnected.
E3	cs_b_asel0	I_u	**Chip Select/Address Select 0 for the Serial Interface (LVCMOS).** Serial interface chip select. When i2c_en = 0, this pin acts as the cs pin (active low) for the serial interface. When i2c_en = 1, this pin acts as the asel0 pin for the I^2C interface.
G2	int_b	O	**Interrupt Pin (LVCMOS).** Indicates a change of device status prompting the processor to read the enabled interrupt service registers (ISR). This pin is an open drain, active low and requires an external pulled up to VDD.
J2	i2c_en	I_u	**I^2C Interface Enable (LVCMOS).** If set high, the I^2C interface is enabled, if set low, the SPI interface is enabled. Internally pull-up to Vdd.

Pin #	Name	I/O Type	Description
APLL Loop Filter			
A6	apll_filter	A	**External Analog PLL Loop Filter terminal.**
B6	filter_ref0	A	**Analog PLL External Loop Filter Reference.**
C6	filter_ref1	A	**Analog PLL External Loop Filter Reference.**
JTAG and Test			
J4	tdo	O	**Test Serial Data Out (Output).** JTAG serial data is output on this pin on the falling edge of tck. This pin is held in high impedance state when JTAG scan is not enabled.
K2	tdi	I_u	**Test Serial Data In (Input).** JTAG serial test instructions and data are shifted in on this pin. This pin is internally pulled up to Vdd. If this pin is not used then it should be left unconnected.
H4	trst_b	I_u	**Test Reset (LVCMOS).** Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be pulsed low on power-up to ensure that the device is in the normal functional state. This pin is internally pulled up to Vdd. If this pin is not used then it should be connected to GND.
K3	tck	I	**Test Clock (LVCMOS):** Provides the clock to the JTAG test logic. If this pin is not used then it should be pulled down to GND.
J3	tms	I_u	**Test Mode Select (LVCMOS).** JTAG signal that controls the state transitions of the TAP controller. This pin is internally pulled up to V_{DD}. If this pin is not used then it should be left unconnected.
Master Clock			
K4	osci	I	**Oscillator Master Clock Input (LVCMOS).** This input accepts a 20 MHz reference from a clock oscillator (TCXO, OCXO). The stability and accuracy of the clock at this input determines the free-run accuracy and the long term holdover stability of the output clocks.
K5	osco	O	**Oscillator Master Clock Output (LVCMOS).** This pin must be left unconnected when the osci pin is connected to a clock oscillator.
Miscellaneous			
J6 G3	IC		**Internal Connection.** Connect to ground.
K6	IC		**Internal Connection.** Leave unconnected.
F2 F3 H7	NC		**No Connection.** Leave unconnected.

Pin #	Name	I/O Type	Description
Power and Ground			
D9 E4 G8 G9 J8 J9 H6 H8	V_{DD}	P P P P P P P P	**Positive Supply Voltage.** +3.3V_{DC} nominal.
E8 F4	V_{CORE}	P P	**Positive Supply Voltage.** +1.8V_{DC} nominal.
A5 A8 C10	AV_{DD}	P P P	**Positive Analog Supply Voltage.** +3.3V_{DC} nominal.
B7 B8 H2	AV_{CORE}	P P P	**Positive Analog Supply Voltage.** +1.8V_{DC} nominal.
D4 D5 D6 D7 E5 E6 E7 F5 F6 F7 G4 G5 G6 G7 E9 F8 F9 H9	V_{SS}	G G G G G G G G G G G G G G G G G G	**Ground.** 0 Volts.
A7 C7 C8 C9 D8 H3	AV_{SS}	G G G G G G	**Analog Ground.** 0 Volts.

I - Input

I_d - Input, Internally pulled down

I_u - Input, Internally pulled up

O - Output

A - Analog

P - Power

G - Ground

1.0 Pin Diagram

TOP VIEW

	1	2	3	4	5	6	7	8	9	10
A	sync1	sync2	ref2	ref7	AV_{DD}	apll_filter	AV_{SS}	AV_{DD}	diff0_p	diff1_p
B	sync0	ref1	ref4	ref5	sync8/ ext_fb_fp	filter_ref0	AV_{CORE}	AV_{CORE}	diff1_n	diff0_n
C	ref0	dpll1_mod_ sel0	ref3	ref6	ref8/ ext_fb_clk	filter_ref1	AV_{SS}	AV_{SS}	AV_{SS}	AV_{DD}
D	slave_en	dpll1_mod_ sel1	diff1_en	V_{SS}	V_{SS}	V_{SS}	V_{SS}	AV_{SS}	V_{DD}	apll_clk0
E	dpll2_ref	sck/ scl	cs_b/ asel0	VDD	V_{SS}	V_{SS}	V_{SS}	V_{CORE}	V_{SS}	apll_fp0
F	si/ sdh	NC	IC	V_{CORE}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	apll_fp1
G	so	int_b	IC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DD}	apll_clk1
H	dpll1_lock	AV_{CORE}	AV_{SS}	trst_b	rst_b	V_{DD}	IC	V_{DD}	V_{SS}	fb_clk
J	dpll1_hold	i2c_en	tms	tdo	dpll1_hs_en	IC	p0_fp1	V_{DD}	V_{DD}	p1_clk0
K	diff0_en	tdi	tck	osci	osco	IC	p0_clk1	p0_fp0	p0_clk0	p1_clk1

1 - A1 corner is identified by metallized markings.

2.0 High Level Overview

The ZL30138 SONET/SDH/Ethernet Stratum 2/3E/3 System Synchronizer and SETS device is a highly integrated device that provides all of the functionality that is required for a central timing card in carrier grade network equipment. The basic functions of a central timing card include:

- Input reference monitoring for both frequency accuracy and phase irregularities
- Automatic input reference selection
- Support of both external timing and line timing modes
- Hitless reference switching
- Wander and jitter filtering
- Optional Input phase transient filtering (Stratum 3E phase build-out)
- Master/slave crossover for minimizing phase alignment between redundant timing cards
- Independent derived output timing path for support of the SETS functionality

In a typical application, the main timing path uses DPLL1 to synchronize to either an external BITS source or to a recovered line timed source. DPLL1 monitors all references and automatically selects the best available reference based on configurable priority and revertive properties. DPLL1 provides the wander filtering function and the P0 synthesizer generates a jitter filtered clock and frame pulse for the system timing bus which supplies all line cards with a common timing reference. The APLL is used to generate a reference clock for an Ethernet PHY which can be used to synchronize remote equipment. A derived output timing path using DPLL2 is available to support the SETS function. In this case DPLL2 uses a filter above 10 Hz to prevent it from filtering wander.

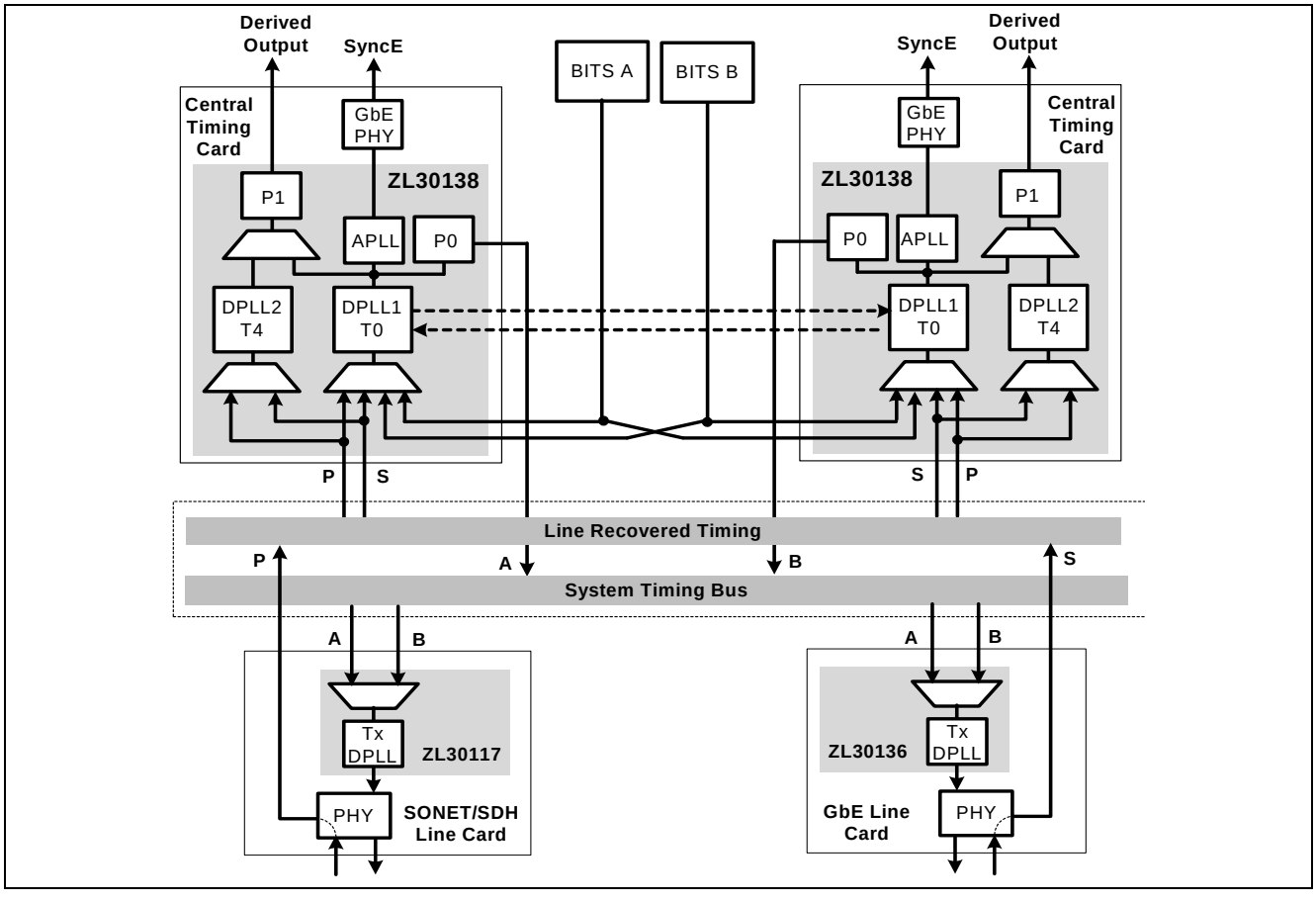


Figure 2 - Typical Application of the ZL30138

Alternatively, the ZL30138 could be used in systems that were not designed with central timing cards in mind. In this case, the ZL30138 provides all of the features required to meet both the timing card and the line card functions in one package. This application is shown in Figure 3. DPLL1 recovers the reference clock from the backplane and filters wander. The APLL and the P0 synthesizer filter jitter and generate transmit clocks for a SONET/SDH/10GbE PHY (up to OC-192/STM-64) and/or a PDH PHY (T1/E1, DS3/E3, etc). DPLL2 is used to recover the line timing reference, filter jitter, and translate its frequency to the rate required by the backplane.

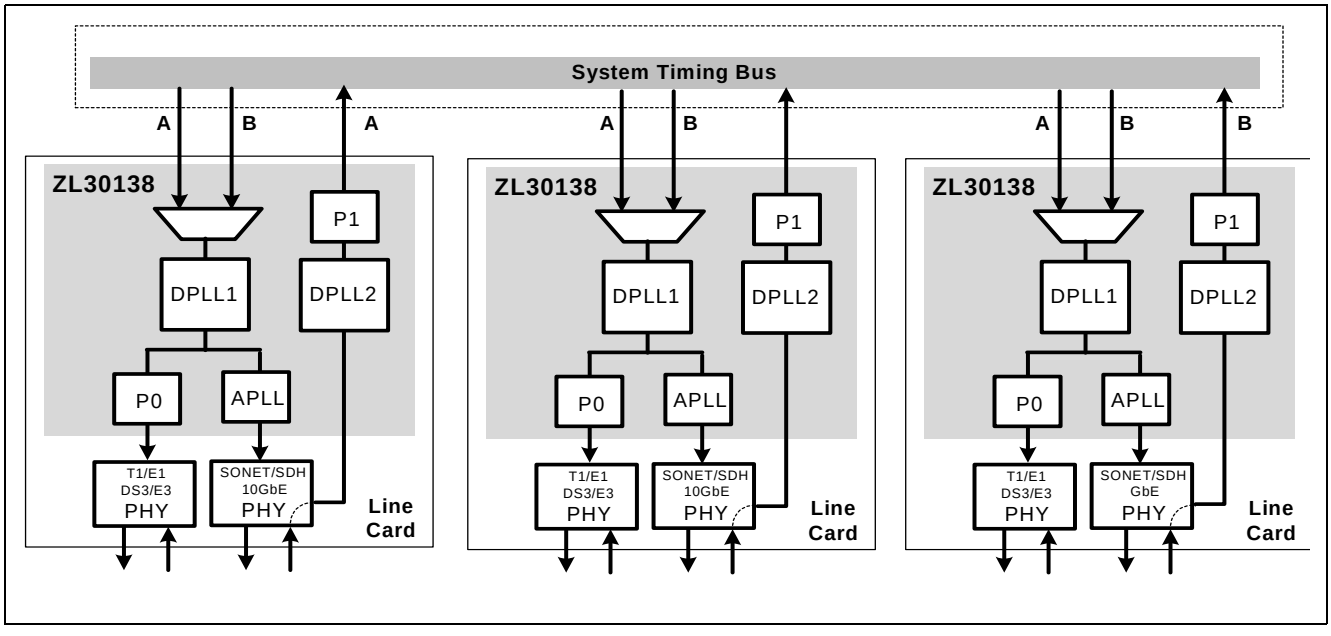
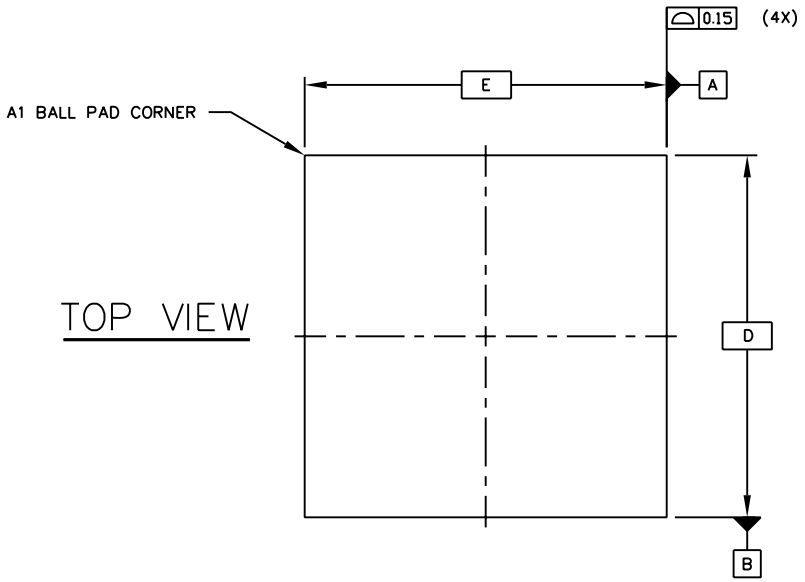
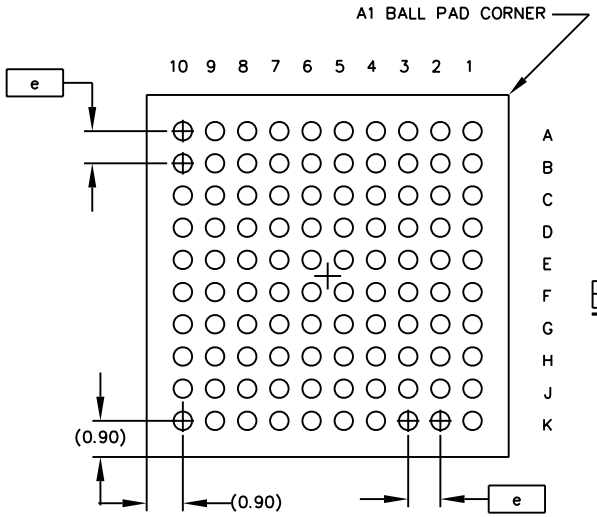


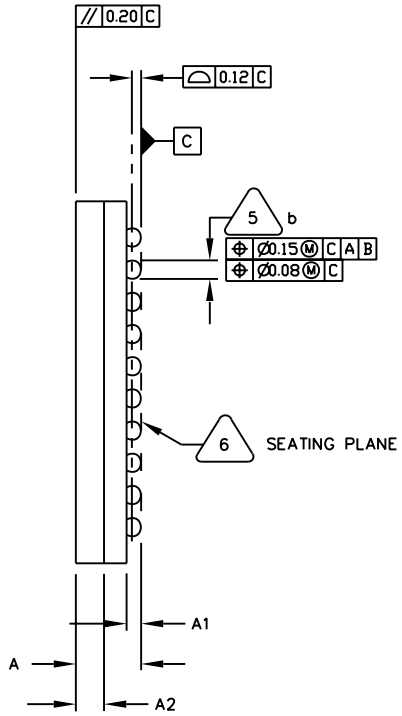
Figure 3 - The ZL30138 as a Timing Card and a Line Card Device





BOTTOM VIEW

100 SOLDER BALLS



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.52	1.62	1.72
A1	0.31	0.36	0.41
A2	0.65	0.70	0.75
b		0.46 Typ.	
D	8.85	9.00	9.15
E	8.85	9.00	9.15
e		0.8 Ref	
n		100	

6. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

5. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.

4. THE MAXIMUM ALLOWABLE NUMBER OF SOLDER BALLS IS 100.

3. Not to Scale.

2. THE BASIC SOLDER BALL GRID PITCH IS 0.8mm.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.

NOTES: UNLESS OTHERWISE SPECIFIED

ISSUE	1	2	3	
ACN	CDCA	CDCA	CDCA	
DATE	15April05	24Aug05	26Oct06	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

N/A

Package Code GG

Package Outline for 100ball 9x9mm, 0.8 mm Pitch, 4 layer, CABGA

111040

For more information about all Zarlink products visit our Web Site at

www.zarlink.com