International
IOR Rectifier

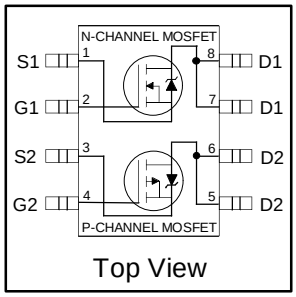
PD - 9.1098B

PRELIMINARY

IRF7106

HEXFET® Power MOSFET

- Advanced Process Technology
- Ultra Low On-Resistance
- Dual N and P Channel Mosfet
- Surface Mount
- Available in Tape & Reel
- Dynamic dv/dt Rating
- Fast Switching



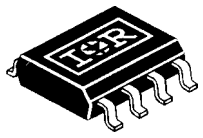
Top View

	N-Ch	P-Ch
V_{DSS}	20V	-20V
$R_{DS(on)}$	0.125Ω	0.20Ω
I_D	3.0A	-2.5A

Description

Fourth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design for which HEXFET Power MOSFETs are well known, provides the designer with an extremely efficient device for use in a wide variety of applications.

The SO-8 has been modified through a customized leadframe for enhanced thermal characteristics and multiple-die capability making it ideal in a variety of power applications. With these improvements, multiple devices can be used in an application with dramatically reduced board space. The package is designed for vapor phase, infra-red, or wave soldering techniques. Power dissipation of greater than 0.8W is possible in a typical PCB mount application.



SO-8

Absolute Maximum Ratings

	Parameter	Max.		Units
		N-Channel	P-Channel	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	3.0	-2.5	A
I_D @ T_C = 70°C	Continuous Drain Current, V_{GS} @ 10V	2.5	-2.0	
I_{DM}	Pulsed Drain Current ①	10	-10	
P_D @T_C = 25°C	Power Dissipation	2.0		W
	Linear Derating Factor	0.016		W/°C
V_{GS}	Gate-to-Source Voltage	± 20		V
dv/dt	Peak Diode Recovery dv/dt ②	3.0	-3.0	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150		°C

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount)**	——	——	62.5	°C/W

** When mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to application note #AN-994.

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter		Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	N-Ch	20	—	—	V	V_{GS} = 0V, I_D = 250µA
		P-Ch	-20	—	—		V_{GS} = 0V, I_D = -250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	N-Ch	—	0.037	—	V/°C	Reference to 25°C, I_D = 1mA
		P-Ch	—	-0.022	—		Reference to 25°C, I_D = -1mA
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	N-Ch	—	—	0.125	Ω	V_{GS} = 10V, I_D = 1.0A ③
			—	—	0.25		V_{GS} = 4.5V, I_D = 0.50A ③
		P-Ch	—	—	0.20		V_{GS} = -10V, I_D = -1.0A ③
			—	—	0.35		V_{GS} = -4.5V, I_D = -0.50A ③
$V_{GS(th)}$	Gate Threshold Voltage	N-Ch	1.0	—	—	V	V_{DS} = V_{GS}, I_D = 250µA
		P-Ch	-1.0	—	—		V_{DS} = V_{GS}, I_D = -250µA
g_{fs}	Forward Transconductance	N-Ch	—	4.4	—	S	V_{DS} = 15V, I_D = 3.0A ③
		P-Ch	—	3.0	—		V_{DS} = -15V, I_D = -3.0A③
I_{DSS}	Drain-to-Source Leakage Current	N-Ch	—	—	2.0	µA	V_{DS} = 16V, V_{GS} = 0V
		P-Ch	—	—	-2.0		V_{DS} = -16V, V_{GS} = 0V
		N-Ch	—	—	25		V_{DS} = 16V, V_{GS} = 0V, T_J = 125°C
		P-Ch	—	—	-25		V_{DS} = -16V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	N-P	—	—	±100	nA	V_{GS} = ± 20V
Q_g	Total Gate Charge	N-Ch	—	9.1	25	nC	N-Channel I_D = 2.3A, V_{DS} = 10V, V_{GS} = 10V ③ P-Channel I_D = -2.3A, V_{DS} = -10V, V_{GS} = -10V
		P-Ch	—	11	25		
Q_{gs}	Gate-to-Source Charge	N-Ch	—	1.2	—		
		P-Ch	—	1.6	—		
Q_{gd}	Gate-to-Drain ("Miller") Charge	N-Ch	—	2.5	—		
		P-Ch	—	3.5	—		
$t_{d(on)}$	Turn-On Delay Time	N-Ch	—	5.0	15	ns	N-Channel V_{DD} = 20V, I_D = 1.0A, R_G = 6.0Ω, R_D = 20Ω ③ P-Channel V_{DD} = -20V, I_D = -1.0A, R_G = 6.0Ω, R_D = 20Ω
		P-Ch	—	10	40		
t_r	Rise Time	N-Ch	—	10	20		
		P-Ch	—	15	40		
$t_{d(off)}$	Turn-Off Delay Time	N-Ch	—	29	50		
		P-Ch	—	41	90		
t_f	Fall Time	N-Ch	—	22	50		
		P-Ch	—	39	60		
L_D	Internal Drain Inductace	N-P	—	4.0	—	nH	Between lead tip and center of die contact
L_S	Internal Source Inductance	N-P	—	6.0	—		
C_{iss}	Imput Capacitance	N-Ch	—	300	—	pF	N-Channel V_{GS} = 0V, V_{DS} = 15V, f = 1.0MHz ③ P-Channel V_{GS} = 0V, V_{DS} = -15V, f = 1.0MHz
		P-Ch	—	280	—		
	C_{oss} Output Capacitance	N-Ch	—	260	—		
		P-Ch	—	250	—		
C_{rss}	Reverse Transfer Capacitance	N-Ch	—	62	—		
		P-Ch	—	86	—		

Source-Drain Ratings and Characteristics

	Parameter		Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	N-Ch	—	—	1.7	A	
		P-Ch	—	—	-1.6		
I_{SM}	Pulsed Source Current (Body Diode) ①	N-Ch	—	—	10		
		P-Ch	—	—	-10		
V_{SD}	Diode Forward Voltage	N-Ch	—	0.90	1.2	V	T_J = 25°C, I_S = 1.6A, V_{GS} = 0V ③
		P-Ch	—	-0.90	-1.6		T_J = 25°C, I_S = -1.3A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	N-Ch	—	69	100	ns	N-Channel T_J = 25°C, I_F = 1.25A, di/dt = 100A/µs P-Channel ③ T_J = 25°C, I_F = -1.25A, di/dt = 100A/µs
		P-Ch	—	69	100		
Q_{rr}	Reverse Recovery Charge	N-Ch	—	58	120	nC	
		P-Ch	—	91	180		
t_{on}	Forward Turn-On Time	N-P	Intrinsic turn-on time is neglegible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 23)

② N-Channel I_{SD} ≤ 2.3A, di/dt ≤ 100A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 150°C
P-Channel I_{SD} ≤ -2.3A, di/dt ≤ 50A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 150°C

③ Pulse width ≤ 300µs; duty cycle ≤ 2%.

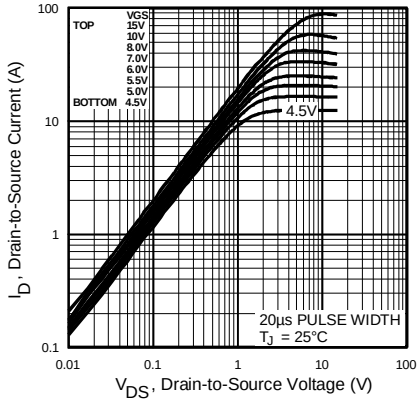


Fig 1. Typical Output Characteristics, $T_J = 25^oC$

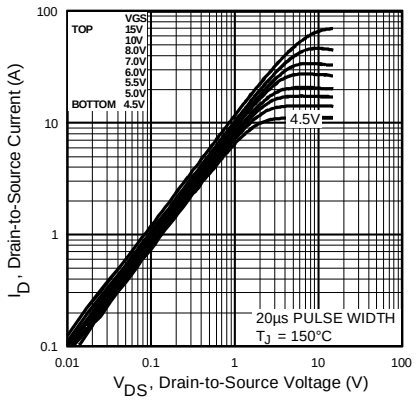


Fig 2. Typical Output Characteristics, $T_J = 150^oC$

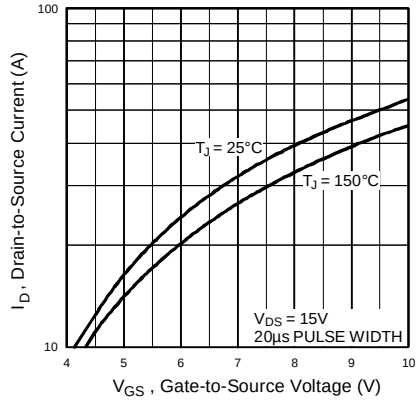


Fig 3. Typical Transfer Characteristics

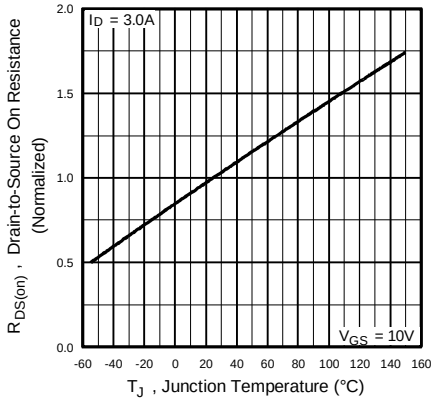


Fig 4. Normalized On-Resistance Vs. Temperature

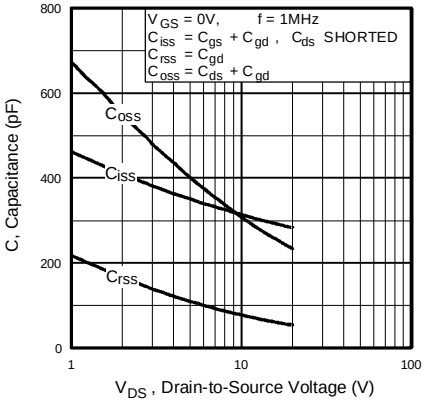


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

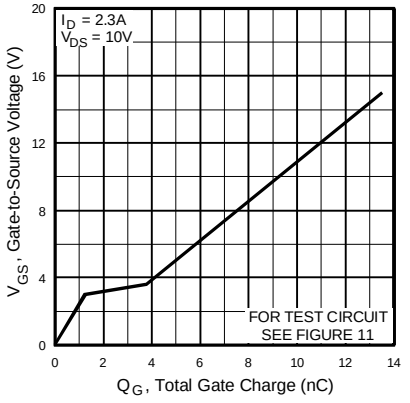


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

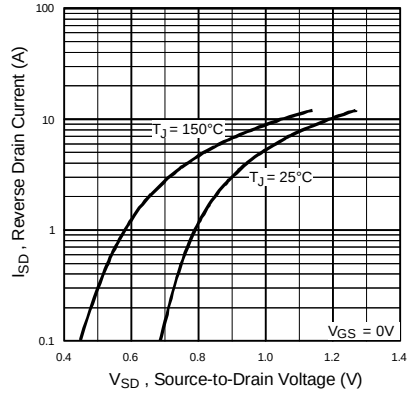


Fig 7. Typical Source-Drain Diode Forward Voltage

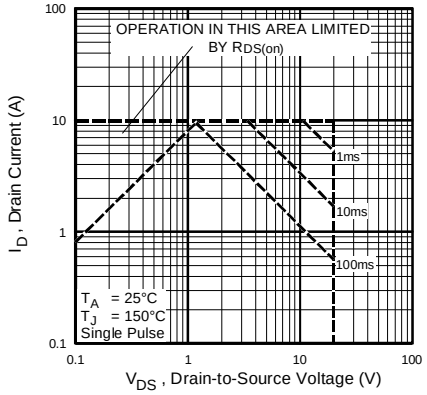


Fig 8. Maximum Safe Operating Area

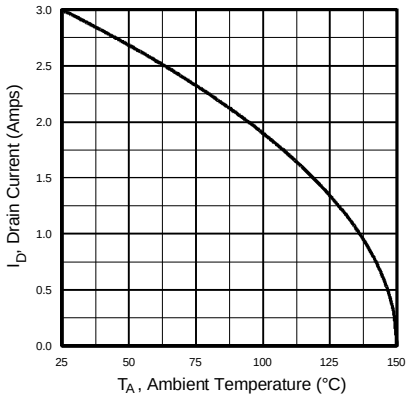


Fig 9. Maximum Drain Current Vs. Ambient Temperature

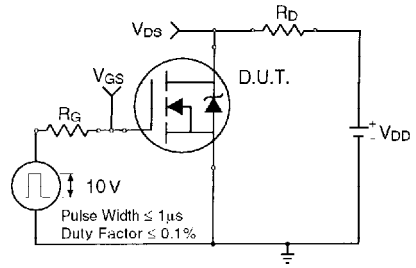


Fig 10a. Switching Time Test Circuit

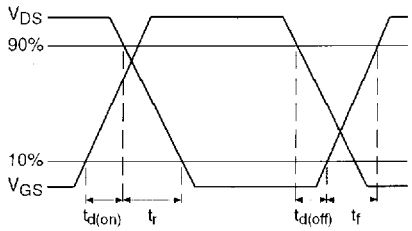


Fig 10b. Switching Time Waveforms

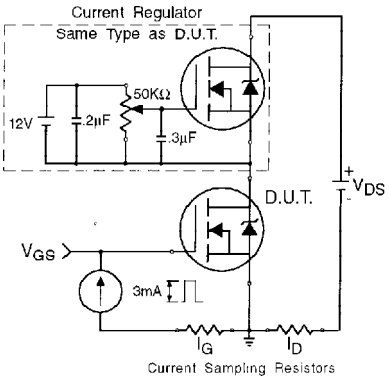


Fig 11a. Gate Charge Test Circuit

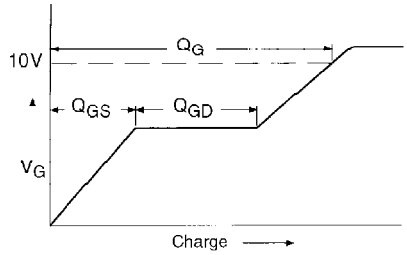


Fig 11b. Basic Gate Charge Waveform

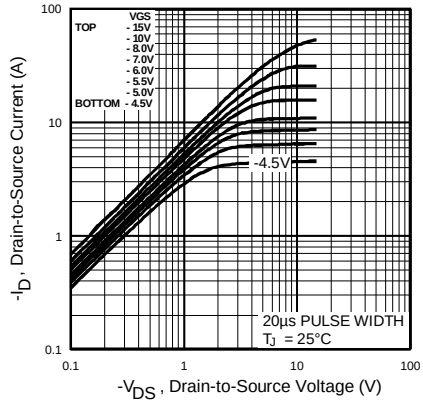


Fig 12. Typical Output Characteristics, $T_J = 25^oC$

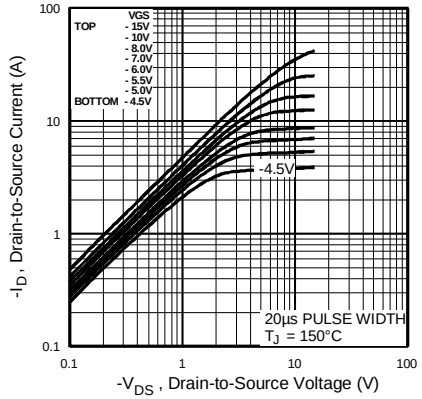


Fig 13. Typical Output Characteristics, $T_J = 150^oC$

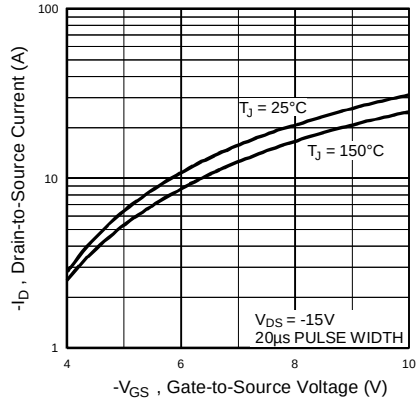


Fig 14. Typical Transfer Characteristics

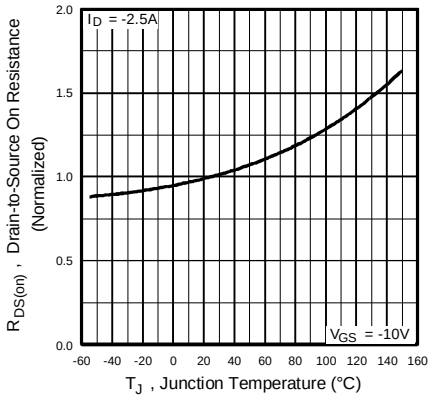


Fig 15. Normalized On-Resistance Vs. Temperature

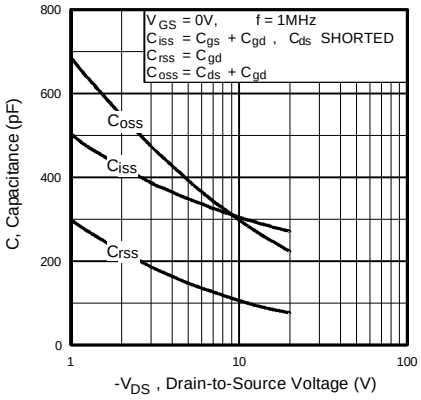


Fig 16. Typical Capacitance Vs. Drain-to-Source Voltage

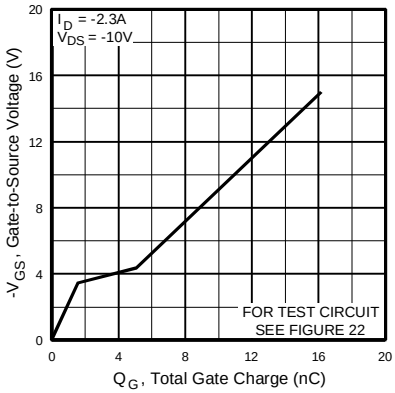


Fig 17. Typical Gate Charge Vs. Gate-to-Source Voltage

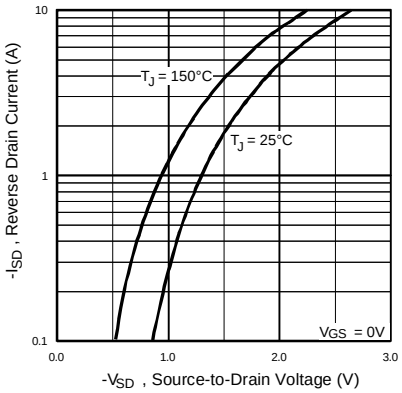


Fig 18. Typical Source-Drain Diode Forward Voltage

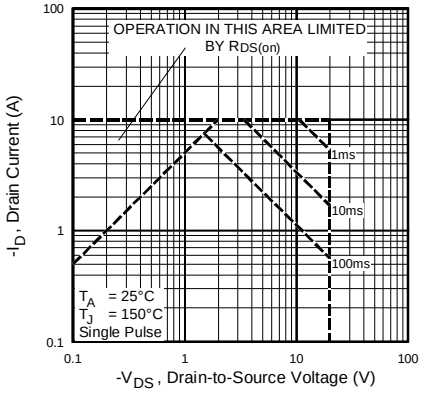


Fig 19. Maximum Safe Operating Area

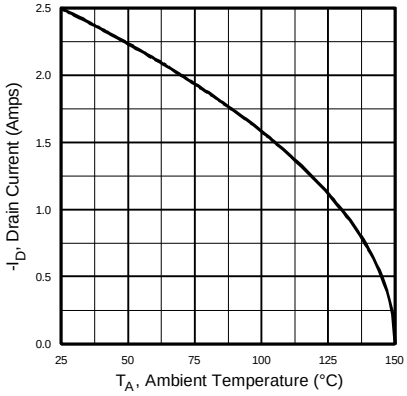


Fig 20. Maximum Drain Current Vs. Ambient Temperature

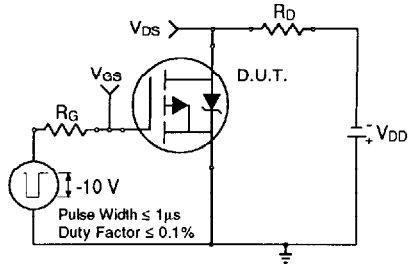


Fig 21a. Switching Time Test Circuit

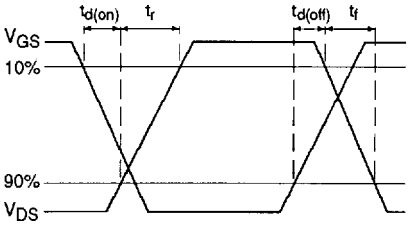


Fig 21b. Switching Time Waveforms

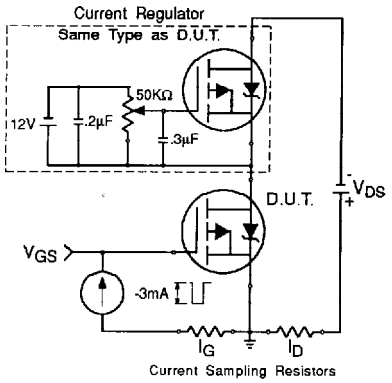


Fig 22a. Gate Charge Test Circuit

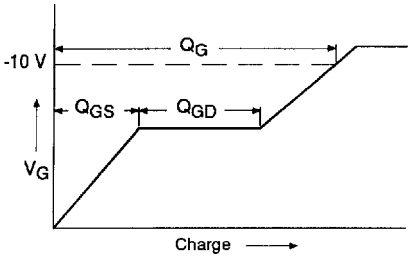


Fig 22b. Basic Gate Charge Waveform

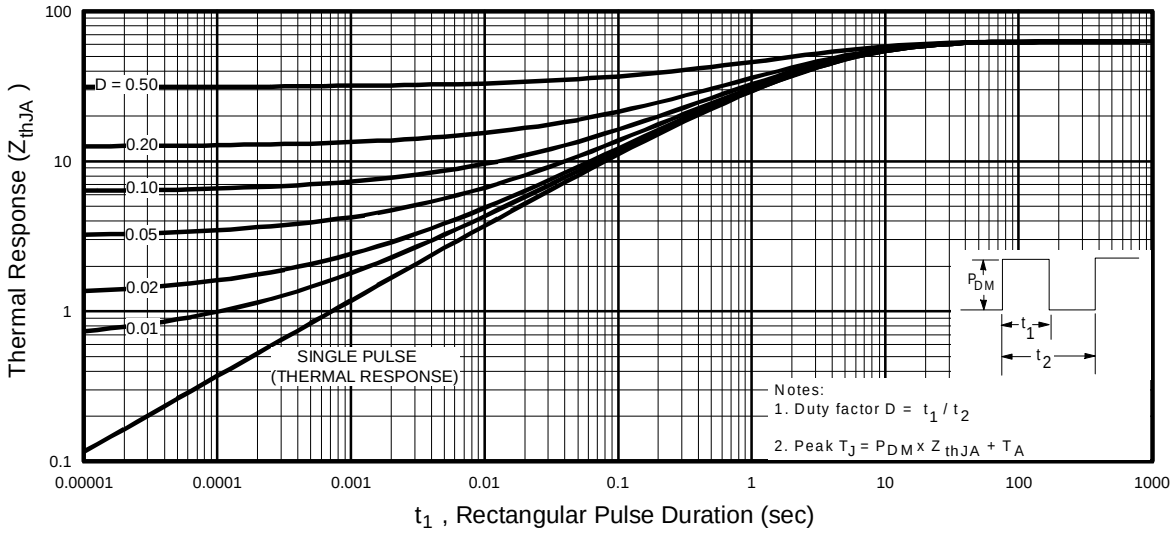


Fig 23. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

Refer to the Appendix Section for the following:

Appendix A: Figure 24, Peak Diode Recovery dv/dt Test Circuit — See page 329.

Appendix B: Package Outline Mechanical Drawing — See page 332.

Appendix C: Part Marking Information — See page 332.

Appendix D: Tape and Reel Information — See page 336.