

# 74LV4053

Triple single-pole double-throw analog switch

Rev. 9 — 2 April 2024

Product data sheet

## 1. General description

The 74LV4053 is a triple single-pole double-throw (SPDT) analog switch, suitable for use in 2:1 multiplexer/demultiplexer applications. Each switch features a digital select input ( $S_n$ ), two independent inputs/outputs ( $Y_0$  and  $Y_1$ ) and a common input/output ( $Z$ ). A digital enable input ( $\bar{E}$ ) is common to all switches. When  $\bar{E}$  is HIGH, the switches are turned off.

Digital inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess  $V_{CC}$ .

## 2. Features and benefits

- Wide supply voltage range from 1.0 V to 6.0 V
- Optimized for low-voltage applications: 1.0 V to 3.6 V
- CMOS low power dissipation
- Accepts TTL input levels between  $V_{CC} = 2.7$  V and  $V_{CC} = 3.6$  V
- Low ON resistance:
  - 180  $\Omega$  (typical) at  $V_{CC} - V_{EE} = 2.0$  V
  - 100  $\Omega$  (typical) at  $V_{CC} - V_{EE} = 3.0$  V
  - 75  $\Omega$  (typical) at  $V_{CC} - V_{EE} = 4.5$  V
- Logic level translation:
  - To enable 3 V logic to communicate with  $\pm 3$  V analog signals
  - Typical 'break before make' built in
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8C (2.7 V to 3.6 V)
  - JESD36 (4.6 V to 5.5 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

**nexperia**

### 3. Ordering information

Table 1. Ordering information

Type number	Package				Version
	Temperature range	Name	Description		
74LV4053D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm		<a href="#">SOT109-1</a>
74LV4053PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm		<a href="#">SOT403-1</a>
74LV4053BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm		<a href="#">SOT763-1</a>

### 4. Functional diagram

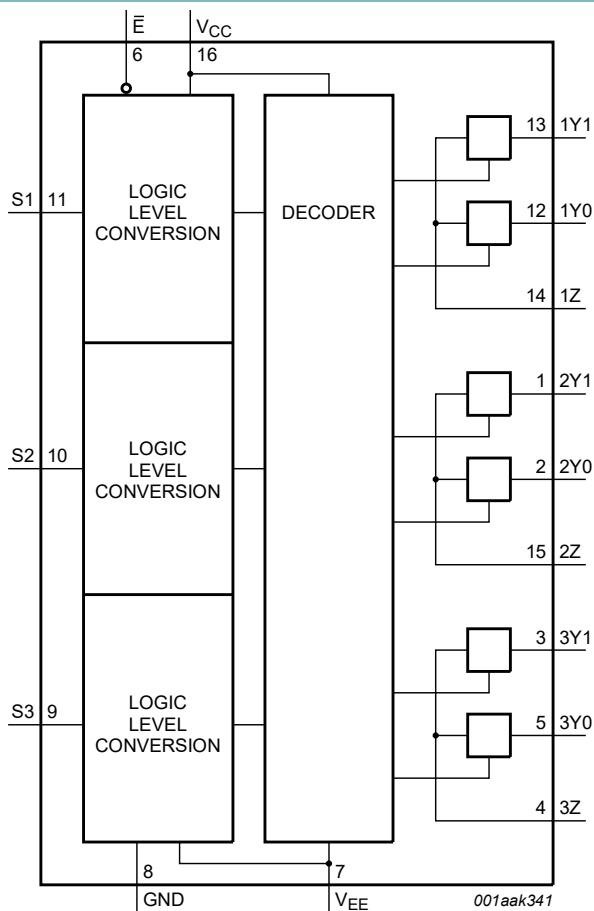


Fig. 1. Functional diagram

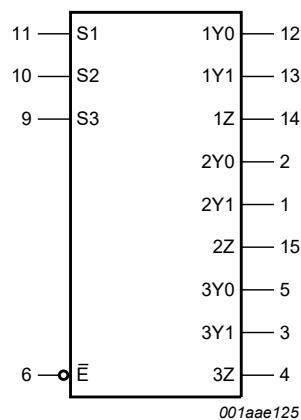


Fig. 2. Logic symbol

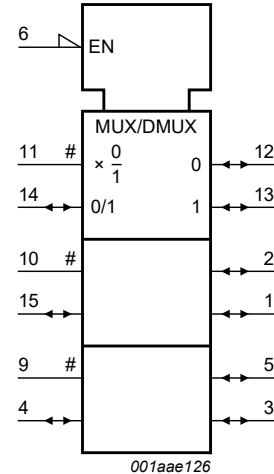


Fig. 3. IEC logic symbol

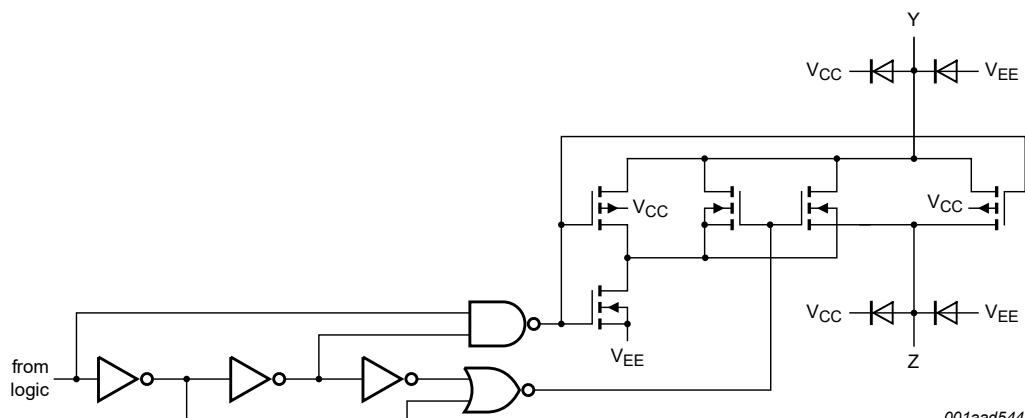
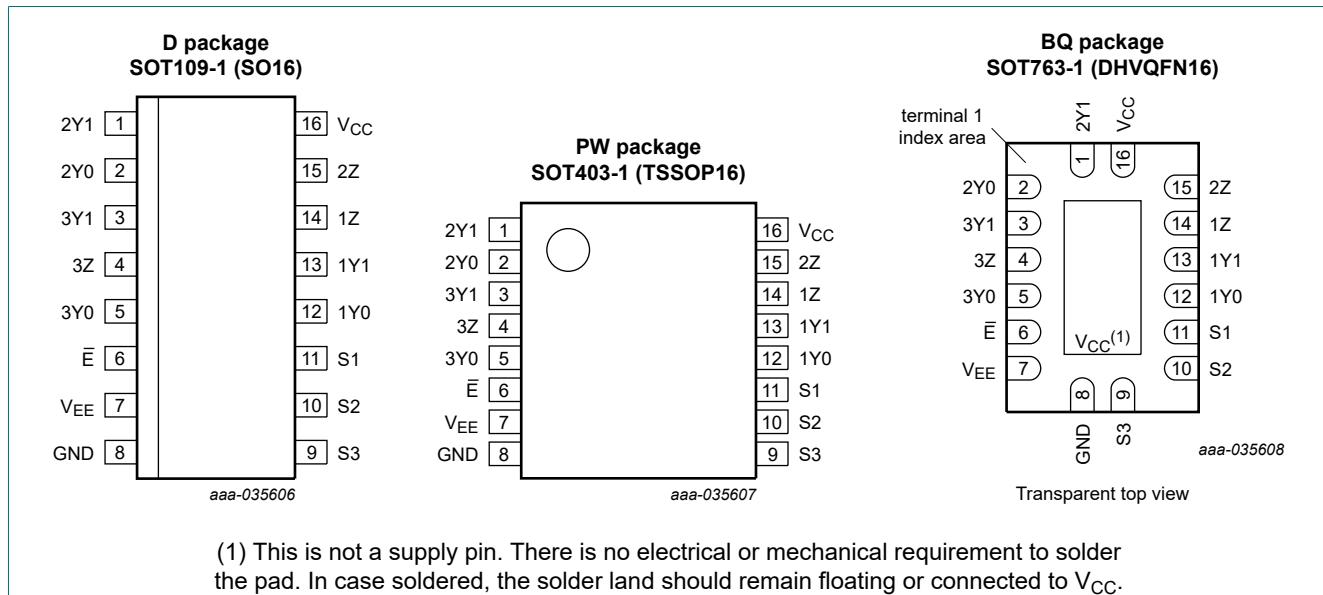


Fig. 4. Schematic diagram (one switch)

## 5. Pinning information

### 5.1. Pinning



### 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
E	6	enable input (active LOW)
V <sub>EE</sub>	7	supply voltage
GND	8	ground supply voltage
S1, S2, S3	11, 10, 9	select input
1Y0, 2Y0, 3Y0	12, 2, 5	independent input or output
1Y1, 2Y1, 3Y1	13, 1, 3	independent input or output
1Z, 2Z, 3Z	14, 15, 4	common output or input
V <sub>CC</sub>	16	supply voltage

## 6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Inputs	Sn	Channel on
E		
L	L	nY0 to nZ
L	H	nY1 to nZ
H	X	switches off

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to  $V_{SS} = 0$  V (ground).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		[1]	-0.5	+7.0
$I_{IK}$	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	[2]	-	$\pm 20$ mA
$I_{SK}$	switch clamping current	$V_{SW} < -0.5$ V or $V_{SW} > V_{CC} + 0.5$ V	[2]	-	$\pm 20$ mA
$I_{SW}$	switch current	$V_{SW} > -0.5$ V or $V_{SW} < V_{CC} + 0.5$ V; source or sink current	[2]	-	$\pm 25$ mA
$T_{stg}$	storage temperature			-65	+150 °C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C	[3]	-	500 mW

[1] To avoid drawing  $V_{CC}$  current out of terminal nZ, when switch current flows into terminals nYn, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal nZ, no  $V_{CC}$  current will flow out of terminals nYn, and in this case there is no limit for the voltage drop across the switch, but the voltages at nYn and nZ may not exceed  $V_{CC}$  or  $V_{EE}$ .

[2] The minimum input voltage rating may be exceeded if the input current rating is observed.

[3] For SOT109-1 (SO16) package:  $P_{tot}$  derates linearly with 12.4 mW/K above 110 °C.

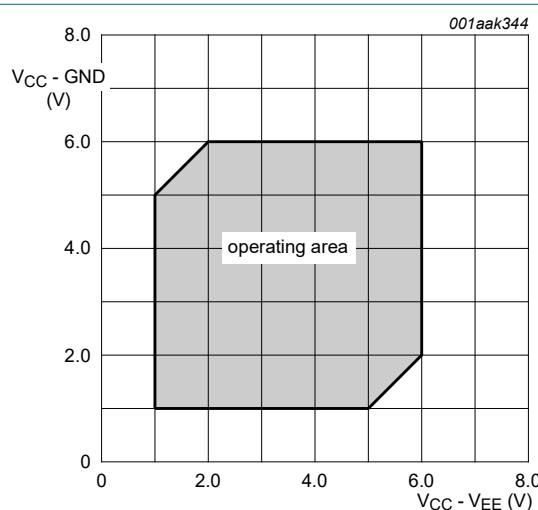
For SOT403-1 (TSSOP16) package:  $P_{tot}$  derates linearly with 8.5 mW/K above 91 °C.

For SOT763-1 (DHVQFN16) package:  $P_{tot}$  derates linearly with 11.2 mW/K above 106 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage	see Fig. 5	1	3.3	6	V
$V_I$	input voltage		0	-	$V_{CC}$	V
$V_{SW}$	switch voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature	in free air	-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.0$ V to 2.0 V	-	-	500	ns/V
		$V_{CC} = 2.0$ V to 2.7 V	-	-	200	ns/V
		$V_{CC} = 2.7$ V to 3.6 V	-	-	100	ns/V



**Fig. 5. Guaranteed operating area as a function of the supply voltages**

## 9. Static characteristics

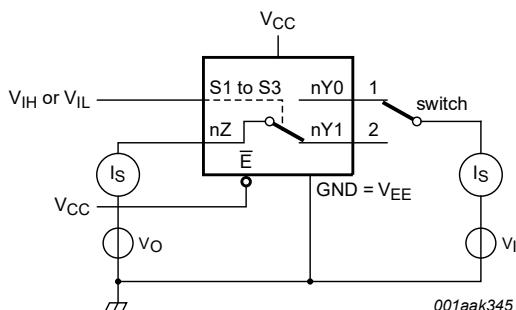
**Table 6. Static characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.2 V	0.9	-	-	0.9	-	V
		V <sub>CC</sub> = 2.0 V	1.4	-	-	1.4	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V <sub>CC</sub> = 4.5 V	3.15	-	-	3.15	-	V
		V <sub>CC</sub> = 6.0 V	4.20	-	-	4.20	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.2 V	-	-	0.3	-	0.3	V
		V <sub>CC</sub> = 2.0 V	-	-	0.6	-	0.6	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V <sub>CC</sub> = 4.5 V	-	-	1.35	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	-	1.80	-	1.80	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND						
		V <sub>CC</sub> = 3.6 V	-	-	1.0	-	1.0	µA
		V <sub>CC</sub> = 6.0 V	-	-	2.0	-	2.0	µA
I <sub>S(OFF)</sub>	OFF-state leakage current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; see Fig. 6						
		V <sub>CC</sub> = 3.6 V	-	-	1.0	-	1.0	µA
		V <sub>CC</sub> = 6.0 V	-	-	2.0	-	2.0	µA
I <sub>S(ON)</sub>	ON-state leakage current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; see Fig. 7						
		V <sub>CC</sub> = 3.6 V	-	-	1.0	-	1.0	µA
		V <sub>CC</sub> = 6.0 V	-	-	2.0	-	2.0	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A						
		V <sub>CC</sub> = 3.6 V	-	-	20	-	40	µA
		V <sub>CC</sub> = 6.0 V	-	-	40	-	80	µA
ΔI <sub>CC</sub>	additional supply current	per input; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	500	-	850	µA
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	pF
C <sub>sw</sub>	switch capacitance	independent pins nYn	-	5	-	-	-	pF
		common pins nZ	-	8	-	-	-	pF

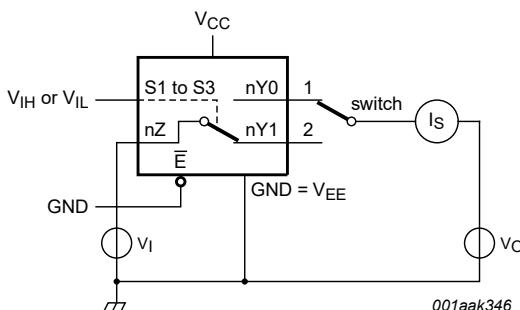
[1] Typical values are measured at T<sub>amb</sub> = 25 °C.

## 9.1. Test circuits



$V_I = V_{CC}$  or  $V_{EE}$  and  $V_O = V_{EE}$  or  $V_{CC}$ .

Fig. 6. Test circuit for measuring OFF-state leakage current



$V_I = V_{CC}$  or  $V_{EE}$  and  $V_O = \text{open circuit}$ .

Fig. 7. Test circuit for measuring ON-state leakage current

## 9.2. ON resistance

**Table 7. ON resistance**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for graphs see Fig. 8 and Fig. 9.

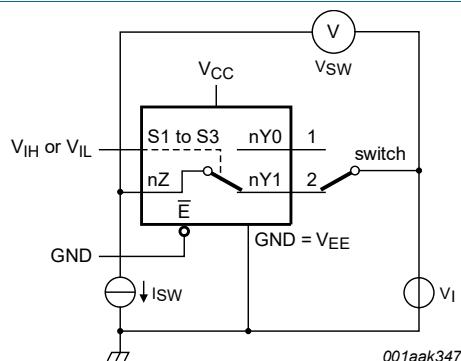
Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
R <sub>ON(peak)</sub>	ON resistance (peak)	V <sub>I</sub> = 0 V to V <sub>CC</sub> - V <sub>EE</sub>						
		V <sub>CC</sub> = 1.2 V; I <sub>SW</sub> = 100 µA [2]	-	-	-	-	-	Ω
		V <sub>CC</sub> = 2.0 V; I <sub>SW</sub> = 1000 µA	-	180	365	-	435	Ω
		V <sub>CC</sub> = 2.7 V; I <sub>SW</sub> = 1000 µA	-	115	225	-	270	Ω
		V <sub>CC</sub> = 3.0 V to 3.6 V; I <sub>SW</sub> = 1000 µA	-	100	200	-	245	Ω
		V <sub>CC</sub> = 4.5 V; I <sub>SW</sub> = 1000 µA	-	75	150	-	180	Ω
		V <sub>CC</sub> = 6.0 V; I <sub>SW</sub> = 1000 µA	-	70	140	-	165	Ω
ΔR <sub>ON</sub>	ON resistance mismatch between channels	V <sub>I</sub> = 0 V to V <sub>CC</sub> - V <sub>EE</sub>						
		V <sub>CC</sub> = 1.2 V; I <sub>SW</sub> = 100 µA [2]	-	-	-	-	-	Ω
		V <sub>CC</sub> = 2.0 V; I <sub>SW</sub> = 1000 µA	-	5	-	-	-	Ω
		V <sub>CC</sub> = 2.7 V; I <sub>SW</sub> = 1000 µA	-	4	-	-	-	Ω
		V <sub>CC</sub> = 3.0 V to 3.6 V; I <sub>SW</sub> = 1000 µA	-	4	-	-	-	Ω
		V <sub>CC</sub> = 4.5 V; I <sub>SW</sub> = 1000 µA	-	3	-	-	-	Ω
		V <sub>CC</sub> = 6.0 V; I <sub>SW</sub> = 1000 µA	-	2	-	-	-	Ω
R <sub>ON(rail)</sub>	ON resistance (rail)	V <sub>I</sub> = GND						
		V <sub>CC</sub> = 1.2 V; I <sub>SW</sub> = 100 µA [2]	-	250	-	-	-	Ω
		V <sub>CC</sub> = 2.0 V; I <sub>SW</sub> = 1000 µA	-	120	280	-	325	Ω
		V <sub>CC</sub> = 2.7 V; I <sub>SW</sub> = 1000 µA	-	75	170	-	195	Ω
		V <sub>CC</sub> = 3.0 V to 3.6 V; I <sub>SW</sub> = 1000 µA	-	70	155	-	180	Ω
		V <sub>CC</sub> = 4.5 V; I <sub>SW</sub> = 1000 µA	-	50	120	-	135	Ω
		V <sub>CC</sub> = 6.0 V; I <sub>SW</sub> = 1000 µA	-	45	105	-	120	Ω

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
$R_{ON(rail)}$	ON resistance (rail)	$V_I = V_{CC} - V_{EE}$						
		$V_{CC} = 1.2 \text{ V}; I_{SW} = 100 \mu\text{A}$ [2]	-	350	-	-	-	$\Omega$
		$V_{CC} = 2.0 \text{ V}; I_{SW} = 1000 \mu\text{A}$	-	170	340	-	400	$\Omega$
		$V_{CC} = 2.7 \text{ V}; I_{SW} = 1000 \mu\text{A}$	-	105	210	-	250	$\Omega$
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}; I_{SW} = 1000 \mu\text{A}$	-	95	190	-	225	$\Omega$
		$V_{CC} = 4.5 \text{ V}; I_{SW} = 1000 \mu\text{A}$	-	70	140	-	165	$\Omega$
		$V_{CC} = 6.0 \text{ V}; I_{SW} = 1000 \mu\text{A}$	-	65	125	-	150	$\Omega$

[1] Typical values are measured at  $T_{amb} = 25 \text{ °C}$ .

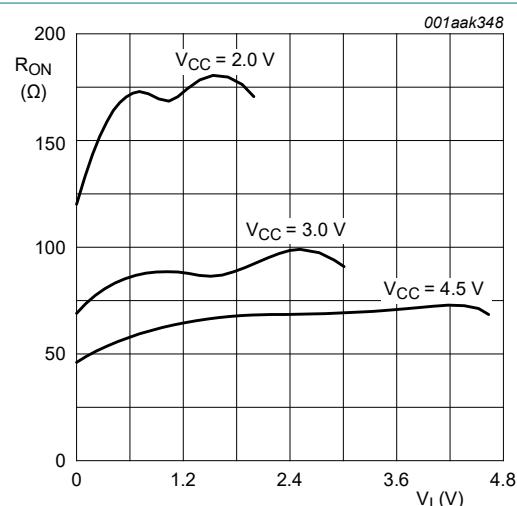
[2] When supply voltages ( $V_{CC} - V_{EE}$ ) near 1.2 V the analog switch ON resistance becomes extremely non-linear. When using a supply of 1.2 V, it is recommended to use these devices only for transmitting digital signals.

### 9.3. On resistance waveform and test circuit



$$R_{ON} = V_{SW} / I_{SW}$$

Fig. 8. Test circuit for measuring  $R_{ON}$



$$V_I = 0 \text{ V to } V_{CC} - V_{EE}$$

Fig. 9. Typical  $R_{ON}$  as a function of input voltage

## 10. Dynamic characteristics

**Table 8. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V). For test circuit see [Fig. 12](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit	
			Min	Typ[1]	Max	Min	Max		
t <sub>pd</sub>	propagation delay	nYn, nZ to nZ, nYn; see <a href="#">Fig. 10</a>	[2]						
		V <sub>CC</sub> = 1.2 V	-	25	-	-	-	ns	
		V <sub>CC</sub> = 2.0 V	-	9	17	-	20	ns	
		V <sub>CC</sub> = 2.7 V	-	6	13	-	15	ns	
		V <sub>CC</sub> = 3.0 V to 3.6 V	[3]	-	5	10	-	12	ns
		V <sub>CC</sub> = 4.5 V	-	4	9	-	10	ns	
		V <sub>CC</sub> = 6.0 V	-	3	7	-	8	ns	
t <sub>en</sub>	enable time	E to nYn, nZ; see <a href="#">Fig. 11</a>	[2]						
		V <sub>CC</sub> = 1.2 V	-	100	-	-	-	ns	
		V <sub>CC</sub> = 2.0 V	-	34	65	-	77	ns	
		V <sub>CC</sub> = 2.7 V	-	25	48	-	56	ns	
		V <sub>CC</sub> = 3.0 V to 3.6 V; C <sub>L</sub> = 15 pF	[3]	-	16	-	-	ns	
		V <sub>CC</sub> = 3.0 V to 3.6 V	[3]	-	19	38	-	45	ns
		V <sub>CC</sub> = 4.5 V	-	17	32	-	38	ns	
		V <sub>CC</sub> = 6.0 V	-	13	25	-	29	ns	
		Sn to nYn, nZ; see <a href="#">Fig. 11</a>	[2]						
		V <sub>CC</sub> = 1.2 V	-	125	-	-	-	ns	
		V <sub>CC</sub> = 2.0 V	-	43	82	-	97	ns	
		V <sub>CC</sub> = 2.7 V	-	31	60	-	71	ns	
		V <sub>CC</sub> = 3.0 V to 3.6 V; C <sub>L</sub> = 15 pF	[3]	-	20	-	-	ns	
		V <sub>CC</sub> = 3.0 V to 3.6 V	[3]	-	24	48	-	57	ns
		V <sub>CC</sub> = 4.5 V	-	21	41	-	48	ns	
		V <sub>CC</sub> = 6.0 V	-	16	31	-	37	ns	
t <sub>dis</sub>	disable time	E to nYn, nZ; see <a href="#">Fig. 11</a>	[2]						
		V <sub>CC</sub> = 1.2 V	-	95	-	-	-	ns	
		V <sub>CC</sub> = 2.0 V	-	34	61	-	73	ns	
		V <sub>CC</sub> = 2.7 V	-	26	46	-	54	ns	
		V <sub>CC</sub> = 3.0 V to 3.6 V; C <sub>L</sub> = 15 pF	[3]	-	17	-	-	ns	
		V <sub>CC</sub> = 3.0 V to 3.6 V	[3]	-	20	37	-	44	ns
		V <sub>CC</sub> = 4.5 V	-	18	32	-	38	ns	
		V <sub>CC</sub> = 6.0 V	-	15	25	-	30	ns	
		Sn to nYn, nZ; see <a href="#">Fig. 11</a>	[2]						
		V <sub>CC</sub> = 1.2 V	-	90	-	-	-	ns	
		V <sub>CC</sub> = 2.0 V	-	32	59	-	70	ns	
		V <sub>CC</sub> = 2.7 V	-	24	44	-	52	ns	
		V <sub>CC</sub> = 3.0 V to 3.6 V; C <sub>L</sub> = 15 pF	[3]	-	16	-	-	ns	
		V <sub>CC</sub> = 3.0 V to 3.6 V	[3]	-	19	36	-	42	ns
		V <sub>CC</sub> = 4.5 V	-	17	31	-	36	ns	
		V <sub>CC</sub> = 6.0 V	-	14	24	-	28	ns	

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
$C_{PD}$	power dissipation capacitance	$C_L = 50 \text{ pF}$ ; $f_i = 1 \text{ MHz}$ ; $V_i = \text{GND to } V_{CC}$ [4]	-	36	-	-	-	pF

[1] All typical values are measured at  $T_{amb} = 25 \text{ °C}$ .

[2]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

$t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .

$t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ .

[3] Typical values are measured at nominal supply voltage ( $V_{CC} = 3.3 \text{ V}$ ).

[4]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum((C_L + C_{SW}) \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz,  $f_o$  = output frequency in MHz

$C_L$  = output load capacitance in pF

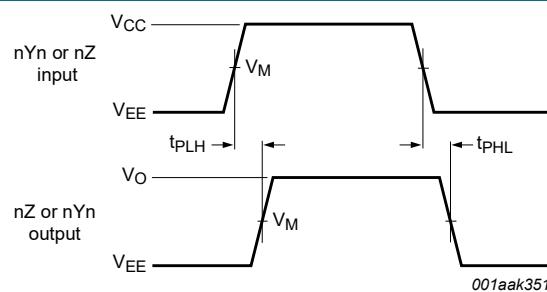
$C_{SW}$  = maximum switch capacitance in pF;

$V_{CC}$  = supply voltage in Volts

$N$  = number of inputs switching

$$\sum(C_L \times V_{CC}^2 \times f_o) = \text{sum of the outputs.}$$

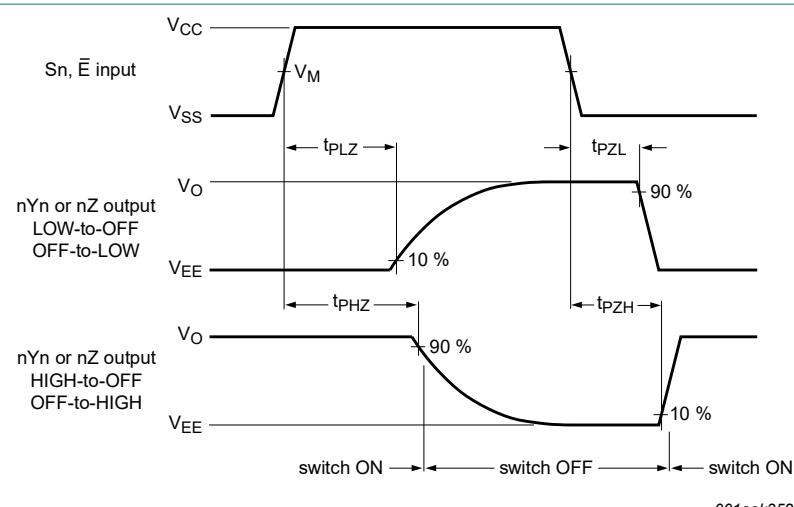
### 10.1. Waveforms and test circuit



Measurement points are given in [Table 9](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

Fig. 10. Propagation delay input (nYn, nZ) to output (nZ, nYn)



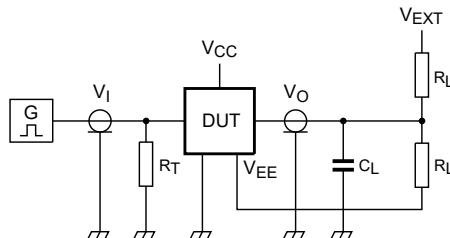
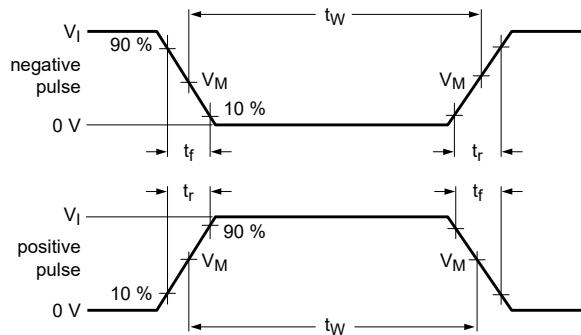
Measurement points are given in [Table 9](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

Fig. 11. Enable and disable times

Table 9. Measurement points

Supply voltage	Input	Output		
$V_{CC}$	$V_M$	$V_M$	$V_X$	$V_Y$
< 2.7 V	0.5 $V_{CC}$	0.5 $V_{CC}$	$V_{OL} + 0.1V_{CC}$	$V_{OH} - 0.1V_{CC}$
2.7 V to 3.6 V	1.5 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$
> 3.6 V	0.5 $V_{CC}$	0.5 $V_{CC}$	$V_{OL} + 0.1V_{CC}$	$V_{OH} - 0.1V_{CC}$



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Test data is given in [Table 10](#).

Definitions for test circuit:

 $R_L$  = Load resistance. $C_L$  = Load capacitance including jig and probe capacitance. $R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator. $V_{EXT}$  = External voltage for measuring switching times.

Fig. 12. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input	Load		$V_{EXT}$				
$V_{CC}$	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$	
< 2.7 V	$V_{CC}$	$\leq 6$ ns	50 pF	1 k $\Omega$	open	$V_{EE}$	$2V_{CC}$	
2.7 V to 3.6 V	2.7 V	$\leq 6$ ns	15 pF, 50 pF	1 k $\Omega$	open	$V_{EE}$	$2V_{CC}$	
> 3.6 V	$V_{CC}$	$\leq 6$ ns	50 pF	1 k $\Omega$	open	$V_{EE}$	$2V_{CC}$	

## 10.2. Additional dynamic parameters

**Table 11. Additional dynamic characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);  $V_I$  = GND or  $V_{CC}$  (unless otherwise specified);  $t_r = t_f \leq 6.0 \text{ ns}$ ;  $T_{amb} = 25^\circ \text{C}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
THD	total harmonic distortion	$f_i = 1 \text{ kHz}$ ; $C_L = 50 \text{ pF}$ ; $R_L = 10 \text{ k}\Omega$ ; see Fig. 13				
		$V_{CC} = 3.0 \text{ V}$ ; $V_I = 2.75 \text{ V}$ (p-p)	-	0.8	-	%
		$V_{CC} = 6.0 \text{ V}$ ; $V_I = 5.5 \text{ V}$ (p-p)	-	0.4	-	%
		$f_i = 10 \text{ kHz}$ ; $C_L = 50 \text{ pF}$ ; $R_L = 10 \text{ k}\Omega$ ; see Fig. 13				
		$V_{CC} = 3.0 \text{ V}$ ; $V_I = 2.75 \text{ V}$ (p-p)	-	2.4	-	%
		$V_{CC} = 6.0 \text{ V}$ ; $V_I = 5.5 \text{ V}$ (p-p)	-	1.2	-	%
$f_{(-3\text{dB})}$	-3 dB frequency response	$C_L = 50 \text{ pF}$ ; $R_L = 50 \Omega$ ; see Fig. 14 [1]				
		$V_{CC} = 3.0 \text{ V}$	-	180	-	MHz
		$V_{CC} = 6.0 \text{ V}$	-	200	-	MHz
$\alpha_{iso}$	isolation (OFF-state)	$f_i = 1 \text{ MHz}$ ; $C_L = 50 \text{ pF}$ ; $R_L = 600 \Omega$ ; see Fig. 16 [2]				
		$V_{CC} = 3.0 \text{ V}$	-	-50	-	dB
		$V_{CC} = 6.0 \text{ V}$	-	-50	-	dB
$V_{ct}$	crosstalk voltage	between digital inputs and switch; $f_i = 1 \text{ MHz}$ ; $C_L = 50 \text{ pF}$ ; $R_L = 600 \Omega$ ; see Fig. 18 [2]				
		$V_{CC} = 3.0 \text{ V}$	-	0.11	-	V
		$V_{CC} = 6.0 \text{ V}$	-	0.12	-	V
Xtalk	crosstalk	between switches; $f_i = 1 \text{ MHz}$ ; $C_L = 50 \text{ pF}$ ; $R_L = 600 \Omega$ ; see Fig. 19				
		$V_{CC} = 3.0 \text{ V}$	-	-60	-	dB
		$V_{CC} = 6.0 \text{ V}$	-	-60	-	dB

[1] Adjust  $f_i$  voltage to obtain 0 dBm level at output for 1 MHz (0 dBm = 1 mW into  $50 \Omega$ ).

[2] Adjust  $f_i$  voltage to obtain 0 dBm level at output for 1 MHz (0 dBm = 1 mW into  $600 \Omega$ ).

### 10.2.1. Test circuits

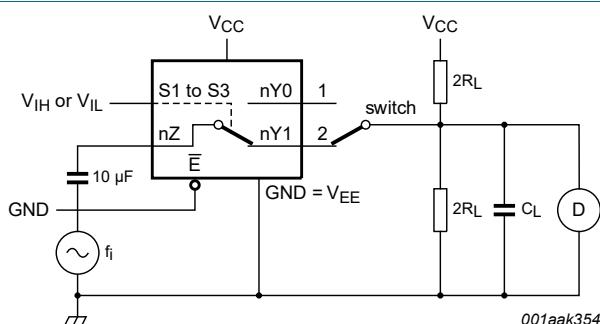


Fig. 13. Test circuit for measuring total harmonic distortion

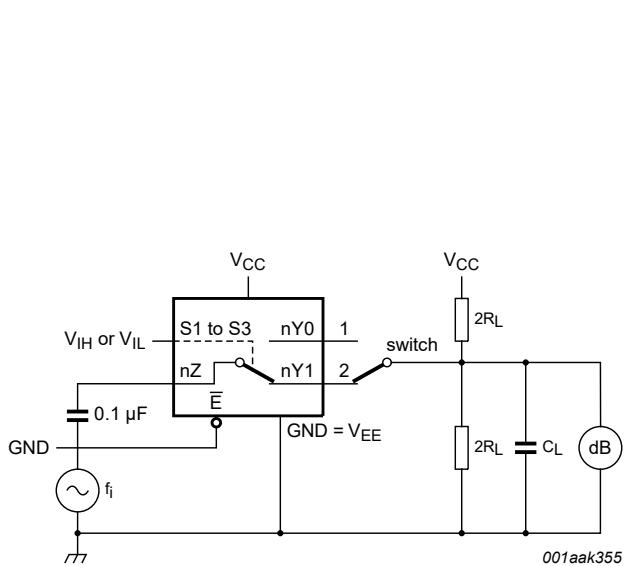


Fig. 14. Test circuit for measuring frequency response

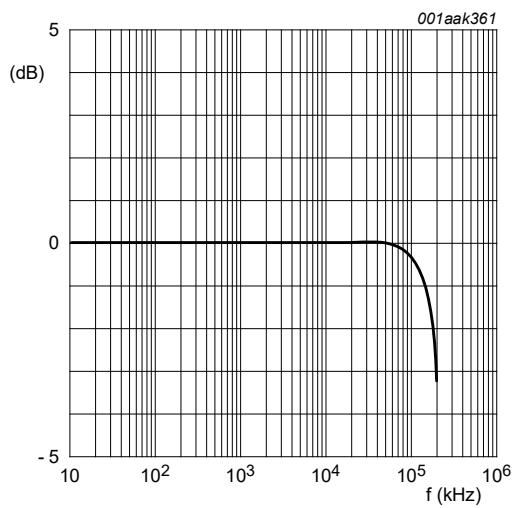


Fig. 15. Typical frequency response

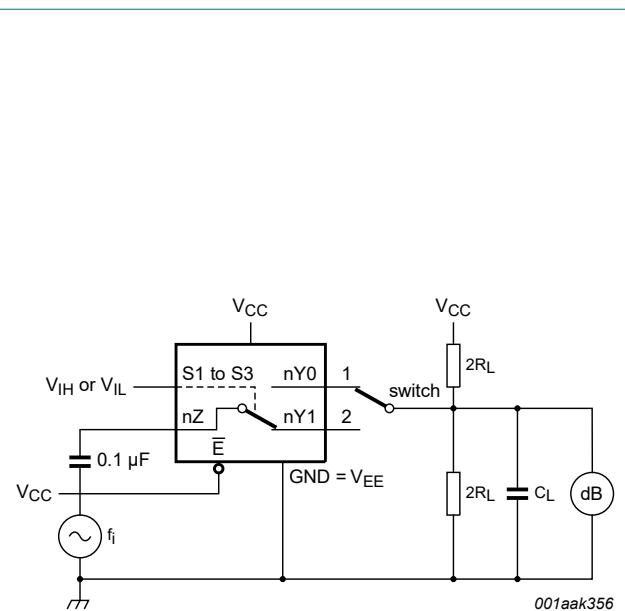


Fig. 16. Test circuit for measuring isolation (OFF-state)

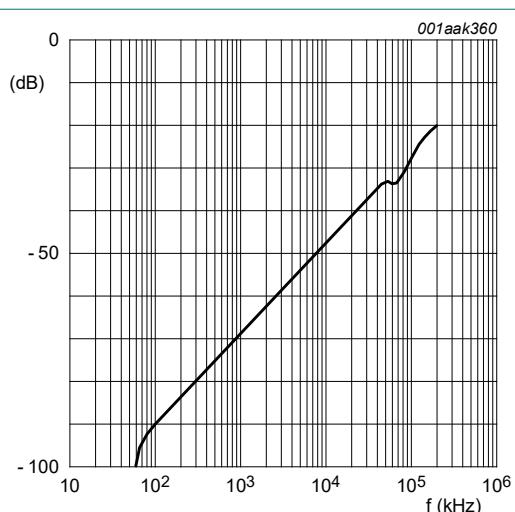
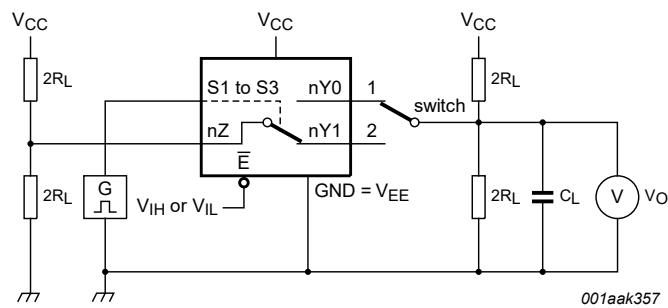
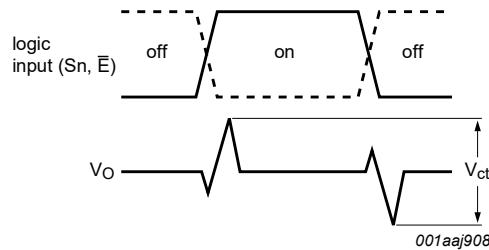


Fig. 17. Typical isolation (OFF-state) as function of frequency

## Triple single-pole double-throw analog switch



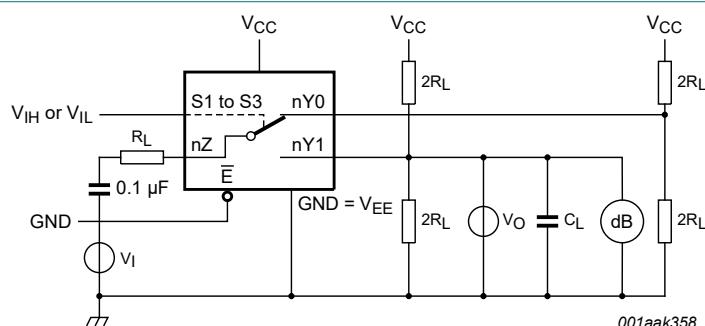
a. Test circuit



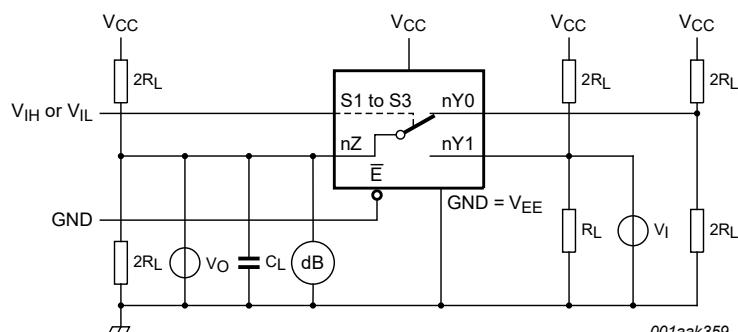
b. Input and output pulse definitions

 $V_I$  may be connected to  $S_n$  or  $\bar{E}$ .

Fig. 18. Test circuit for measuring crosstalk voltage between digital inputs and switch



a. Switch closed condition



b. Switch open condition

Fig. 19. Test circuit for measuring crosstalk between switches

## 11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

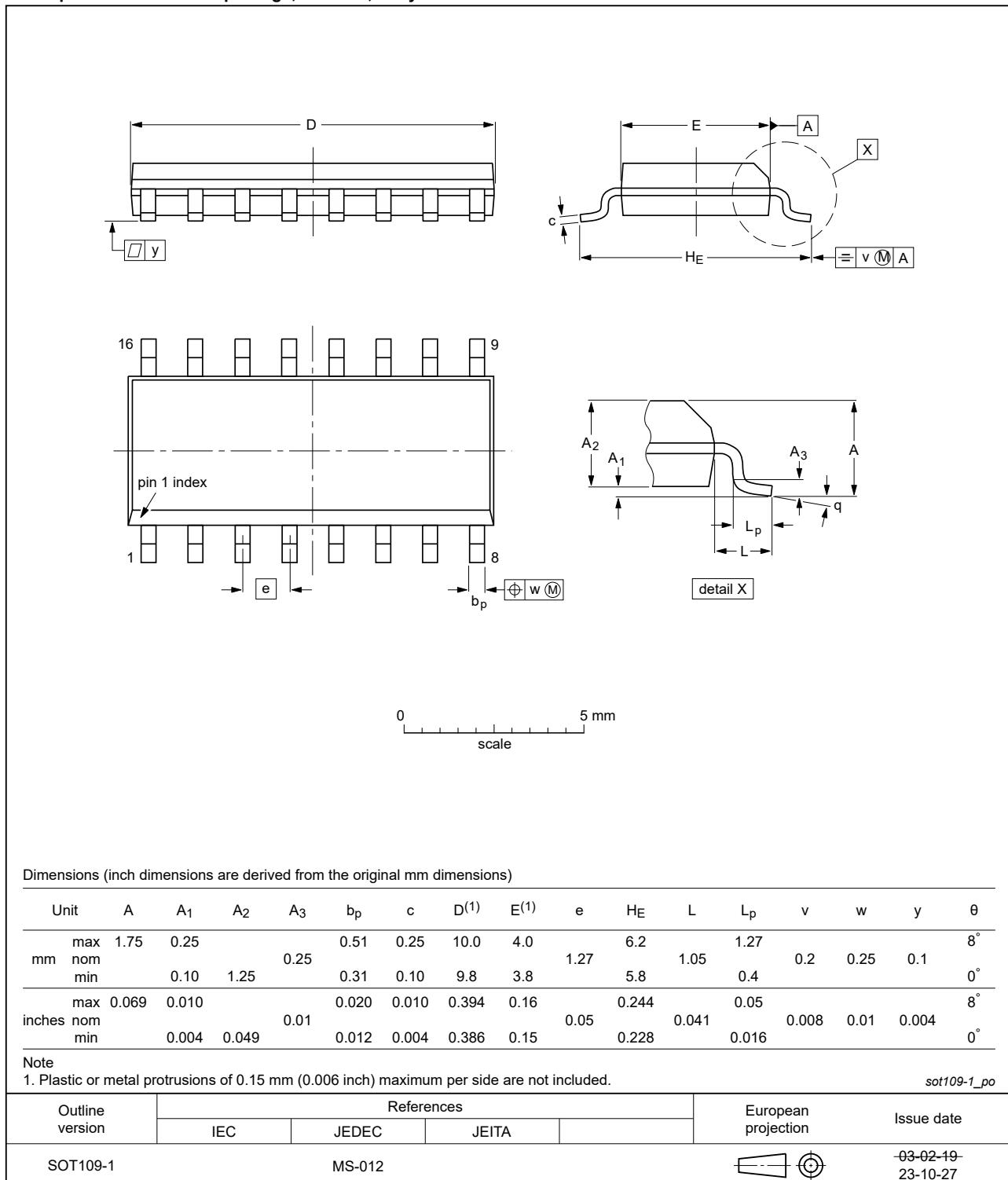


Fig. 20. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

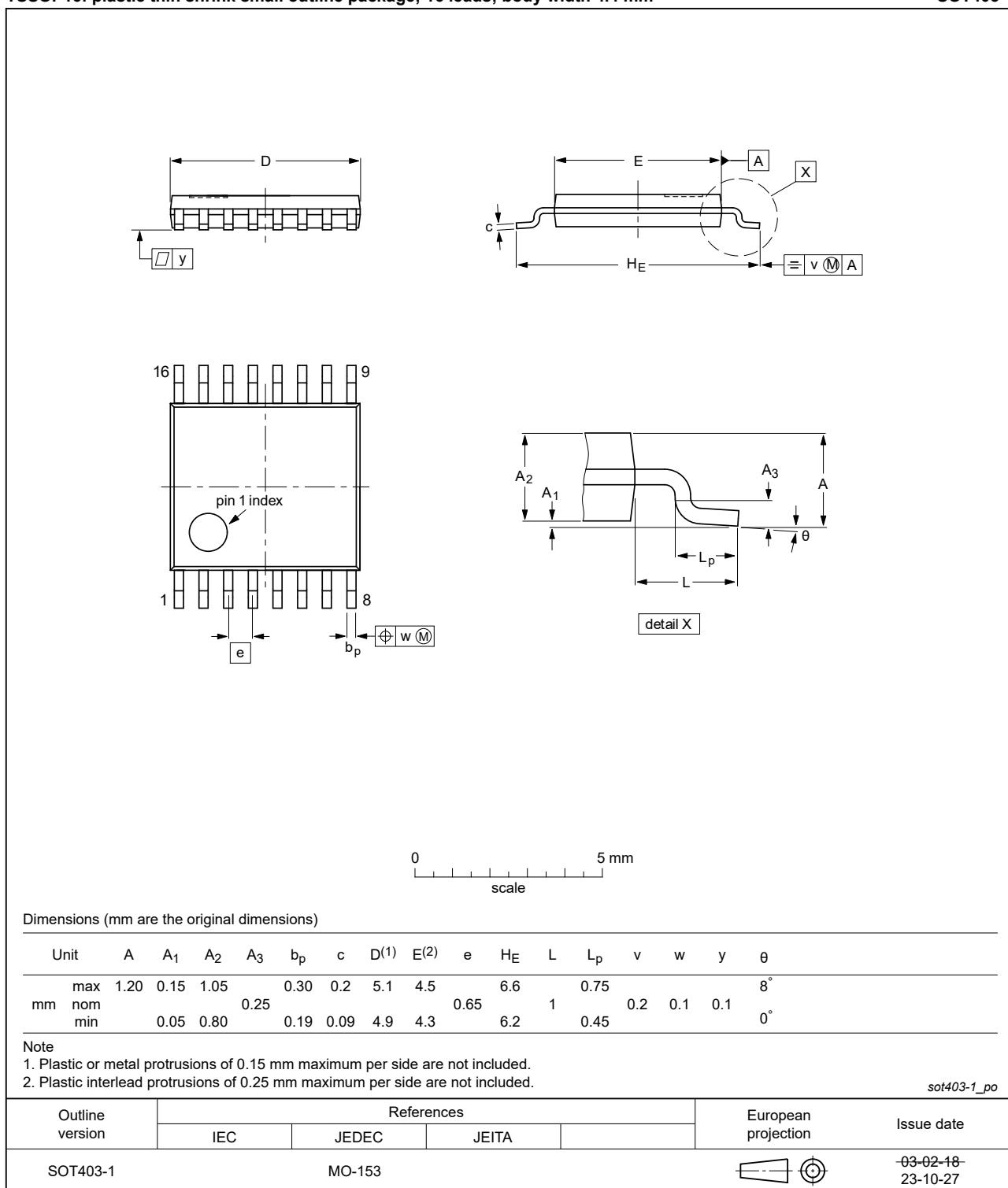


Fig. 21. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;  
16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

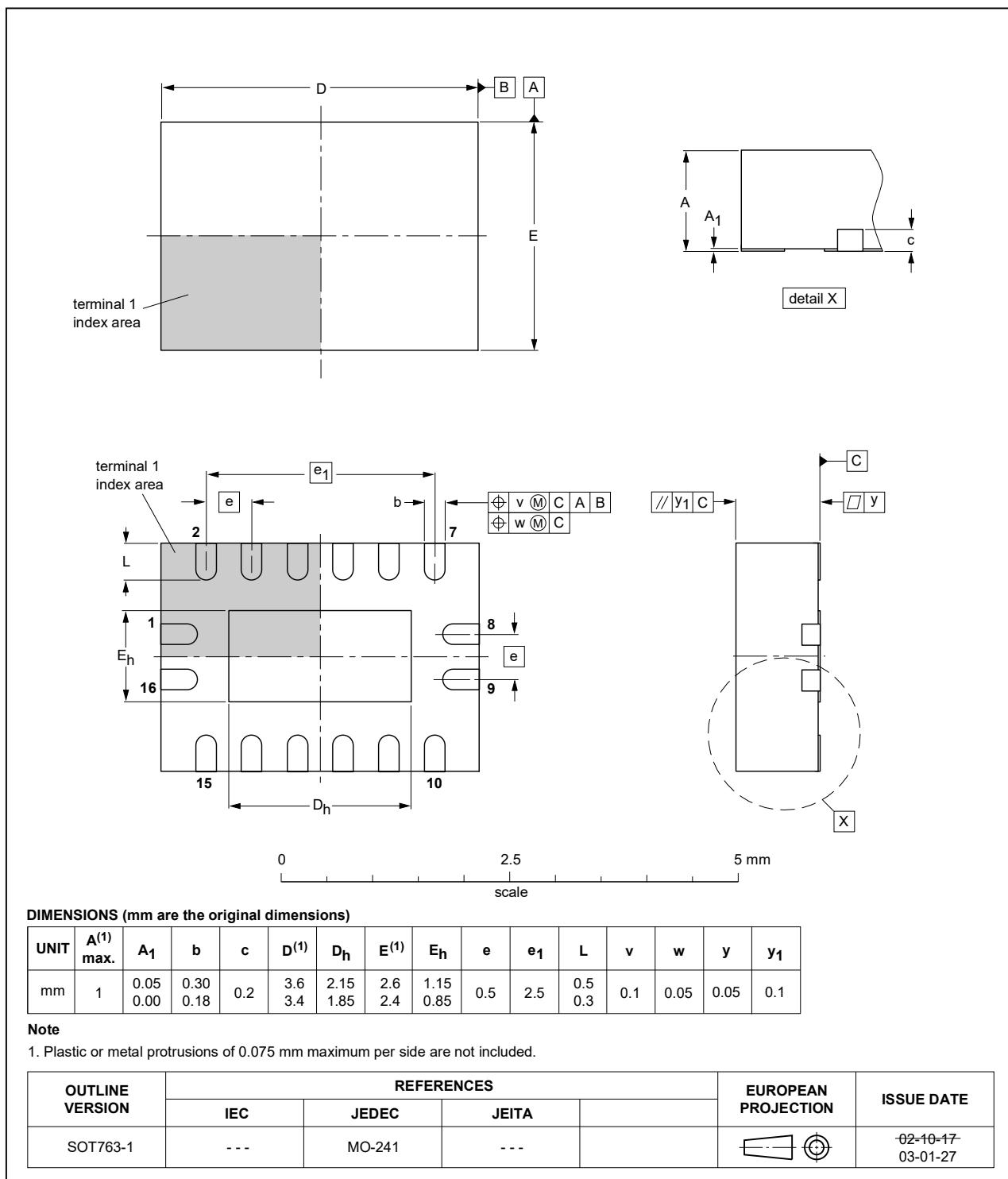


Fig. 22. Package outline SOT763-1 (DHVQFN16)

## 12. Abbreviations

**Table 12. Abbreviations**

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

## 13. Revision history

**Table 13. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV4053 v.9	20240402	Product data sheet	-	74LV4053 v.8
Modifications:				<ul style="list-style-type: none"> <li><a href="#">Section 2</a>: ESD specification updated according to the latest JEDEC standard.</li> <li><a href="#">Fig. 20</a> and <a href="#">Fig. 21</a>: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153.</li> </ul>
74LV4053 v.8	20210915	Product data sheet	-	74LV4053 v.7
Modifications:				<ul style="list-style-type: none"> <li>Type number 74LV4053DB (SOT338-1/SSOP16) removed.</li> <li><a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li> </ul>
74LV4053 v.7	20200923	Product data sheet	-	74LV4053 v.6
Modifications:				<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Table 4</a>: Derating values for <math>P_{tot}</math> total power dissipation updated.</li> </ul>
74LV4053 v.6	20160317	Product data sheet	-	74LV4053 v.5
Modifications:				<ul style="list-style-type: none"> <li>Type number 74LV4053N (SOT38-4) removed.</li> </ul>
74LV4053 v.5	20140918	Product data sheet	-	74LV4053 v.4
Modifications:				<ul style="list-style-type: none"> <li><a href="#">Section 5.1</a>: Figure note added for DHVQFN16 package.</li> </ul>
74LV4053 v.4	20090810	Product data sheet	-	74LV4053 v.3
Modifications:				<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Added type number 74LV4053BQ (DHVQFN16 package)</li> <li><math>R_{ON}</math> values changed in <a href="#">Section 2</a>.</li> <li>Package version SOT38-1 changed to SOT38-4 in <a href="#">Section 5</a>, and <a href="#">Section 11</a>.</li> </ul>
74LV4053 v.3	19980623	Product specification	-	74LV4053 v.2
74LV4053 v.2	19970715	Product specification	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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