

N-channel 60 V, 0.0031 Ω typ., 70 A STripFET™ F7 Power MOSFET in a TO-220FP package

Datasheet - production data

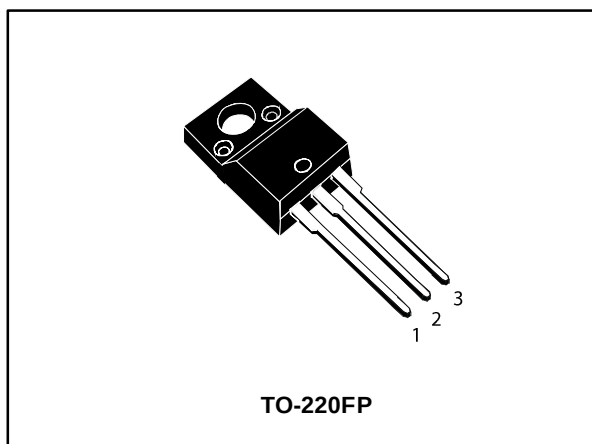
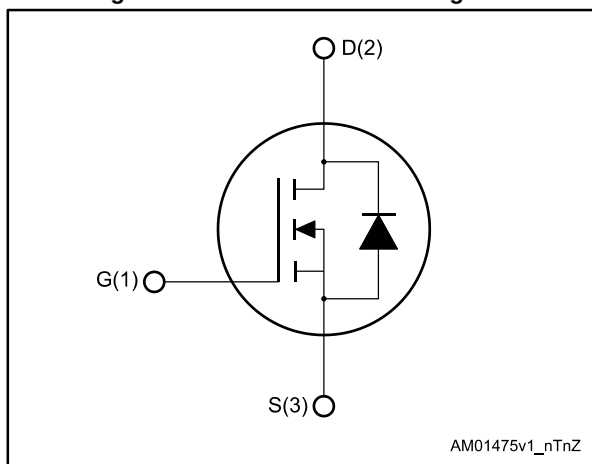


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STF140N6F7	60 V	0.0035 Ω	70 A	33 W

- Among the lowest R_{DS(on)} on the market
- Excellent figure of merit (FoM)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packing
STF140N6F7	140N6F7	TO-220FP	Tube

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
	2.1 Electrical characteristics (curves)	6
3	Test circuits	8
4	Package information	9
	4.1 TO-220FP package information	10
5	Revision history	12

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_{case} = 25\text{ }^{\circ}\text{C}$	70	A
	Drain current (continuous) at $T_{case} = 100\text{ }^{\circ}\text{C}$	50	
$I_{DM}^{(2)}$	Drain current (pulsed)	280	A
P_{TOT}	Total dissipation at $T_{case} = 25\text{ }^{\circ}\text{C}$	33	W
$E_{AS}^{(3)}$	Single pulse avalanche energy	250	mJ
$dV/dt^{(4)}$	Drain-body diode dynamic dV/dt ruggedness	7.1	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$; $T_c = 25\text{ }^{\circ}\text{C}$)	2500	V
T_{stg}	Storage temperature	-55 to 175	$^{\circ}\text{C}$
T_j	Maximum junction temperature	175	

Notes:

- (1) Current is limited by package.
 (2) Pulse width is limited by safe operating area.
 (3) Starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = 20\text{ A}$, $V_{DD} = 30\text{ V}$.
 (4) $I_{SD} = 70\text{ A}$; $di/dt = 600\text{ A}/\mu\text{s}$; $V_{DD} = 48\text{ V}$; $T_j < T_{jmax}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	4.5	$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	62.5	

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 4: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0 V, I _D = 1 mA	60			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = 60 V			1	μA
		V _{GS} = 0 V, V _{DS} = 60 V, T _j = 125 °C			100	
I _{GSS}	Gate-body leakage current	V _{DS} = 0 V, V _{GS} = 20 V			100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2		4	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 35 A		0.0031	0.0035	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0 V	-	3100	-	pF
C _{oss}	Output capacitance		-	1520	-	
C _{rss}	Reverse transfer capacitance		-	193	-	
Q _g	Total gate charge	V _{DD} = 30 V, I _D = 70 A, V _{GS} = 10 V (see Figure 14: "Test circuit for gate charge behavior")	-	55	-	nC
Q _{gs}	Gate-source charge		-	19	-	
Q _{gd}	Gate-drain charge		-	18	-	

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 30 V, I _D = 35 A R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 13: "Test circuit for resistive load switching times" and Figure 18: "Switching time waveform")	-	24	-	ns
t _r	Rise time		-	68	-	
t _{d(off)}	Turn-off delay time		-	39	-	
t _f	Fall time		-	20	-	

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 70\text{ A}$	-		1.2	V
t_{rr}	Reverse recovery time	$I_{SD} = 70\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 48\text{ V}$ (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	42.4		ns
Q_{rr}	Reverse recovery charge		-	38.2		nC
I_{RRM}	Reverse recovery current		-	1.8		A

Notes:

⁽¹⁾ Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

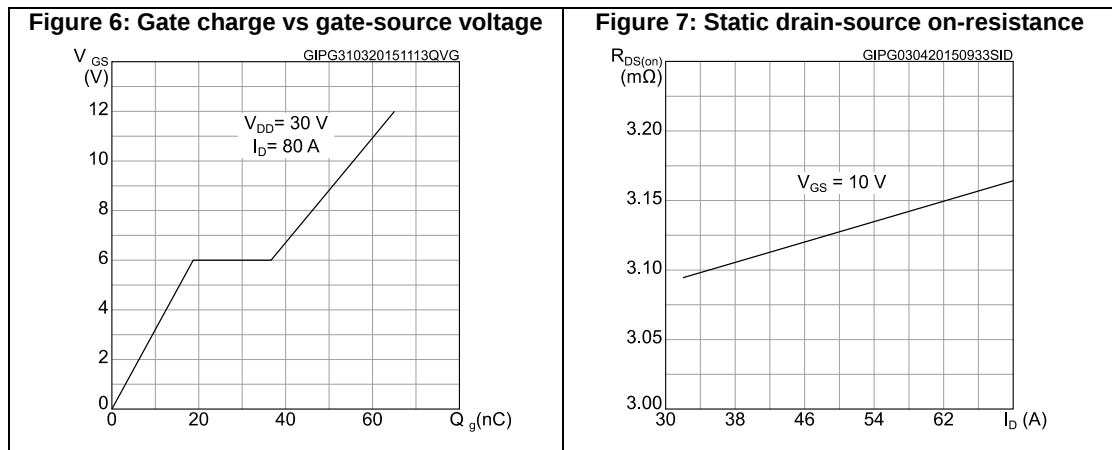
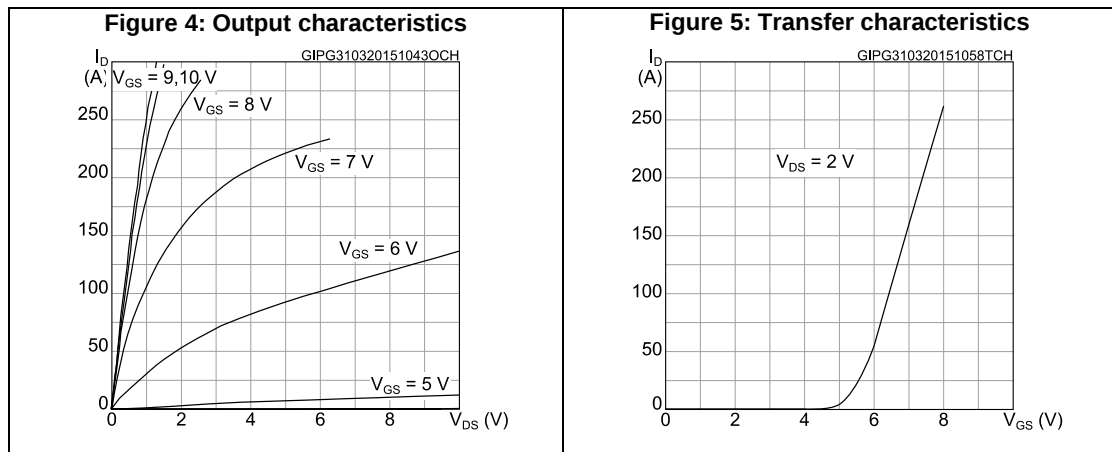
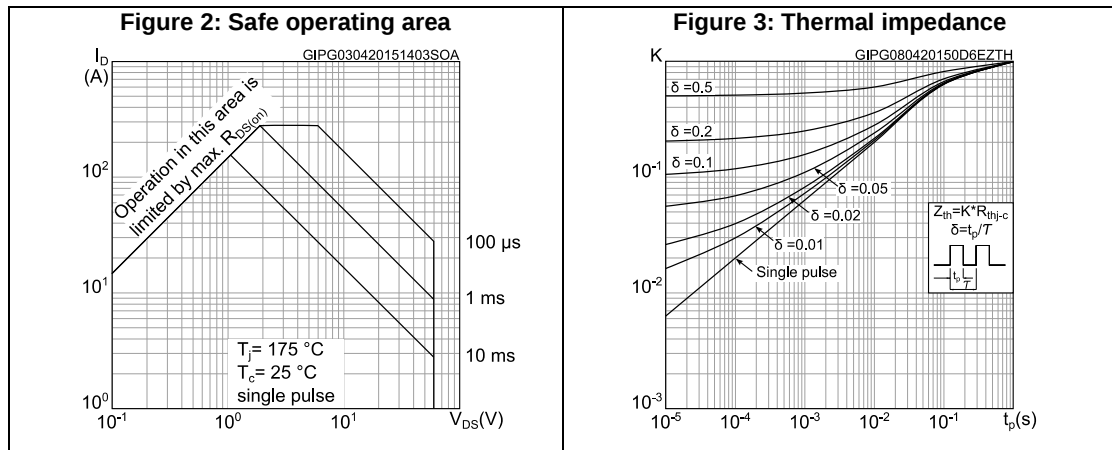


Figure 8: Capacitance variations

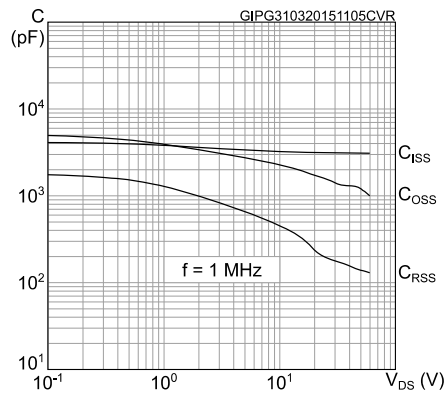


Figure 9: Normalized gate threshold voltage vs temperature

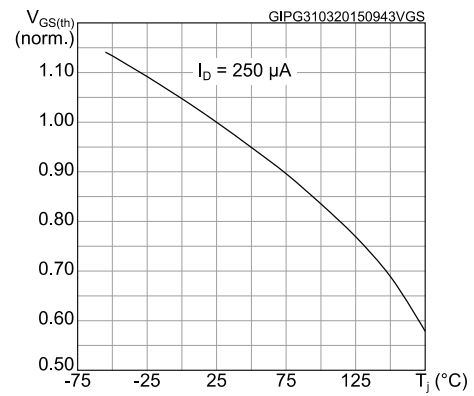


Figure 10: Normalized on-resistance vs temperature

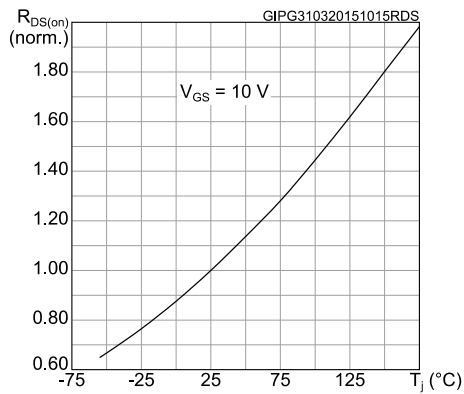


Figure 11: Normalized V(BR)DSS vs temperature

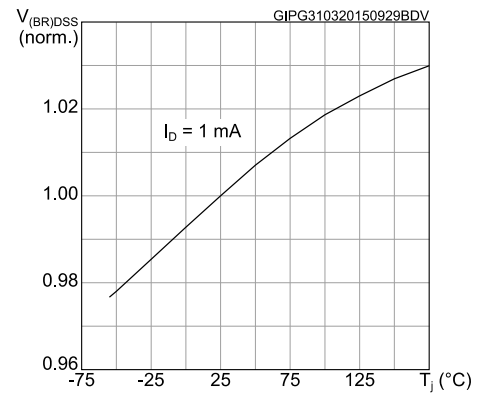
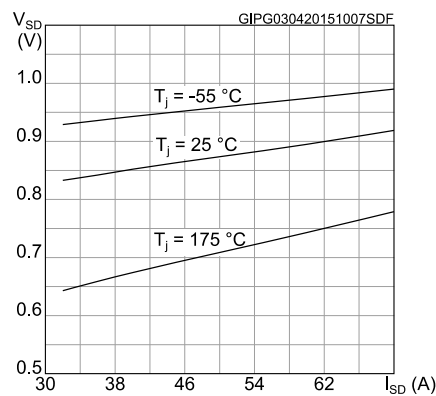
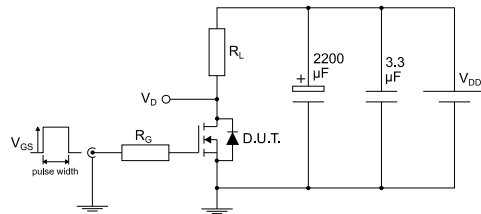


Figure 12: Source-drain diode forward characteristics



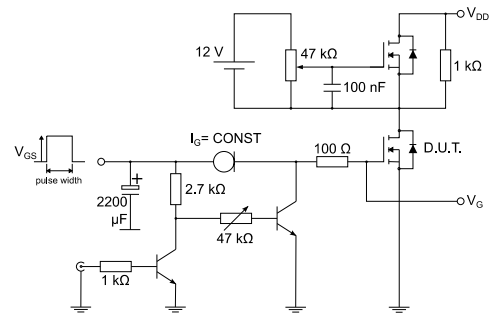
3 Test circuits

Figure 13: Test circuit for resistive load switching times



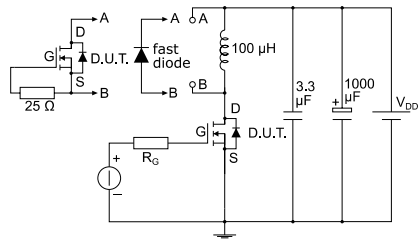
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Figure 14: Test circuit for gate charge behavior



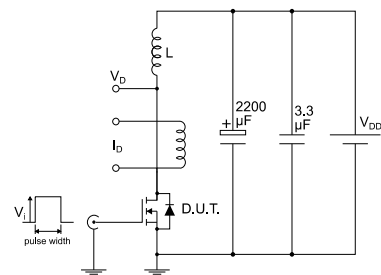
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Figure 15: Test circuit for inductive load switching and diode recovery times



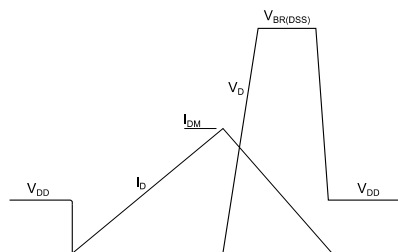
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Figure 16: Unclamped inductive load test circuit



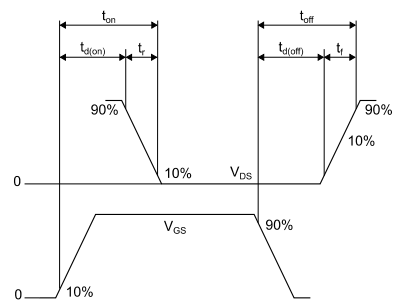
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Figure 17: Unclamped inductive waveform



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Figure 18: Switching time waveform



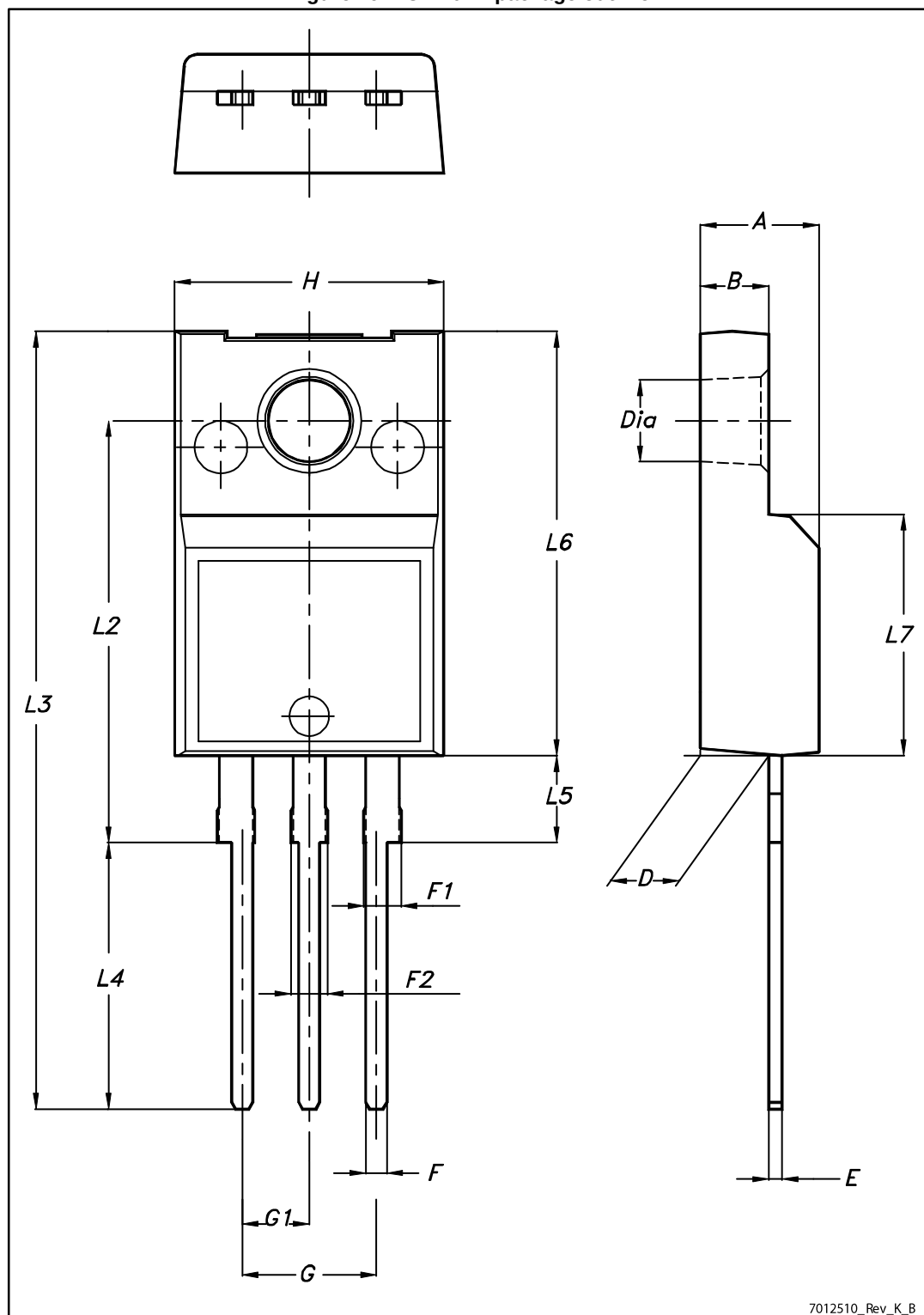
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.

4.1 TO-220FP package information

Figure 19: TO-220FP package outline



7012510_Rev_K_B

Table 8: TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

5 Revision history

Table 9: Document revision history

Date	Revision	Changes
09-Apr-2015	1	First release.
17-Apr-2015	2	Throughout document: - minor text edits - updated drain-source on-resistance values
14-Jan-2016	3	Updated Table 2: "Absolute maximum ratings" .

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