# IS43R32800B

## 8Mx32
## 256Mb DDR Synchronous DRAM

**PRELIMINARY INFORMATION**
**MAY 2008**

### FEATURES

- $V_{DD}/V_{DDQ}$=2.5V+0.2V (-5, -6, -75)
- Double data rate architecture; two data transfers per clock cycle
- Bidirectional, data strobe (DQS) is transmitted/ received with data
- Differential clock input (CLK and /CLK)
- DLL aligns DQ and DQS transitions with CLK transitions edges of DQS
- Commands entered on each positive CLK edge;
- Data and data mask referenced to both edges of DQS
- 4 bank operation controlled by BA0, BA1 (Bank Address)
- /CAS latency –2.0/2.5/3.0 (programmable)
- Burst length - 2/4/8 (programmable)
- Burst type - Sequential/ Interleave (programmable)
- Auto precharge / All bank precharge controlled by A8
- 4096 refresh cycles/ 64ms (4 banks concurrent refresh)
- Auto refresh and Self refresh
- Row address A0-11/ Column address A0-7, A9- SSTL_2 Interface
- Package 144-ball FBGA
- Available in Industrial Temperature
- Temperature Range:
  Commercial (0°C to +70°C)
  Industrial (-40°C to +85°C)

### DESCRIPTION:

IS43R32800B is a 4-bank x 2,097,152-word x32bit Double Data Rate Synchronous DRAM, with SSTL_2 interface. All control and address signals are referenced to the rising edge of CLK. Input data is registered on both edges of data strobe, and output data and data strobe are referenced on both edges of CLK. The IS43R32800B achieves very high speed clock rate up to 200 MHz. It is packaged in 144-ball FBGA.

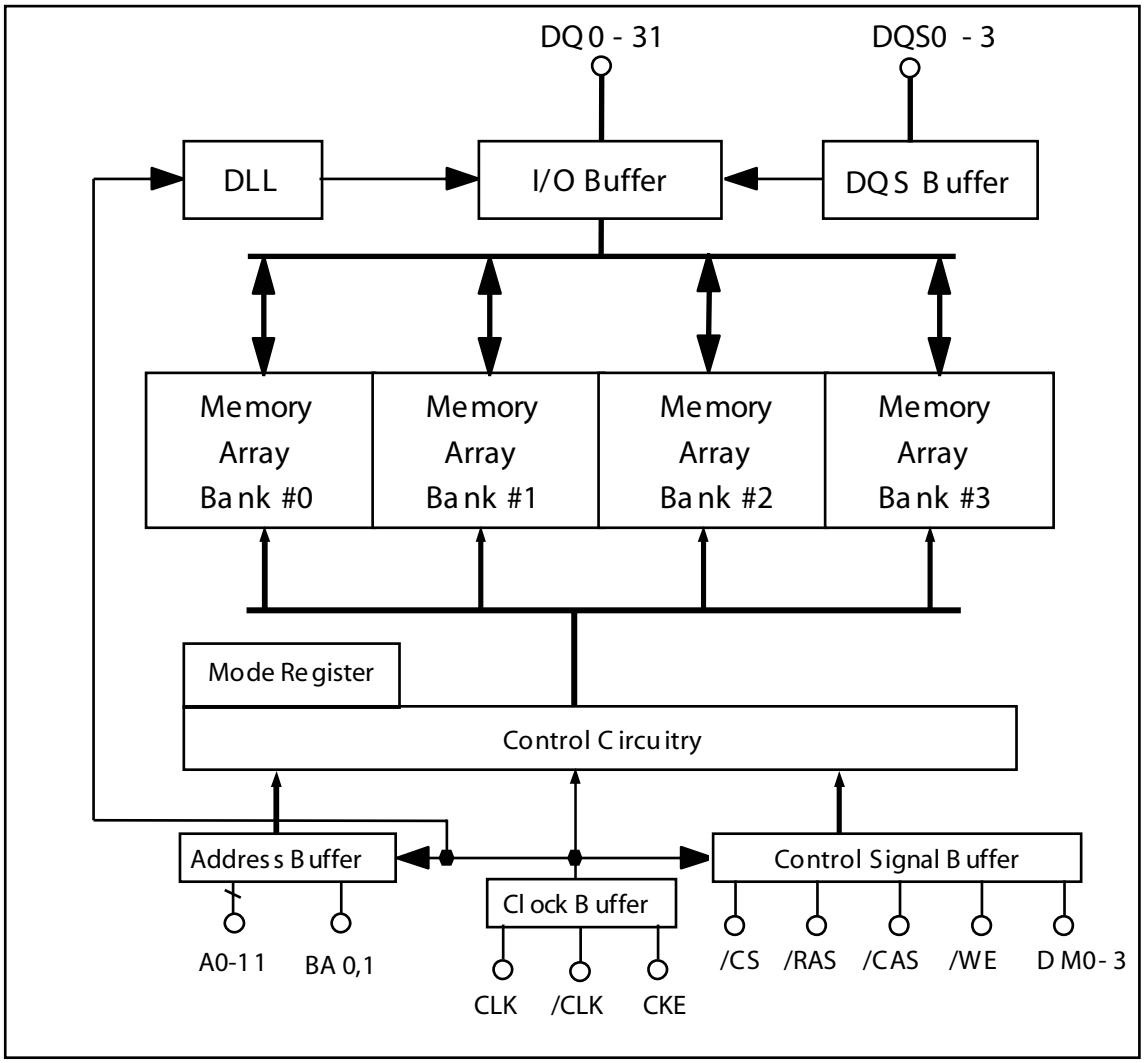
### KEY TIMING PARAMETERS

| Parameter | -5 | -6 | -75 | Unit |
|---|---|---|---|---|
| Clk Cycle Time | | | | |
| CAS Latency = 3 | 5 | 6 | 7.5 | ns |
| CAS Latency = 2.5 | 5 | 6 | 7.5 | ns |
| CAS Latency = 2 | 7.5 | 7.5 | 7.5 | ns |
| Clk Frequency | | | | |
| CAS Latency = 3 | 200 | 167 | 143 | MHz |
| CAS Latency = 2.5 | 200 | 167 | 143 | MHz |
| CAS Latency = 2 | 143 | 143 | 143 | MHz |
| Access Time from Clock | | | | |
| CAS Latency = 3 | ±0.70 | ±0.70 | ±0.70 | ns |
| CAS Latency = 2.5 | ±0.70 | ±0.70 | ±0.70 | ns |
| CAS Latency = 2 | ±0.75 | ±0.75 | ±0.70 | ns |

### ADDRESS TABLE

| Parameter | 8M x 32 |
|---|---|
| Configuration | 2M x 32 x 4 banks |
| Bank Address Pins | BA0, BA1 |
| Autoprecharge Pins | A8/AP |
| Row Addresses | A0 – A11 |
| Column Addresses | A0 – A7, A9 |
| Refresh Count | 4096 / 64ms |

## FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION

**Package Code: B 144-ball FBGA (Top View) (12.00mm x 12.00mm Body, 0.8mm Ball Pitch**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | DQS0 | DM0 | VSSQ | DQ3 | DQ2 | DQ0 | DQ31 | DQ29 | DQ28 | VSSQ | DM3 | DQS3 |
| B | DQ4 | VDDQ | NC | VDDQ | DQ1 | VDDQ | VDDQ | DQ30 | VDDQ | NC | VDDQ | DQ27 |
| C | DQ6 | DQ5 | VSSQ | VSSQ | VSSQ | VDD | VDD | VSSQ | VSSQ | VSSQ | DQ26 | DQ25 |
| D | DQ7 | VDDQ | VDD | VSS | VSSQ | VSS | VSS | VSSQ | VSS | VDD | VDDQ | DQ24 |
| E | DQ17 | DQ16 | VDDQ | VSSQ | VSS | VSS | VSS | VSS | VSSQ | VDDQ | DQ15 | DQ14 |
| F | DQ19 | DQ18 | VDDQ | VSSQ | VSS | VSS | VSS | VSS | VSSQ | VDDQ | DQ13 | DQ12 |
| G | DQS2 | DM2 | NC | VSSQ | VSS | VSS | VSS | VSS | VSSQ | NC | DM1 | DQS1 |
| H | DQ21 | DQ20 | VDDQ | VSSQ | VSS | VSS | VSS | VSS | VSSQ | VDDQ | DQ11 | DQ10 |
| J | DQ22 | DQ23 | VDDQ | VSSQ | VSS | VSS | VSS | VSS | VSSQ | VDDQ | DQ9 | DQ8 |
| K | /CAS | /WE | VDD | VSS | A10 | VDD | VDD | NC | VSS | VDD | NC | NC |
| L | /RAS | NC | NC | BA1 | A2 | A11 | A9 | A5 | NC | CLK | /CLK | NC |
| M | /CS | NC | BA0 | A0 | A1 | A3 | A4 | A6 | A7 | A8/AP | CKE | VREF |

## PIN DESCRIPTIONS

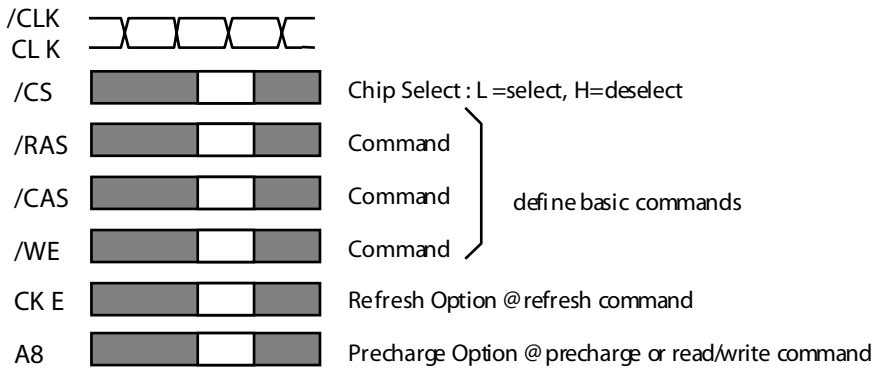
| | | | |
|---|---|---|---|
| CLK, /CLK | : Master Clock | A0-11 | : Address Input |
| CKE | : Clock Enable | BA 0,1 | : Bank Address Input |
| /CS | : Chip Select | $V_{DD}$ | : Power Supply |
| /RAS | : Row Address Strobe | $V_{DDQ}$ | : Power Supply for Output |
| /CAS | : Column Address Strobe | Vss | : Ground |
| /WE | : Write Enable | VssQ | : Ground for Output |
| DQ 0-31 | : Data I/O | DQS0-3 | : Data Strobe |
| DM 0-3 | : Write Mask | $V_{REF}$ | : Reference Voltage |

## PIN FUNCTIONS

| SYMBOL | TYPE | DESCRIPTION |
|---|---|---|
| CLK, /CLK | Input | Clock: CLK and /CLK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CLK and negative edge of /CLK. Output (read) data is referenced to the crossings of CLK and /CLK (both directions of crossing). |
| CKE | Input | Clock Enable: CKE controls internal clock. When CKE is low, internal clock for the following cycle is ceased. CKE is also used to select auto/ self refresh. After self refresh mode is started, CKE becomes asynchronous input. Self refresh is maintained as long as CKE is low. |
| /CS | Input | Chip Select: When /CS is high, any command means No Operation. |
| /RAS, /CAS, /WE | Input | Combination of /RAS, /CAS, /WE defines basic commands. |
| A0-11 | Input | A0-11 specify the Row / Column Address in conjunction with BA0,1. The Row Address is specified by A0-11. The Column Address is specified by A0-7,A9. A8 is also used to indicate precharge option. When A8 is high at a read / write command, an auto precharge is performed. When A8 is high at a precharge command, all banks are precharged. |
| BA 0,1 | Input | Bank Address: BA 0,1 specifies one of four banks to which a command is applied. BA 0,1 must be set with ACT, PRE, READ, WRITE commands. |
| DQ0-31 | Input / Output | Data Input/Output: Data bus |
| DQS0-3 | Input / Output | Data Strobe: Output with read data, input with write data. Edge-aligned with read data, centered in write data. Used to capture write data. DQS0 for DQ0 - DQ7, DQS1 for DQ8 - DQ15, DQS2 for DQ16 - DQ23, DQS3 for DQ24 - DQ31. |
| DM0-3 | Input | Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. DM0 for DQ0 - DQ7, DM1 for DQ8 - DQ15, DM2 for DQ16 - DQ23, DM3 for DQ24 - DQ31. |
| $V_{DD}$, Vss | Power Supply | Power Supply for the memory array and peripheral circuitry. |
| $V_{DDQ}$, $V_{SSQ}$ | Power Supply | $V_{DDQ}$ and $V_{SSQ}$ are supplied to the Output Buffers only. |
| Vref | Input | SSTL_2 reference voltage |

# FUNCTIONAL DESCRIPTION

ISSI's 256-Mbit DDR SDRAM provides basic functions, bank (row) activate, burst read / write, bank (row) precharge, and auto / self refresh. Each command is defined by control signals of /RAS, /CAS and /WE at CLK rising edge. In addition to 3 signals, /CS, CKE and A8 are used as chip select, refresh option, and precharge option, respectively. To know the detailed definition of commands, please see the command truth table.




**Activate (ACT)** [/RAS=L, /CAS=/WE=H]

ACT command activates a row in an idle bank indicated by BA.

**Read (READ)** [/RAS=H, /CAS=L, /WE=H]

READ command starts burst read from the active bank indicated by BA. First output data appears after /CAS latency. When A8=H at this command, the bank is deactivated after the burst read (auto-precharge READA)

**Write (WRITE)** [/RAS=H, /CAS=/WE=L]

WRITE command starts burst write to the active bank indicated by BA. Total data length to be written is set by burst length. When A8=H at this command, the bank is deactivated after the burst write (auto-precharge, WRITEA)

**Precharge (PRE)** [/RAS=L, /CAS=H, /WE=L]

PRE command deactivates the active bank indicated by BA. This command also terminates burst read /write operation. When A8=H at this command, all banks are deactivated (precharge all, PREA).

**Auto-Refresh (REFA)** [/RAS=/CAS=L, /WE=CKE=H]

REFA command starts auto-refresh cycle. Refresh address including bank address are generated internally. After this command, the banks are precharged automatically.

## COMMAND TRUTH TABLE

| COMMAND | MNEMONIC | CKE n-1 | CKE n | /CS | /RAS | /CAS | /WE | BA0,1 | A8 /AP | A0-7, A9-11 | note |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Deselect | DESEL | H | X | H | X | X | X | X | X | X | |
| No Operation | NOP | H | X | L | H | H | H | X | X | X | |
| Row Address Entry & Bank Activate | ACT | H | H | L | L | H | H | V | V | V | |
| Single Bank Precharge | PRE | H | H | L | L | H | L | V | L | X | |
| Precharge All Banks | PREA | H | H | L | L | H | L | X | H | X | |
| Column Address Entry & Write | WRITE | H | H | L | H | L | L | V | L | V | |
| Column Address Entry & Write with Auto-Precharge | WRITEA | H | H | L | H | L | L | V | H | V | |
| Column Address Entry & Read | READ | H | H | L | H | L | H | V | L | V | |
| Column Address Entry & Read with Auto-Precharge | READA | H | H | L | H | L | H | V | H | V | |
| Auto-Refresh | REFA | H | H | L | L | L | H | X | X | X | |
| Self-Refresh Entry | REFS | H | L | L | L | L | H | X | X | X | |
| Self-Refresh Exit | REFSX | L | H | H | X | X | X | X | X | X | |
| | | L | H | L | H | H | H | X | X | X | |
| Burst Terminate | TERM | H | H | L | H | H | L | X | X | X | 1 |
| Mode Register Set | MRS | H | H | L | L | L | L | L | L | V | 2 |

H=High Level, L=Low Level, V=Valid, X=Don't Care, n=CLK cycle number

NOTE:

1. Applies only to read bursts with autoprecharge disabled; this command is undefined (and should not be used) for read bursts with autoprecharge enabled, and for write bursts.
2. BA0-BA1 select either the Base or the Extended Mode Register (BA0 = 0, BA1 = 0 selects Mode Register;BA0=1 , BA1 = 0 selects Extended Mode Register; other combinations of BA0-BA1 are reserved; A0-A11 provide the op-code to be written to the selected Mode Register.

## FUNCTIONAL TRUTH TABLE

| Current State | /CS | /RAS | /CAS | /WE | Address | Command | Action | Notes |
|---|---|---|---|---|---|---|---|---|
| IDLE | H | X | X | X | X | DESEL | NOP | |
| | L | H | H | H | X | NOP | NOP | |
| | L | H | H | L | BA | TERM | ILLEGAL | 2 |
| | L | H | L | X | BA, CA, A8 | READ / WRITE | ILLEGAL | 2 |
| | L | L | H | H | BA, RA | ACT | Bank Active, Latch RA | |
| | L | L | H | L | BA, A8 | PRE / PREA | NOP | 4 |
| | L | L | L | H | X | REFA | Auto-Refresh | 5 |
| | L | L | L | L | Op-Code, Mode-Add | MRS | Mode Register Set | 5 |
| ROW ACTIVE | H | X | X | X | X | DESEL | NOP | |
| | L | H | H | H | X | NOP | NOP | |
| | L | H | H | L | BA | TERM | ILLEGAL | |
| | L | H | L | H | BA, CA, A8 | READ / READA | Begin Read, Latch CA, Determine Auto-Precharge | |
| | L | H | L | L | BA, CA, A8 | WRITE / WRITEA | Begin Write, Latch CA, Determine Auto-Precharge | |
| | L | L | H | H | BA, RA | ACT | Bank Active / ILLEGAL | 2 |
| | L | L | H | L | BA, A8 | PRE / PREA | Precharge / Precharge All | |
| | L | L | L | H | X | REFA | ILLEGAL | |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL | |
| READ(Auto-Precharge Disabled) | H | X | X | X | X | DESEL | NOP (Continue Burst to END) | |
| | L | H | H | H | X | NOP | NOP (Continue Burst to END) | |
| | L | H | H | L | BA | TERM | Terminate Burst | |
| | L | H | L | H | BA, CA, A8 | READ / READA | Terminate Burst, Latch CA, Begin New Read, Determine Auto-Precharge | 3 |
| | L | H | L | L | BA, CA, A8 | WRITE / WRITEA | ILLEGAL | |
| | L | L | H | H | BA, RA | ACT | Bank Active / ILLEGAL | 2 |
| | L | L | H | L | BA, A8 | PRE / PREA | Terminate Burst, Precharge | |
| | L | L | L | H | X | REFA | ILLEGAL | |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL | |

## FUNCTIONAL TRUTH TABLE (continued)

| Current State | /CS | /RAS | /CAS | /WE | Address | Command | Action | Notes |
|---|---|---|---|---|---|---|---|---|
| WRITE(Auto-Precharge Disabled) | H | X | X | X | X | DESEL | NOP (Continue Burst to END) | |
| | L | H | H | H | X | NOP | NOP (Continue Burst to END) | |
| | L | H | H | L | BA | TERM | ILLEGAL | |
| | L | H | L | H | BA, CA, A8 | READ / READA | Terminate Burst, Latch CA, Begin Read, Determine Auto-Precharge | 3 |
| | L | H | L | L | BA, CA, A8 | WRITE / WRITEA | Terminate Burst, Latch CA, Begin Write, Determine Auto-Precharge | 3 |
| | L | L | H | H | BA, RA | ACT | Bank Active / ILLEGAL | 2 |
| | L | L | H | L | BA, A8 | PRE / PREA | Terminate Burst, Precharge | |
| | L | L | L | H | X | REFA | ILLEGAL | |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL | |
| READ with Auto-Precharge | H | X | X | X | X | DESEL | NOP (Continue Burst to END) | |
| | L | H | H | H | X | NOP | NOP (Continue Burst to END) | |
| | L | H | H | L | BA | TERM | ILLEGAL | |
| | L | H | L | H | BA, CA, A8 | READ / READA | ILLEGAL | |
| | L | H | L | L | BA, CA, A8 | WRITE / WRITEA | ILLEGAL | |
| | L | L | H | H | BA, RA | ACT | Bank Active / ILLEGAL | 2 |
| | L | L | H | L | BA, A8 | PRE / PREA | Precharge / ILLEGAL | 2 |
| | L | L | L | H | X | REFA | ILLEGAL | |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL | |
| WRITE with Auto-Precharge | H | X | X | X | X | DESEL | NOP (Continue Burst to END) | |
| | L | H | H | H | X | NOP | NOP (Continue Burst to END) | |
| | L | H | H | L | BA | TERM | ILLEGAL | |
| | L | H | L | H | BA, CA, A8 | READ / READA | ILLEGAL | |
| | L | H | L | L | BA, CA, A8 | WRITE / WRITEA | ILLEGAL | |
| | L | L | H | H | BA, RA | ACT | Bank Active / ILLEGAL | 2 |
| | L | L | H | L | BA, A8 | PRE / PREA | Precharge / ILLEGAL | 2 |
| | L | L | L | H | X | REFA | ILLEGAL | |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL | |

## FUNCTIONAL TRUTH TABLE (continued)

| Current State | /CS | /RAS | /CAS | /WE | Address | Command | Action | Notes |
|---|---|---|---|---|---|---|---|---|
| PRE-CHARGING | H | X | X | X | X | DESEL | NOP (Idle after tRP) | |
| | L | H | H | H | X | NOP | NOP (Idle after tRP) | |
| | L | H | H | L | BA | TERM | ILLEGAL | 2 |
| | L | H | L | X | BA, CA, A8 | READ / WRITE | ILLEGAL | 2 |
| | L | L | H | H | BA, RA | ACT | ILLEGAL | 2 |
| | L | L | H | L | BA, A8 | PRE / PREA | NOP (Idle after tRP) | 4 |
| | L | L | L | H | X | REFA | ILLEGAL | |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL | |
| ROW ACTIVATING | H | X | X | X | X | DESEL | NOP (Row Active after tRCD) | |
| | L | H | H | H | X | NOP | NOP (Row Active after tRCD) | |
| | L | H | H | L | BA | TERM | ILLEGAL | 2 |
| | L | H | L | X | BA, CA, A8 | READ / WRITE | ILLEGAL | 2 |
| | L | L | H | H | BA, RA | ACT | ILLEGAL | 2 |
| | L | L | H | L | BA, A8 | PRE / PREA | ILLEGAL | 2 |
| | L | L | L | H | X | REFA | ILLEGAL | |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL | |
| WRITER E-COVERING | H | X | X | X | X | DESEL | NOP | |
| | L | H | H | H | X | NOP | NOP | |
| | L | H | H | L | BA | TERM | ILLEGAL | 2 |
| | L | H | L | X | BA, CA, A8 | READ / WRITE | ILLEGAL | 2 |
| | L | L | H | H | BA, RA | ACT | ILLEGAL | 2 |
| | L | L | H | L | BA, A8 | PRE / PREA | ILLEGAL | 2 |
| | L | L | L | H | X | REFA | ILLEGAL | |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL | |

## FUNCTIONAL TRUTH TABLE (continued)

| Current State | /CS | /RAS | /CAS | /WE | Address | Command | Action | Notes |
|---|---|---|---|---|---|---|---|---|
| REFRESHING | H | X | X | X | X | DESEL | NOP (Idle after tRC) | |
| | L | H | H | H | X | NOP | NOP (Idle after tRC) | |
| | L | H | H | L | BA | TERM | ILLEGAL | |
| | L | H | L | X | BA, CA, A8 | READ / WRITE | ILLEGAL | |
| | L | L | H | H | BA, RA | ACT | ILLEGAL | |
| | L | L | H | L | BA, A8 | PRE / PREA | ILLEGAL | |
| | L | L | L | H | X | REFA | ILLEGAL | |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL | |
| MODE REGISTER SETTING | H | X | X | X | X | DESEL | NOP (Row Active after tRSC) | |
| | L | H | H | H | X | NOP | NOP (Row Active after tRSC) | |
| | L | H | H | L | BA | TERM | ILLEGAL | |
| | L | H | L | X | BA, CA, A8 | READ / WRITE | ILLEGAL | |
| | L | L | H | H | BA, RA | ACT | ILLEGAL | |
| | L | L | H | L | BA, A8 | PRE / PREA | ILLEGAL | |
| | L | L | L | H | X | REFA | ILLEGAL | |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL | |

ABBREVIATIONS:
H=High Level, L=Low Level, X=Don't Care
BA=Bank Address, RA=Row Address, CA=Column Address, NOP=No Operation

NOTES:
1. All entries assume that CKE was High during the preceding clock cycle and the current clock cycle.
2. ILLEGAL to bank in specified state; function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around, write recovery requirements.
4. NOP to bank precharging or in idle state. May precharge bank indicated by BA.
5. ILLEGAL if any bank is not idle.

ILLEGAL = Device operation and/or data-integrity are not guaranteed.

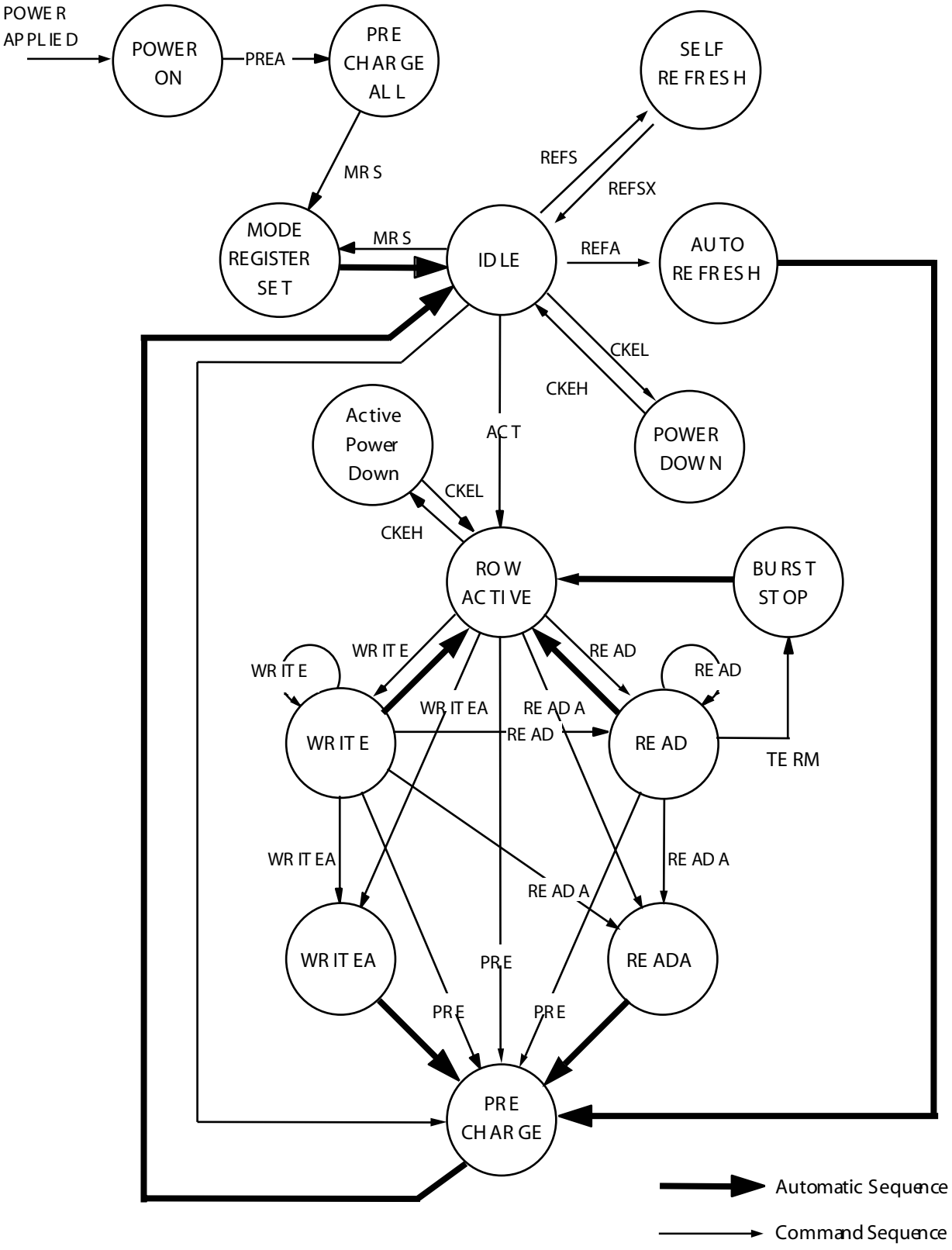
## CKE TRUTH TABLE

| Current State | CKE n-1 | CKE n | /CS | /RAS | /CAS | /WE | Address | Action | Notes |
|---|---|---|---|---|---|---|---|---|---|
| SELF - REFRESHING | H | X | X | X | X | X | X | INVALID | 1 |
| | L | H | H | X | X | X | X | Exit Self-Refresh (Idle after tRC) | 1 |
| | L | H | L | H | H | H | X | Exit Self-Refresh (Idle after tRC) | 1 |
| | L | H | L | H | H | L | X | ILLEGAL | 1 |
| | L | H | L | H | L | X | X | ILLEGAL | 1 |
| | L | H | L | L | X | X | X | ILLEGAL | 1 |
| | L | L | X | X | X | X | X | NOP (Maintain Self-Refresh) | 1 |
| POWER DOWN | H | X | X | X | X | X | X | INVALID | |
| | L | H | X | X | X | X | X | Exit Power Down to Idle | |
| | L | L | X | X | X | X | X | NOP (Maintain Self-Refresh) | |
| ALL BANKS IDLE | H | H | X | X | X | X | X | Refer to Function Truth Table | 2 |
| | H | L | L | L | L | H | X | Enter Self-Refresh | 2 |
| | H | L | H | X | X | X | X | Enter Power Down | 2 |
| | H | L | L | H | H | H | X | Enter Power Down | 2 |
| | H | L | L | H | H | L | X | ILLEGAL | 2 |
| | H | L | L | H | L | X | X | ILLEGAL | 2 |
| | H | L | L | L | X | X | X | ILLEGAL | 2 |
| | L | X | X | X | X | X | X | Refer to Current State =Power Down | 2 |
| ANY STATE other than listed above | H | H | X | X | X | X | X | Refer to Function Truth Table | |
| | H | L | X | X | X | X | X | Begin CLK Suspend at Next Cycle | 3 |
| | L | H | X | X | X | X | X | Exit CLK Suspend at Next Cycle | 3 |
| | L | L | X | X | X | X | X | Maintain CLK Suspend | |

ABBREVIATIONS:
H=High Level, L=Low Level, X=Don't Care

NOTES:
1. CKE Low to High transition will re-enable CLK and other inputs asynchronously.
   A minimum setup time must be satisfied before any command other than EXIT.
2. Power-Down and Self-Refresh can be entered only from the All Banks Idle State.
3. Must be legal command.

## STATE DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Ratings | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | with respect to Vss | -0.5 ~ 3.7 | V |
| $V_{DDQ}$ | Supply Voltage for Output | with respect to VssQ | -0.5 ~ 3.7 | V |
| VI | Input Voltage | with respect to Vss | -0.5 ~ Vdd+0.5 | V |
| VO | Output Voltage | with respect to VssQ | -0.5 ~ VddQ+0.5 | V |
| IO | Output Current | 5 | 50 | mA |
| Pd | Power Dissipation | Ta = 25 °C | 2000 | mW |
| Topr | Operating Temperature | Commercial<br>Industrial | 0 to +70<br>-40 to +85 | °C |
| Tstg | Storage Temperature | | -65 ~ 150 | °C |

## DC OPERATING CONDITIONS

| Parameter | Limits | | | Unit | Notes |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| Supply Voltage | 2.3 | 2.5 | 2.7 | V | -5, -6, -75 |
| Supply Voltage for Output | 2.3 | 2.5 | 2.7 | V | -5, -6, -75 |
| High-Level Input Voltage | $V_{REF}$ +0.15 | | $V_{DD}$+0.3 | V | |
| Low-Level Input Voltage | -0.3 | | $V_{REF}$ -0.15 | V | |
| Input Leakage Current<br>Any input 0V <VIN< VDD<br>(All other pins not under test = 0V) | -2 | —— | 2 | uA | |
| Output Leakage Current DQ are disabled 0V< Vout<$V_{DDQ}$ | -5 | —— | 5 | uA | |
| Output Levels:<br>Output High Voltage (Iout=-4mA) | 2.4 | —— | —— | V | |
| Output Low Voltage(Iout=4mA) | —— | —— | 0.4 | V | |

## CAPACITANCE CHARACTERISTICS

VDD = $V_{DDQ}$ = 2.5V ± 0.2V, Vss = VssQ = 0V, unless otherwise noted)

| Symbol | Parameter | Test Condition | Limits | | Delta Cap.(Max.) | Unit | Notes |
|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | | | |
| CI (A) | Input Capacitance, address pin | VI =1.25V | 1.2 | 2.2 | 0.75 | pF | |
| CI (C) | Input Capacitance, control pin | f=100MHz | 1.2 | 2.2 | | pF | |
| CI (K) | Input Capacitance, CLK pin | VI= 25mVrms | 1.2 | 2.2 | 0.25 | pF | |
| CI /O | I/O Capacitance, I/O, DQS, DM pin | | 2.2 | 4.2 | 1.3 | pF | |

## AVERAGE SUPPLY CURRENT FROM $V_{DD}$

$V_{DD} = V_{DDQ} = 2.5V \pm 0.2V$, Vss = VssQ = 0V, Output Open, unless otherwise noted

| Symbol | Parameter/Test Conditions | Limits (Max) | | | Unit | Notes |
|---|---|---|---|---|---|---|
| | | -5 | -6 | -75 | | |
| IDD1 | OPERATING CURRENT : One Bank; Active-Read-Precharge ;Burst = 2; tRC = tRC MIN; tCK = tCK MIN; IOUT = 0mA; Address and control inputs changing once per clock cycle | 250 | 230 | 230 | mA | |
| IDD2P | PRECHARGE POWER-DOWN STANDBY CURRENT : All banks idle; power-down mode; CKE $\leq$ VIL (MAX); tCK = tCK MIN | 40 | 35 | 35 | | |
| IDD2N | IDLE STANDBY CURRENT : /CS $\geq$ VIH (MIN); All banks idle; CKE $\geq$ VIH (MIN); tCK = tCK MIN; Address and other control inputs changing once per clock cycle | 70 | 65 | 65 | | |
| IDD3P | ACTIVE POWER DOWN STANDBY CURRENT : One bank active;power down mode;CKE $\leq$ VIL (MAX); tCK = tCK MIN | 55 | 50 | 50 | | |
| IDD3N | ACTIVE STANDBY CURRENT: /CS $\geq$ VIH (MIN); CKE $\geq$ VIH (MIN); One bank; Active-Precharge; tRC = tRAS MAX; tCK = tCK MIN; DQ,DM and DQS inputs changing twice per clock cycle; address and other control inputs changing once per clock cycle | 105 | 100 | 100 | | |
| IDD4R | OPERATING CURRENT : Burst = 2; Read ; Continuous burst; All banks active; Address and control inputs changing once per clock cycle; tCK = tCK MIN; IOUT = 0 mA | 400 | 360 | 360 | | |
| IDD4W | OPERATING CURRENT : Burst = 2; Write ; Continuous burst; All banks active; Address and control inputs changing once per clock cycle; tCK = tCK MIN; DQ and DQS inputs changing twice per clock cycle | 400 | 360 | 360 | | |
| IDD5 | AUTO REFRESH CURRENT : tRC = tRFC (MIN) | 250 | 240 | 240 | | |
| IDD6 | SELF REFRESH CURRENT : CKE $\leq$ 0.2V | 5 | 5 | 5 | | |

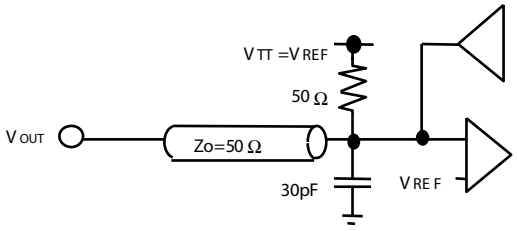
## AC TIMING REQUIREMENTS

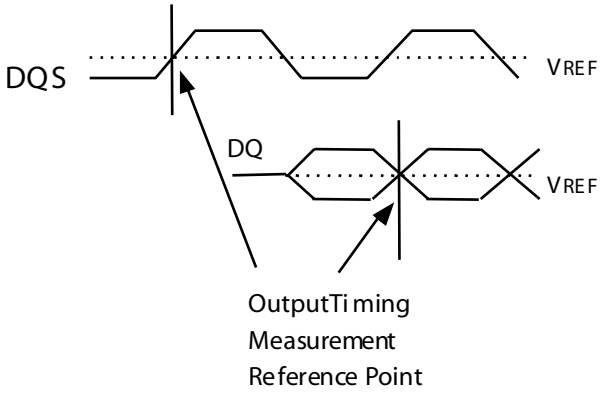
| Symbol | AC Characteristics Parameter | | -5 | | -6 | | -75 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max | Min. | Max | Min. | Max | | |
| tAC | DQ Output access time from CLK //CLK | | -0.70 | +0.70 | -0.70 | +0.70 | -0.75 | +0.75 | ns | |
| tDQSCK | DQS Output access time from CLK //CLK | | -0.6 | +0.6 | -0.60 | +0.60 | -0.75 | +0.75 | ns | |
| tCH | CLK High level width | | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | tCK | |
| tCL | CLK Low level width | | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | tCK | |
| tCK | CLK cycle time | CL=3.0 | 5 | 7.5 | 6 | 12 | 7.5 | 12 | ns | |
| | | CL=2.5 | 5 | 12 | 6 | 12 | 7.5 | 12 | ns | |
| | | CL=2.0 | 7.5 | 12 | 7.5 | 12 | 7.5 | 12 | ns | |
| tDS | Input Setup time (DQ,DM) | | 0.4 | | 0.45 | | 0.5 | | ns | |
| tDH | Input Hold time(DQ,DM) | | 0.4 | | 0.45 | | 0.5 | | ns | |
| tIPW | Control & address input pulse width (for each input) | | 2.2 | | 2.2 | | 2.2 | | ns | |
| tDIPW | DQ and DM input pulse width (for each input) | | 1.75 | | 1.75 | | 1.75 | | ns | |
| tHZ | Data-out-high impedance time from CLK //CLK | | | +0.70 | | +0.70 | | +0.75 | ns | 14 |
| tLZ | Data-out-low impedance time from CLK//CLK | | -0.70 | +0.70 | -0.70 | +0.70 | -0.75 | +0.75 | ns | 14 |
| tDQSQ | DQ Valid data delay time from DQS | | | 0.40 | | 0.45 | | 0.5 | ns | |
| tHP | Clock half period | | tCLmin or tCHmin | | tCLmin or tCHmin | | tCLmin or tCHmin | | ns | 20 |
| tQH | DQ output hold time from DQS (per access) | | tHP-tQHS | | tHP-tQHS | | tHP-tQHS | | ns | |
| tQHS | Data hold skew factor (for DQS & associated DQ signals) | | | 0.50 | | 0.55 | | 0.75 | | |
| tDQSS | Write command to first DQS latching transition | | 0.72 | 1.25 | 0.75 | 1.25 | 0.75 | 1.25 | tCK | |
| tDQSH | DQS input High level width | | 0.35 | | 0.35 | | 0.35 | | tCK | |
| tDQSL | DQS input Low level width | | 0.35 | | 0.35 | | 0.35 | | tCK | |
| tDSS | DQS falling edge to CLK setup time | | 0.2 | | 0.2 | | 0.2 | | tCK | |
| tDSH | DQS falling edge hold time from CLK | | 0.2 | | 0.2 | | 0.2 | | tCK | |
| tMRD | Mode Register Set command cycle time | | 2 | | 2 | | 2 | | tCK | |
| tWPRES | Write preamble setup time | | 0 | | 0 | | 0 | | ns | 16 |
| tWPST | Write postamble | | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | tCK | 15 |
| tWPRE | Write preamble | | 0.25 | | 0.25 | | 0.25 | | tCK | |
| tIS | Input Setup time (address and control) | | 0.6 | | 0.75 | | 0.9 | | ns | 19 |
| tIH | Input Hold time (address and control) | | 0.6 | | 0.75 | | 0.9 | | ns | 19 |
| tRPST | Read postamble | | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | tCK | |
| tRPRE | Read preamble | | 0.9 | 1.1 | 0.9 | 1.1 | 0.9 | 1.1 | tCK | |

## AC TIMING REQUIREMENTS (Continued)

| Symbol | AC Characteristics Parameter | -5 | | -6 | | -75 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max | Min. | Max | Min. | Max | | |
| tRAS | Row Active time | 40 | 120,000 | 42 | 120,000 | 45 | 120,000 | ns | |
| tRC | Row Cycle time(operation) | 55 | | 60 | | 65 | | ns | |
| tRFC | Auto Ref. to Active/Auto Ref. command period | 70 | | 72 | | 75 | | ns | |
| tRCD | Row to Column Delay | 15 | | 18 | | 20 | | ns | |
| tRP | Row Precharge time | 15 | | 18 | | 20 | | ns | |
| tRRD | Act to Act Delay time | 10 | | 12 | | 15 | | ns | |
| tWR | Write Recovery time | 15 | | 15 | | 15 | | ns | |
| tDAL | Auto Precharge write recovery + precharge time | tWR+tRP | | tWR+tRP | | tWR+tRP | | ns | |
| tWTR | Internal Write to Read Command Delay | 2 | | 1 | | 1 | | tCK | |
| tXSNR | Exit Self Ref. to non-Read command | 75 | | 75 | | 75 | | ns | |
| tXSRD | Exit Self Ref. to -Read command | 200 | | 200 | | 200 | | tCK | |
| tXPNR | Exit Power down to command | 1 | | 1 | | 1 | | tCK | |
| tXPRD | Exit Power down to -Read command | 1 | | 1 | | 1 | | tCK | 18 |
| tREFI | Average Periodic Refresh interval | | 15.6 | | 15.6 | | 15.6 | µs | 17 |

### Output Load Condition



Notes
1. All voltages referenced to Vss.
2. Tests for AC timing, IDD, and electrical, AC and DC characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. AC timing and IDD tests may use a VIL to VIH swing of up to 1.5V in the test environment, but input timing is still referenced to VREF (or to the crossing point for CK//CK), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals is 1V/ns in the range between VIL(AC) and VIH(AC).
4. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e. the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above (below) the DC input LOW (HIGH) level.
5. VREF is expected to be equal to 0.5*$V_{DDQ}$ of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on VREF may not exceed ±2% of the DC value.
6. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF, and must track variations in the DC level of VREF.
7. VID is the magnitude of the difference between the input level on CLK and the input level on /CLK.
8. The value of VIX is expected to equal 0.5*$V_{DDQ}$ of the transmitting device and must track variations in the DC level of the same.
9. Enables on-chip refresh and address counters.
10. IDD specifications are tested after the device is properly initialized.
11. This parameter is sampled. $V_{DDQ}$ = 2.5V ± 0.2V, $V_{DD}$ = 2.5V ± 0.2V, f = 100 MHz, Ta = 25°C, VOUT(DC) = $V_{DDQ}$/2, VOUT(PEAK TO PEAK) = 25mV. DM inputs are grouped with I/O pins - reflecting the fact that they are matched in loading (to facilitate trace matching at the board level).
12. The CLK//CLK input reference level (for timing referenced to CLK//CLK) is the point at which CLK and /CLK cross; the input reference level for signals other than CLK//CLK, is VREF.
13. Inputs are not recognized as valid until VREF stabilizes. Exception: during the period before VREF stabilizes, CKE <= 0.3$V_{DDQ}$ is recognized as LOW.
14. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ), or begins driving (LZ).
15. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
16. The specific requirement is that DQS be valid (HIGH, LOW, or at some point on a valid transition) on or before this CLK edge. A valid transition is defined as monotonic, and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from High-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on tDQSS.
17. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM device.
18. tXPRD should be 200 tCLK in the condition of the unstable CLK operation during the power down mode.
19. For command/address and CK & /CK slew rate > 1.0V/ns.
20. Min (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device.

Timing patterns:
tCK = min, tRRD = 2*tCK, BL = 4, tRCD = 3*tCK, Read with Autoprecharge
Read: A0 N A1 R0 A2 R1 N R3 A0 N A1 R0 – repeat the same timing with random address changing
*100% of data changing at every burst
Legend: A = Activate, R = Read, P = Precharge, N = NOP

## FUNCTIONAL DESCRIPTION

The IS43R32800B is a 256Mb DDR SDRAM internally configured as a quad--bank DRAM. These 256Mb device contains 4 banks x 2,097,152 x32 bits. The DDR SDRAM uses a double--data--rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2n prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR SDRAM consists of a single 2n-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access. Prior to normal operation, the DDR SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

### INITIALIZATION

DDR SDRAMs must be powered up and initialized in a predefined manner.

### POWER ON SEQUENCE

Before starting normal operation, the following power on sequence is necessary to prevent a DDR SDRAM from damaged or multi functioning.

1. Apply VDD before or the same time as VDDQ
2. Apply VDDQ before or at the same time as VTT & Vref
3. Maintain stable condition for 200us after stable power and CLK, apply NOP or DSEL
4. Issue precharge command for all banks of the device
5. Issue EMRS
6. Issue MRS for the Mode Register and to reset the DLL
7. Issue 2 or more Auto Refresh commands
8. Maintain stable condition for 200cycles

After these sequence, the DDR SDRAM is idle state and ready for normal operation.

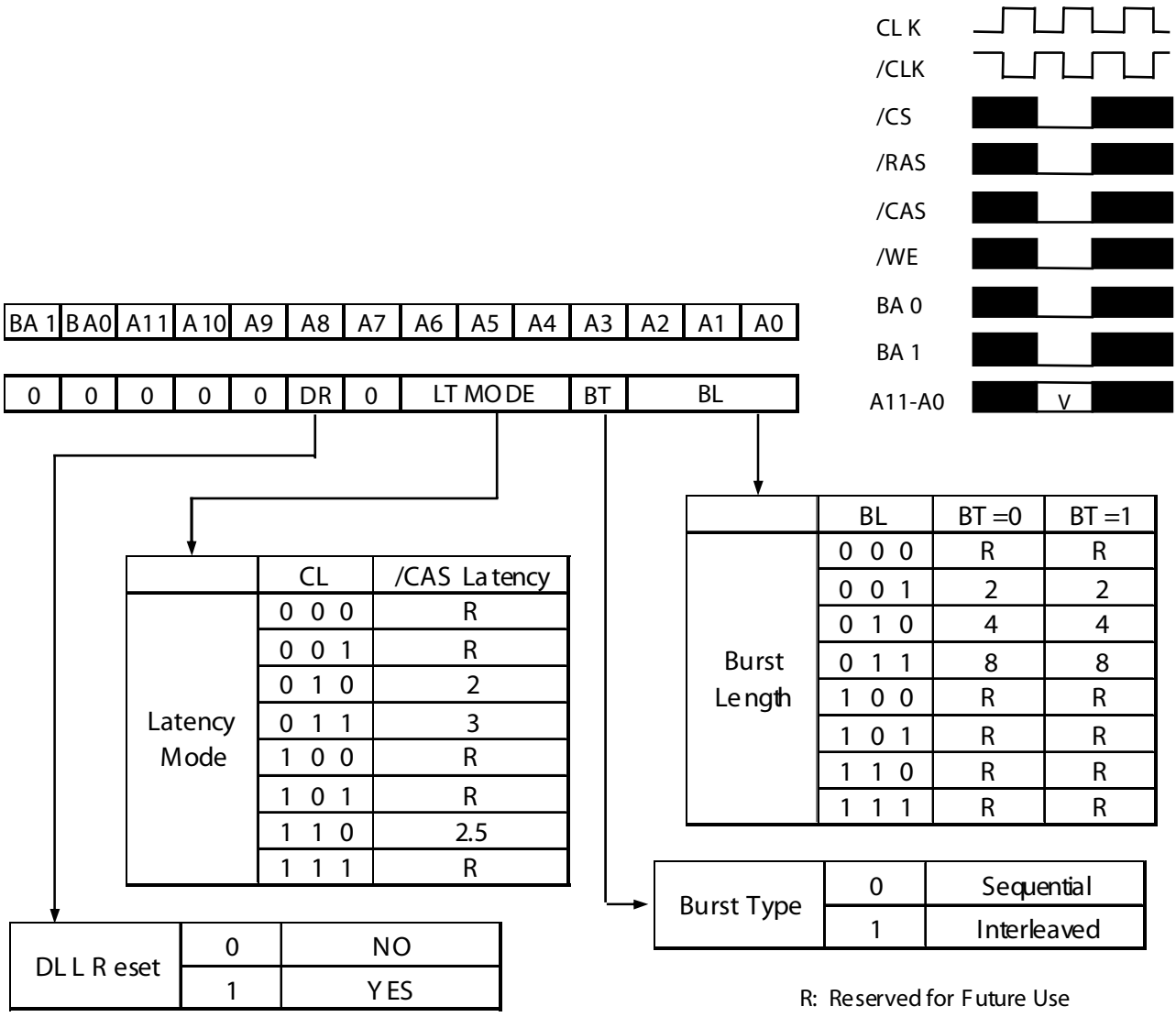
## REGISTER DEFINITION

### MODE REGISTER

The Mode Register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, and an operating mode, as shown in Figure “MODE REGISTER DEFINITION”. The Mode Register is programmed via the MODE REGISTER SET (MRS) command (with BA0 = 0 and BA1 = 0) and will retain stored information until it is programmed again or the device loses power.

Mode Register bits A0-A2 specify the burst length, A3 specifies the type of burst (sequential or interleaved), A4-A6 specify the CAS latency, and A7-A11 specify the operating mode.

The Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. After tMRD from a MRS command the DDR SDRAM is ready for a new command. Violating either of these requirements will result in unspecified operation.




**MODE REGISTER DEFINITION**

## Burst Length

Read and write accesses to the DDR SDRAM are burst oriented, with the burst length being programmable, as shown in Figure “CAS LATENCY”. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result. When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1--Ai when the burst length is set to two, by A2--Ai when the burst length is set to four and by A3--Ai when the burst length is set to eight (where Ai is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both read and write bursts.

## Burst Type

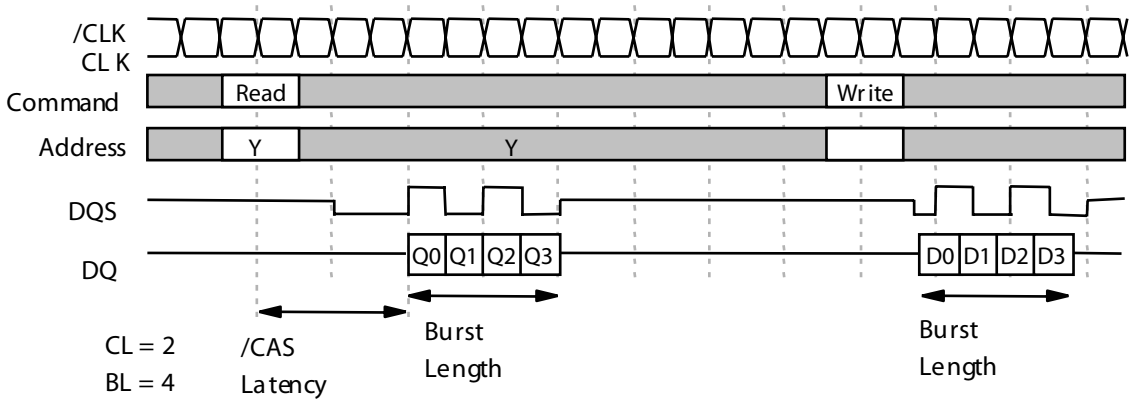
Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit A3. The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Table “BURST DEFINITION”.

## Read Latency

The READ latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. If a READ command is registered at clock edge n, and the latency is m clocks, the data will be available nominally coincident with clock edge n + m.

Reserved states should not be used as unknown operation, or incompatibility with future versions may result.

## CAS LATENCY




## BURST DEFINITION

| Initial Address | | | BL | Column Addressing | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A2 | A1 | A0 | | Sequential | | | | | | | | Interleaved | | | | | | | |
| 0 | 0 | 0 | 8 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 0 | 0 | 1 | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 0 | 3 | 2 | 5 | 4 | 7 | 6 |
| 0 | 1 | 0 | | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 0 | 1 | 6 | 7 | 4 | 5 |
| 0 | 1 | 1 | | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 |
| 1 | 0 | 0 | | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 |
| 1 | 0 | 1 | | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 4 | 7 | 6 | 1 | 0 | 3 | 2 |
| 1 | 1 | 0 | | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 4 | 5 | 2 | 3 | 0 | 1 |
| 1 | 1 | 1 | | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | 0 | 0 | 4 | 0 | 1 | 2 | 3 | | | | | 0 | 1 | 2 | 3 | | | | |
| - | 0 | 1 | | 1 | 2 | 3 | 0 | | | | | 1 | 0 | 3 | 2 | | | | |
| - | 1 | 0 | | 2 | 3 | 0 | 1 | | | | | 2 | 3 | 0 | 1 | | | | |
| - | 1 | 1 | | 3 | 0 | 1 | 2 | | | | | 3 | 2 | 1 | 0 | | | | |
| - | - | 0 | 2 | 0 | 1 | | | | | | | 0 | 1 | | | | | | |
| - | - | 1 | | 1 | 0 | | | | | | | 1 | 0 | | | | | | |

## EXTENDED MODE REGISTER

The Extended Mode Register controls functions beyond those controlled by the Mode Register; these additional functions include DLL enable/disable, output drive strength selection (optional). These functions are controlled via the bits shown in Figure EXTENDED MODE REGISTER.

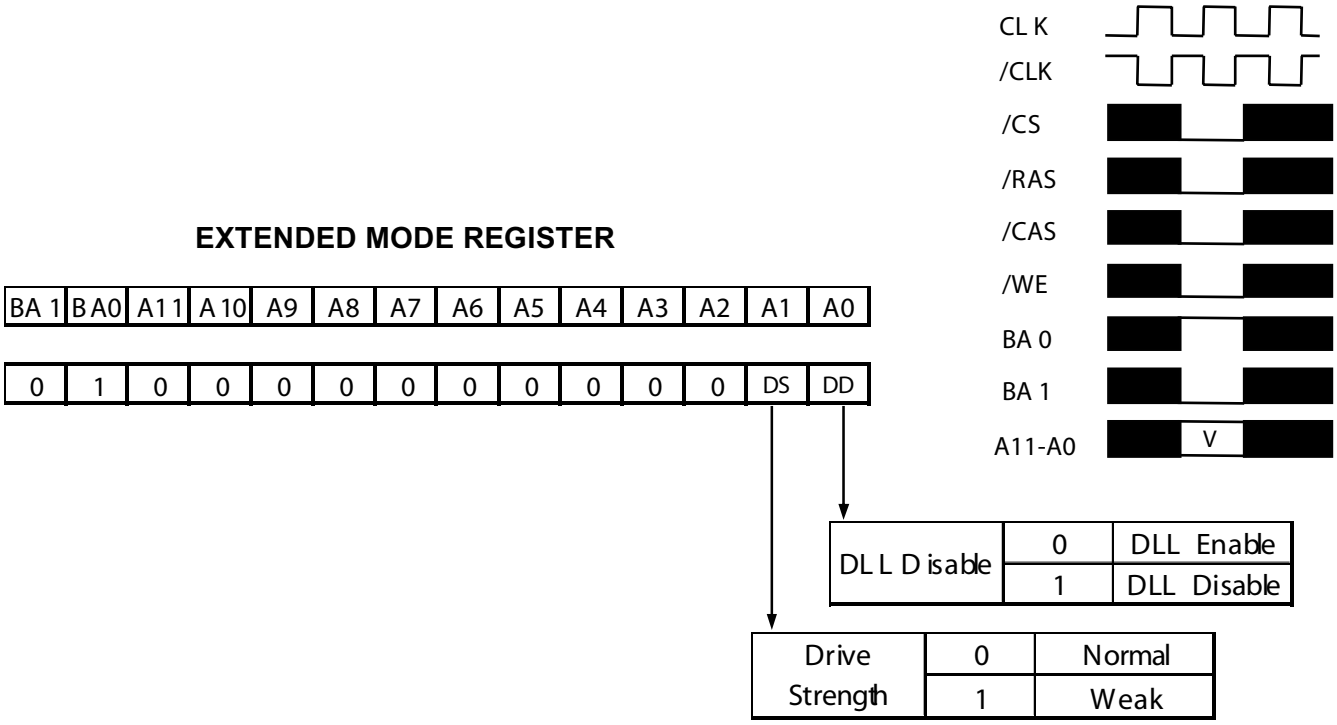
The Extended Mode Register is programmed via the MODE REGISTER SET command (with BA0 = 1 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power. The Extended Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. After tMRD from a MRS command the DDR SDRAM is ready for a new command. Violating either of these requirements will result in unspecified operation.

### DLL Enable/Disable

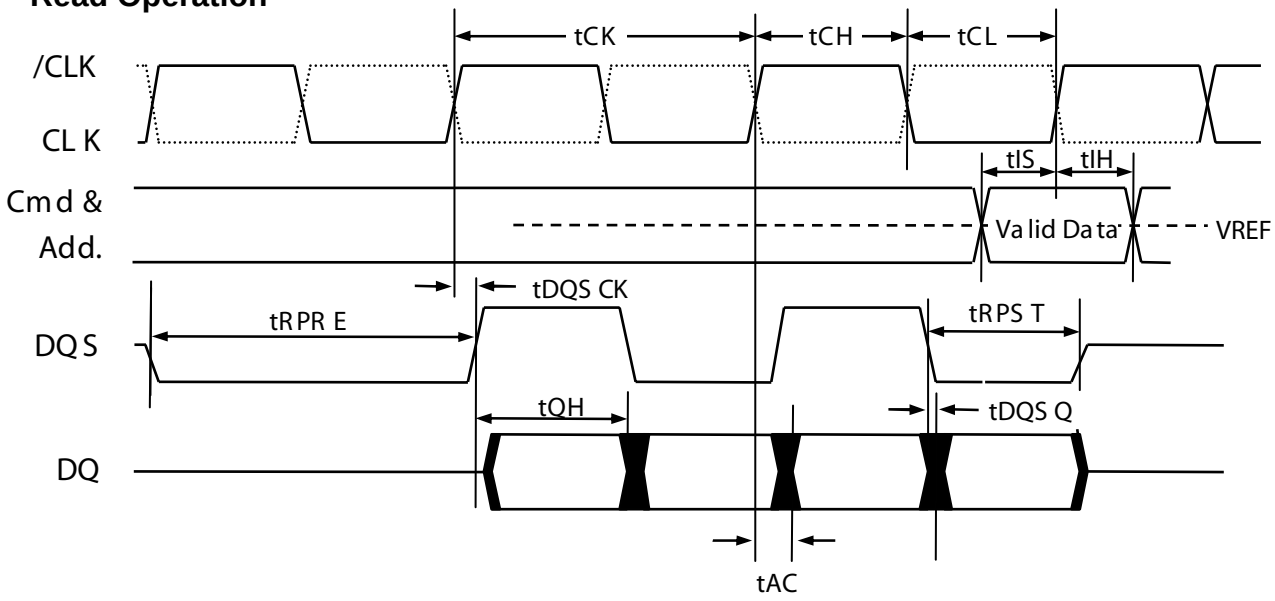
The DLL must be enabled for normal operation. DLL enable is required during power-up initialization, and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation (upon exiting Self Refresh Mode, the DLL is enabled automatically). Any time the DLL is enabled a DLL Reset must follow and 200 clock cycles must occur before any executable command can be issued.

### Output Drive Strength

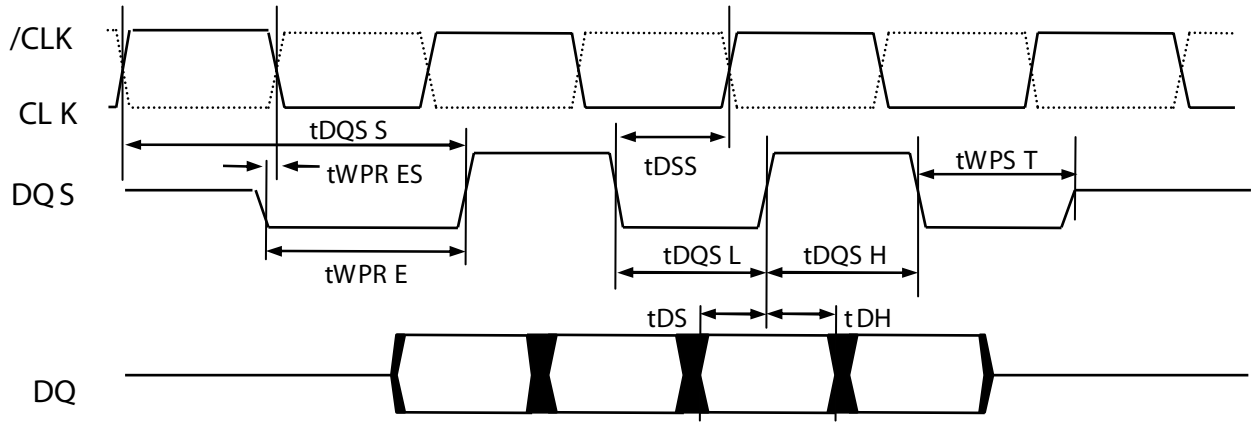
The normal drive strength for all outputs is specified to be SSTL_2, Class II. The ISSI DDR SDRAM also supports a weak driver strength option, intended for lighter load and/or point-to-point environments.



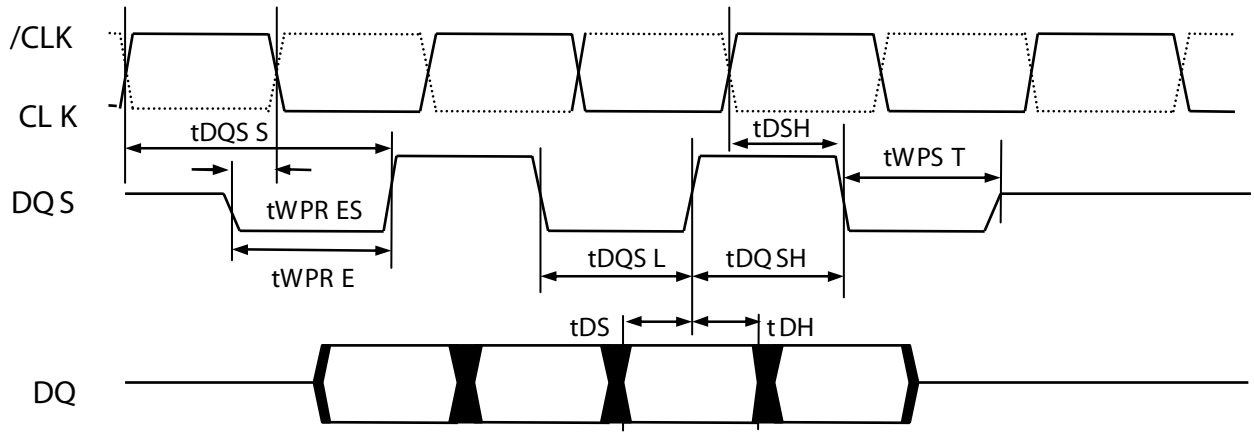
## Read Operation




## Write Operation / tDQSS=max.




## Write Operation / tDQSS=min.



## OPERATIONAL DESCRIPTION

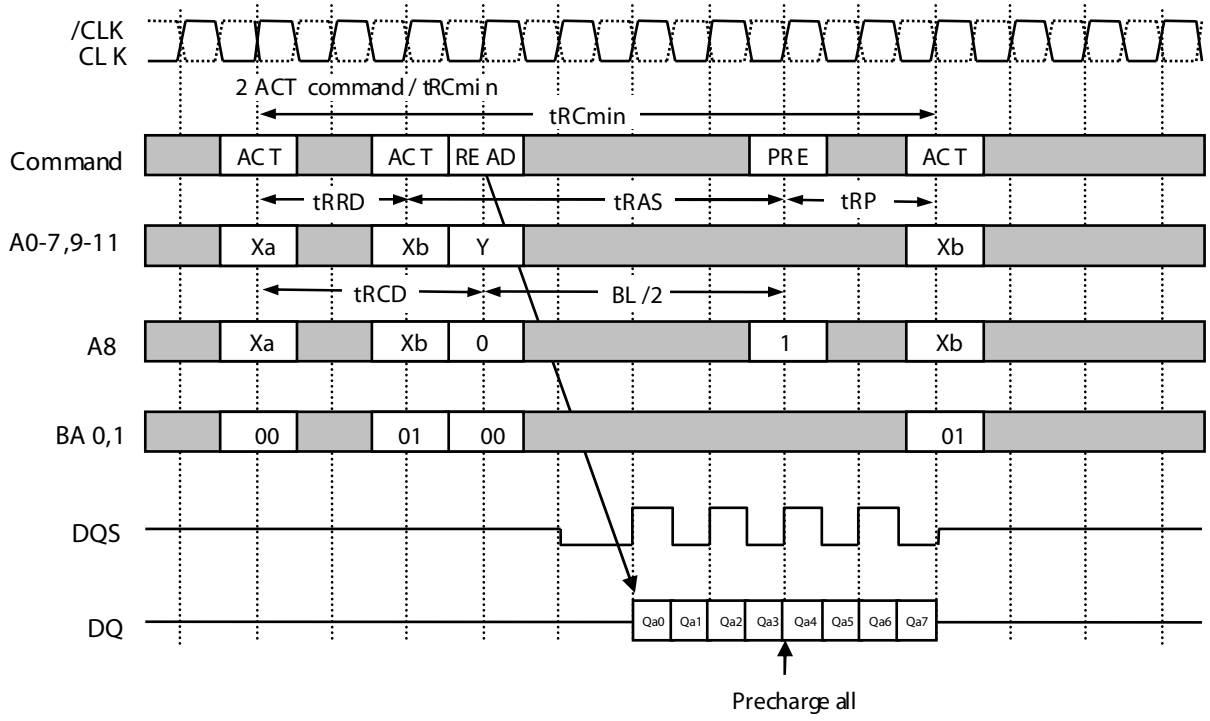
### BANK ACTIVATE

The DDR SDRAM has four independent banks. Each bank is activated by the ACT command with the bank addresses (BA 0,1). A row is indicated by the row address A0-11. The minimum activation interval between one bank and the other bank is tRRD.

### PRECHARGE

The PRE command deactivates the bank indicated by BA 0,1. When multiple banks are active, the prechargeall command (PRE A, PRE+ A8=H) is available to deactivate them at the same time. After tRP from the precharge, an ACT command to the same bank can be issued.

**Bank Activation and PrechargeAll (BL=8, CL=2)**

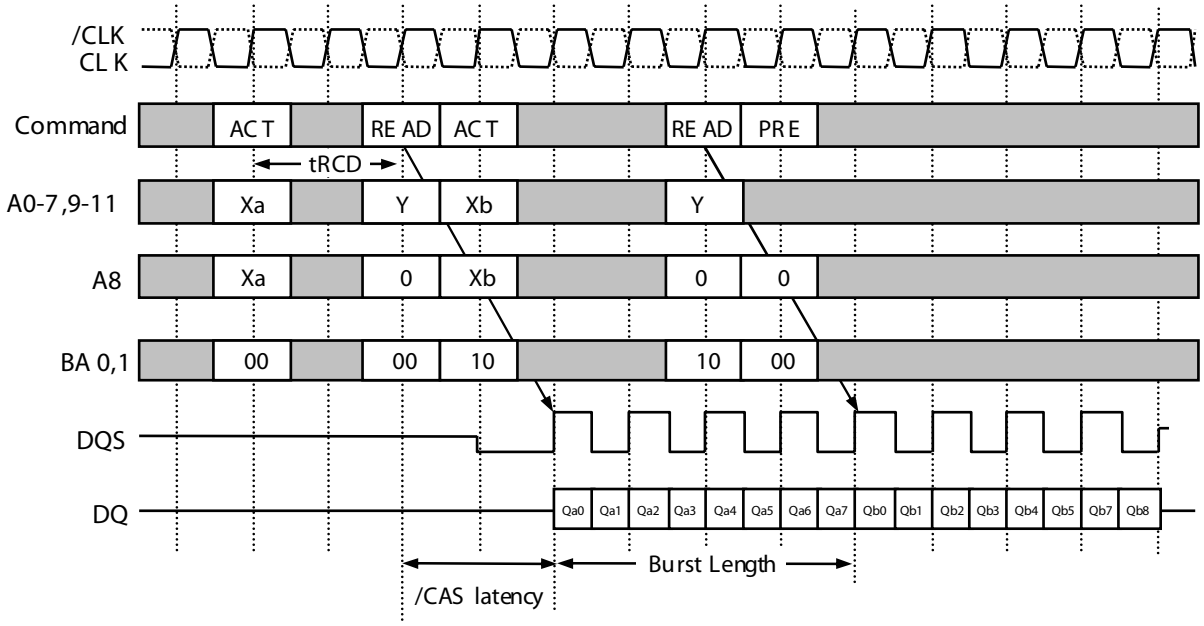



A precharge command can be issued at BL/2 from a read command without data loss.

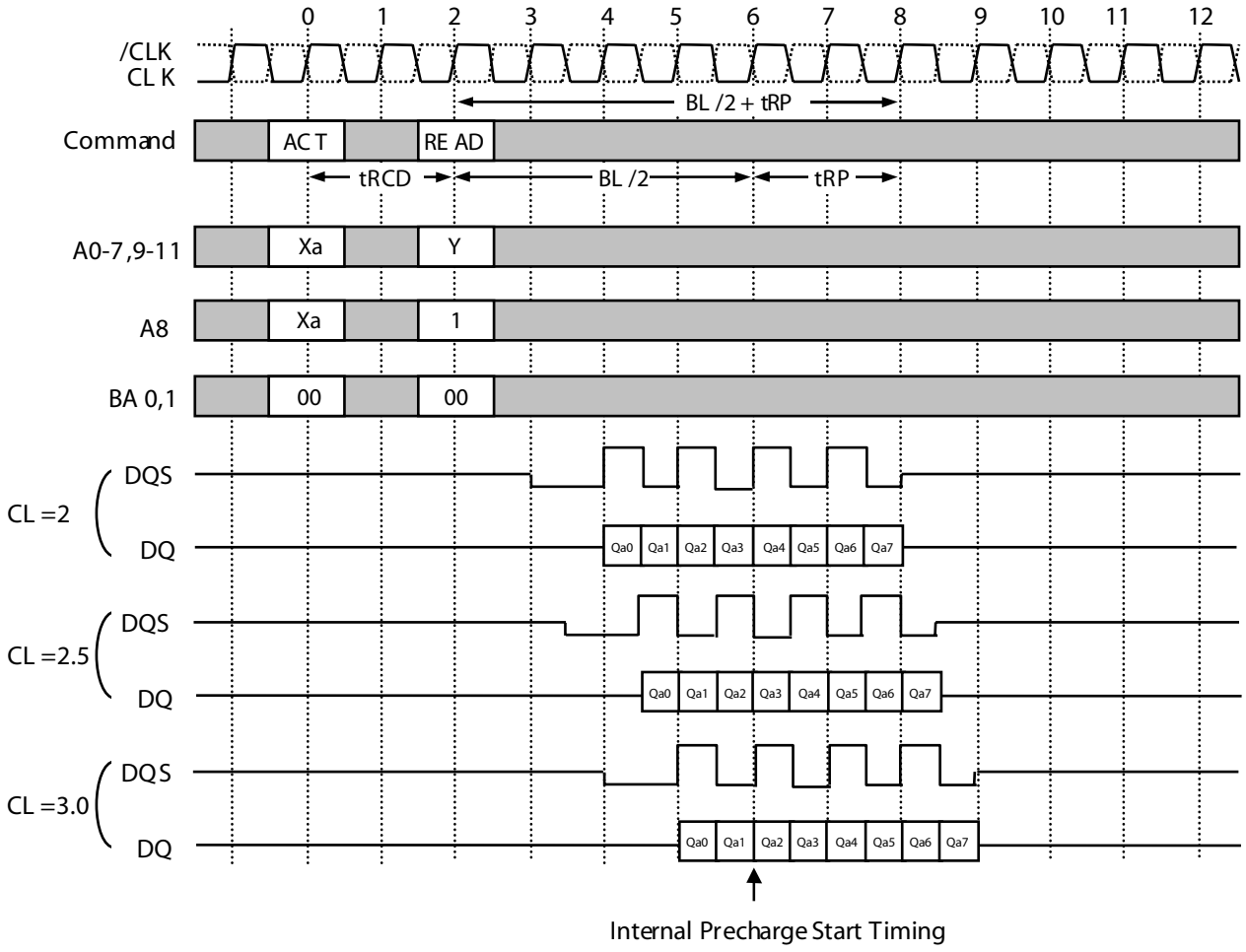
## READ

After tRCD from the bank activation, a READ command can be issued. 1st Output data is available after the /CAS Latency from the READ, followed by (BL-1) consecutive data when the Burst Length is BL. The start address is specified by A0-7,9, and the address sequence of burst data is defined by the Burst Type. A READ command may be applied to any active bank, so the row precharge time (tRP) can be hidden behind continuous output data by interleaving the multiple banks. When A8 is high at a READ command, the auto-precharge (READA) is performed. Any command(READ,WRITE,PRE,ACT) to the same bank is inhibited till the internal precharge is complete. The internal precharge starts at BL/2 after READA. The next ACT command can be issued after (BL/2+tRP) from the previous READA.

**Multi Bank Interleaving READ (BL=8, CL=2)**

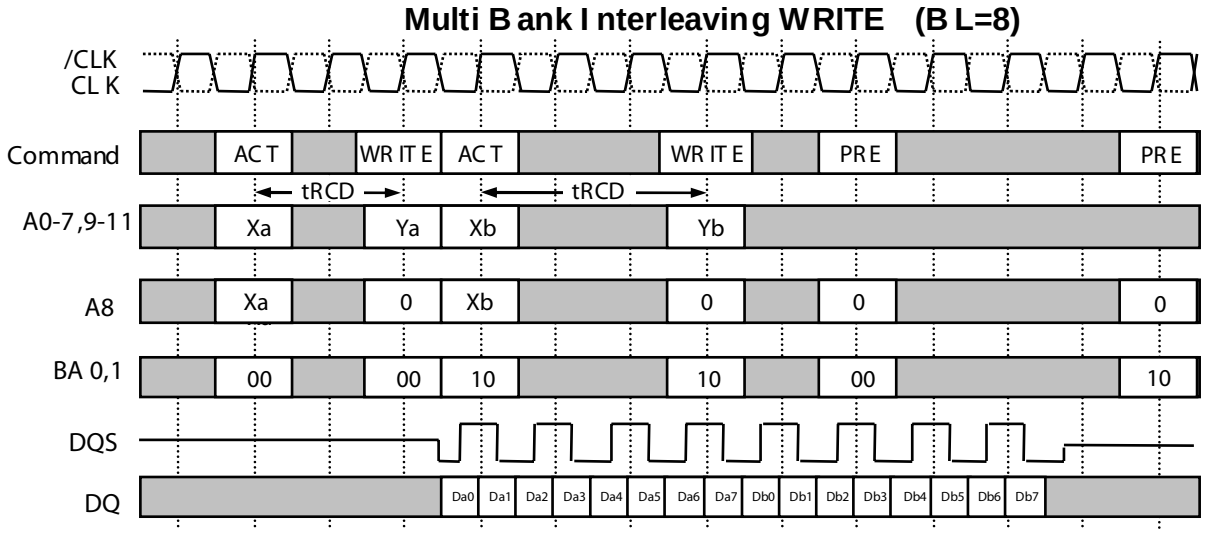


## READ with Auto-Precharge(BL=8, CL=2,2.5,3.0)

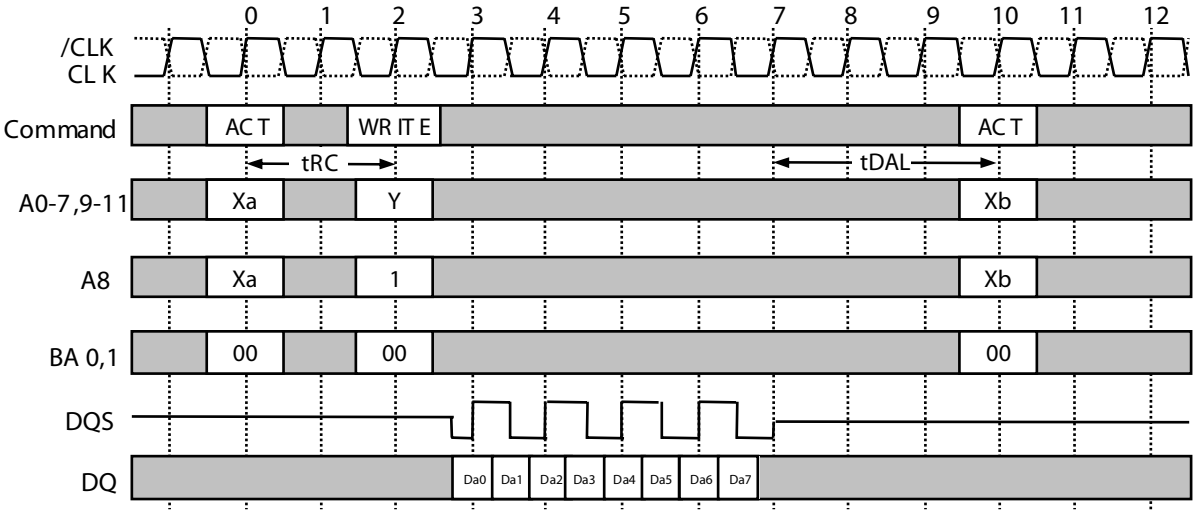


## WRITE

After tRCD from the bank activation, a WRITE command can be issued. 1st input data is set from the WRITE command with data strobe input, following (BL-1) data are written into RAM, when the Burst Length is BL. The start address is specified by A0-7,9, and the address sequence of burst data is defined by the Burst Type. A WRITE command may be applied to any active bank, so the row precharge time (tRP) can be hidden behind continuous input data by interleaving the multiple banks. From the last data to the PRE command, the write recovery time (tWRP) is required. When A8 is high at a WRITE command, the auto-precharge(WRITEA) is performed. Any command(READ,WRITE,PRE,ACT) to the same bank is inhibited till the internal precharge is complete. The next ACT command can be issued after tDAL from the last input data cycle.



## WRITE with Auto-Precharge (BL=8)

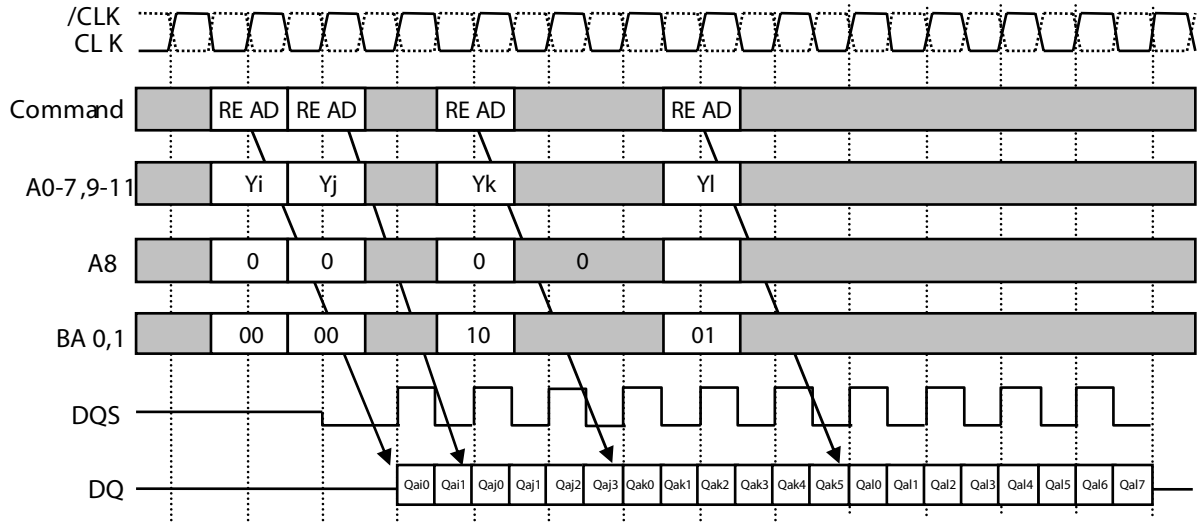


## BURST INTERRUPTION

### Read Interrupted by Read

Burst read operation can be interrupted by new read of any bank. Random column access is allowed. READ to READ interval is minimum 1CLK.

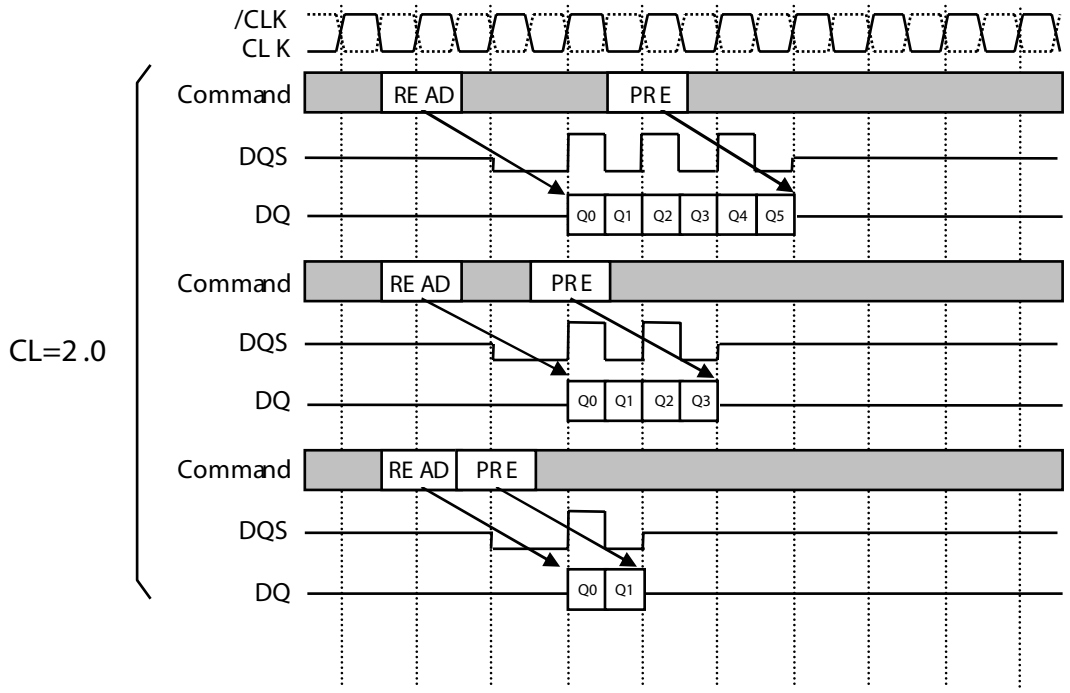
**Read Interrupted by Read (BL=8, CL=2)**




### Read Interrupted by precharge

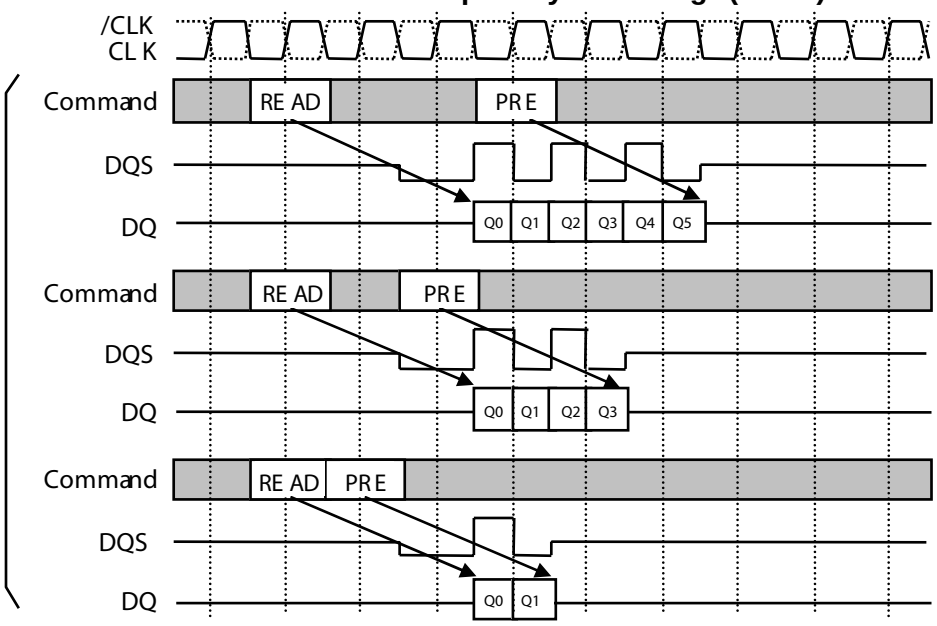
Burst read operation can be interrupted by precharge of the same bank. READ to PRE interval is minimum 1 CLK. A PRE command to output disable latency is equivalent to the /CAS Latency. As a result, READ to PRE interval determines valid data length to be output. The figure below shows examples of BL=8.

**Read Interrupted by Precharge (BL=8)**



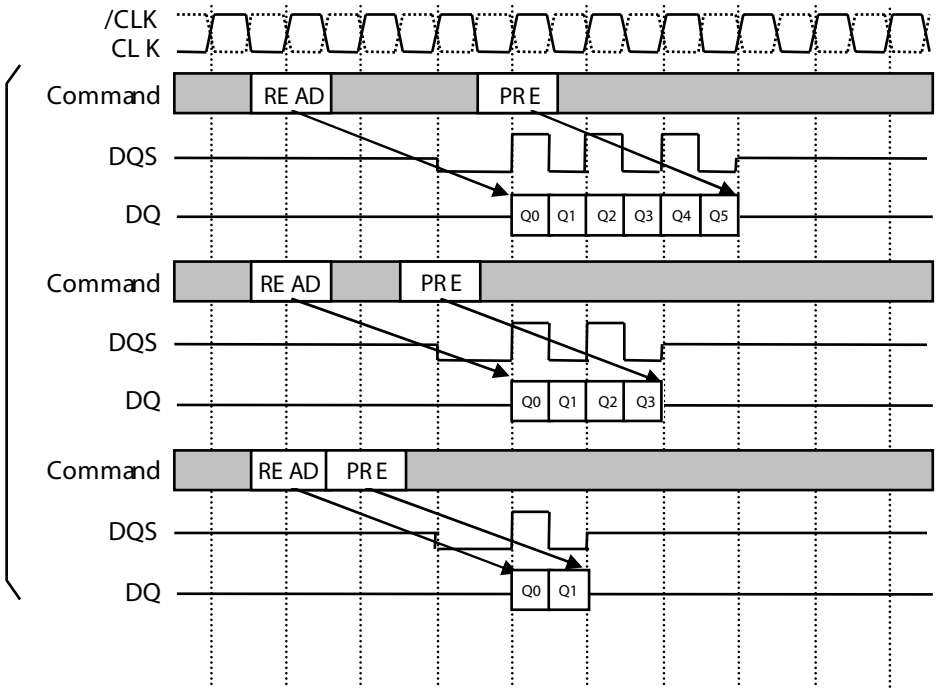
**Read Interrupted by Precharge (BL=8)**

CL=2.5




**Read Interrupted by Precharge (BL=8)**

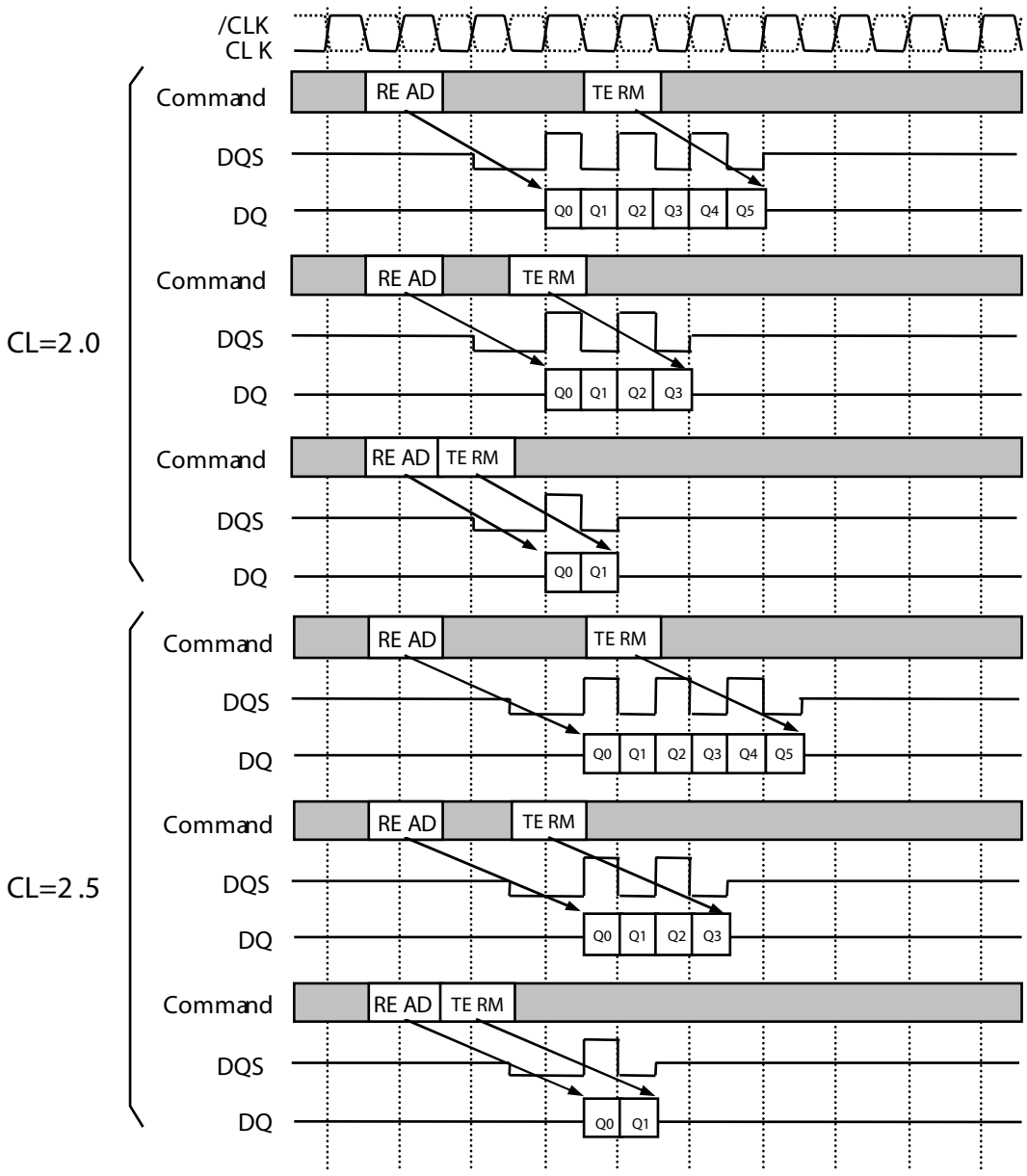
CL=3.0



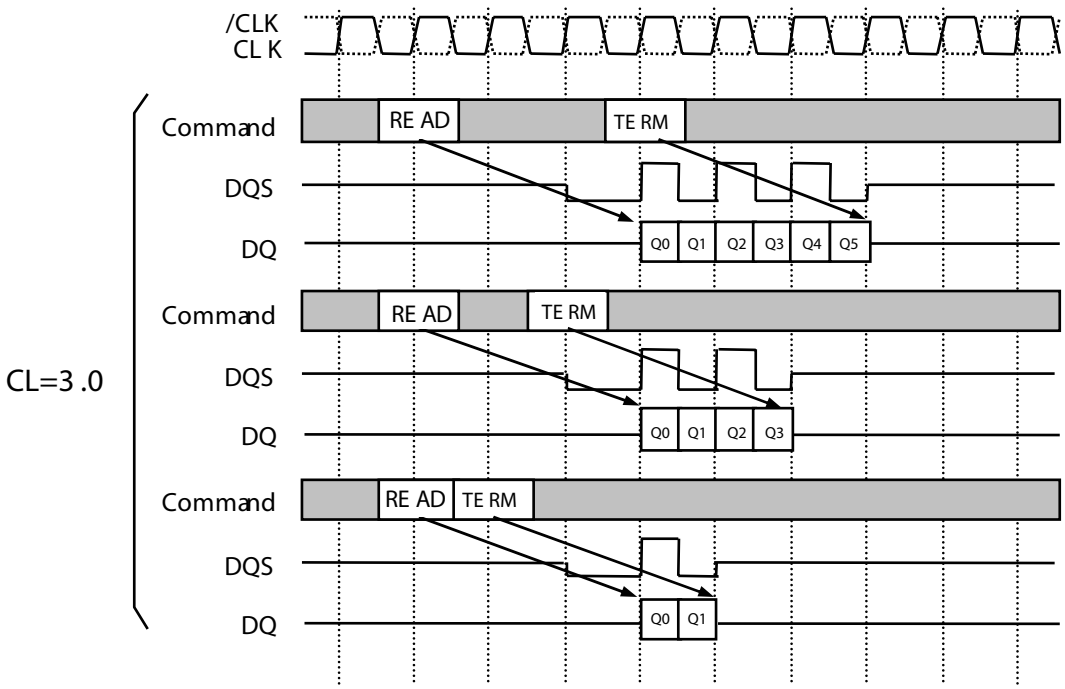
### Read Interrupted by Burst Stop

Burst read operation can be interrupted by a burst stop command(TERM). READ to TERM interval is minimum 1 CLK. A TERM command to output disable latency is equivalent to the /CAS Latency. As a result, READ to TERM interval determines valid data length to be output. The figure below shows examples of BL=8.

**Read Interrupted by TERM (BL=8)**

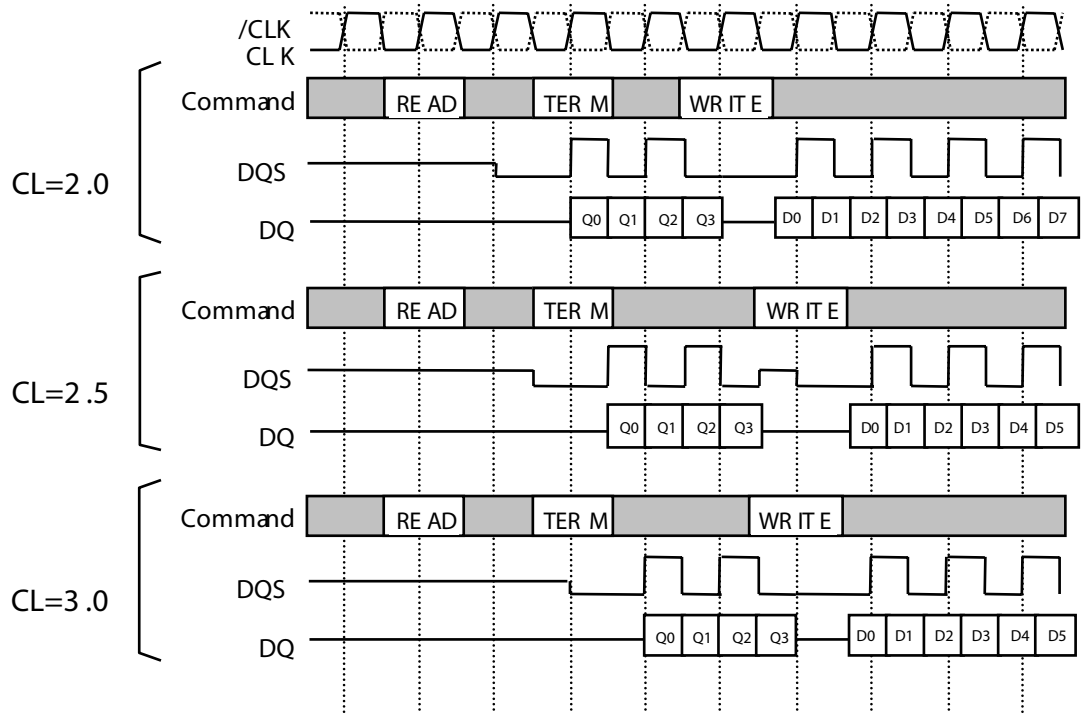


**Read Interrupted by TERM (BL =8)**




**Read Interrupted by Write with TERM**

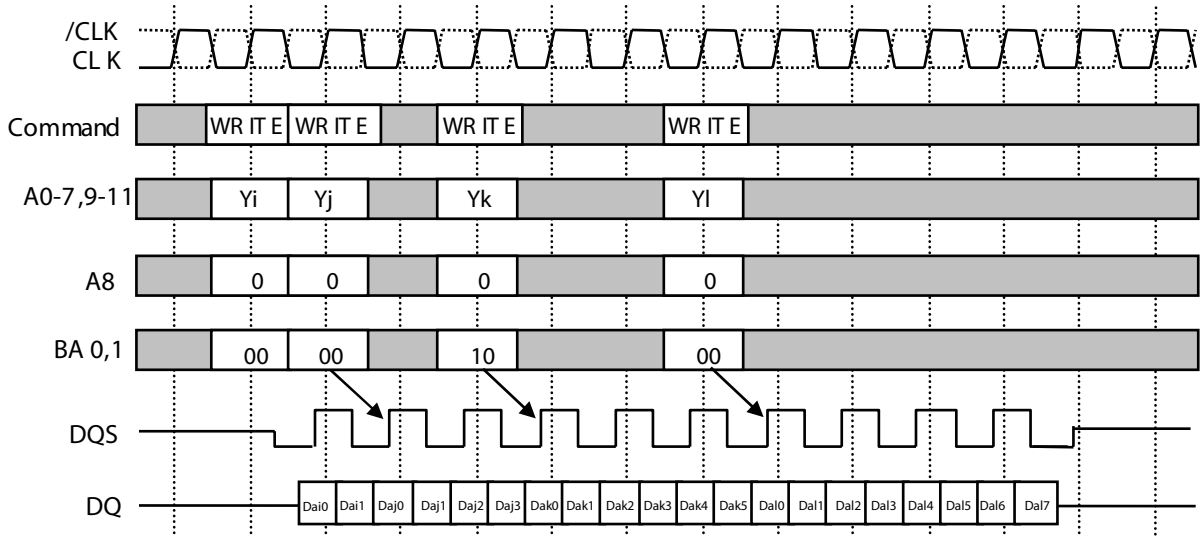
**Read Interrupted by TERM (BL =8)**



### Write interrupted by Write

Burst write operation can be interrupted by write of any bank. Random column access is allowed. WRITE to WRITE interval is minimum 1 CLK.

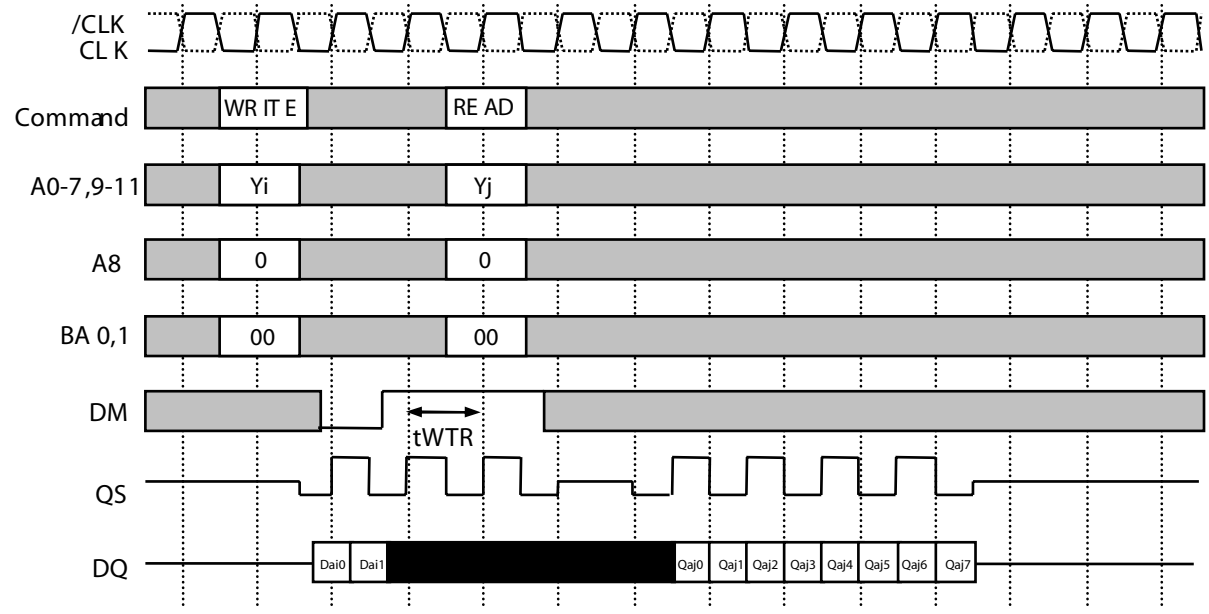
**Write Interrupted by Write (BL=8)**




### Write interrupted by Read

Burst write operation can be interrupted by read of the same or the other bank. Random column access is allowed. Internal WRITE to READ command interval(tWTR) is minimum 1 CLK. The input data on DQ at the interrupting READ cycle is "don't care". tWTR is referenced from the first positive edge after the last data input.

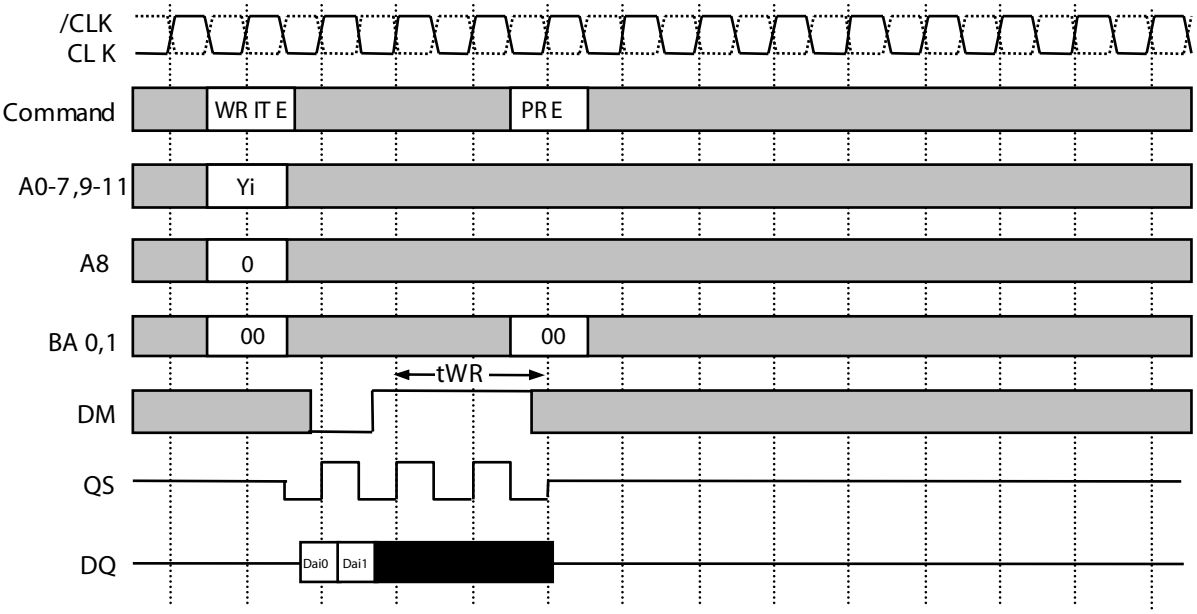
**Write Interrupted by Read (BL=8, CL=2.5)**



### Write interrupted by Precharge

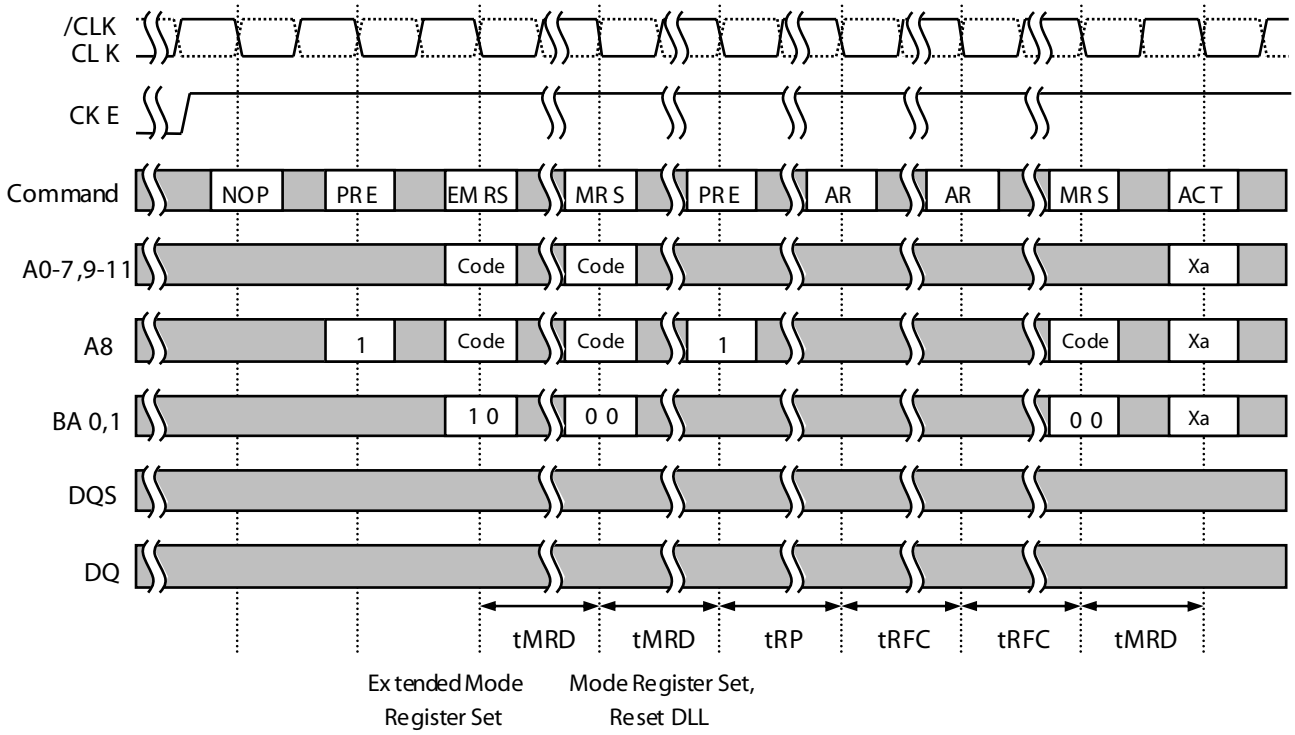
Burst write operation can be interrupted by precharge of the same or all bank. Random column access is allowed. tWR is referenced from the first positive CLK edge after the last data input.

**Write Interrupted by Precharge (BL=8, CL=2.5)**



### Initialize and Mode Register sets

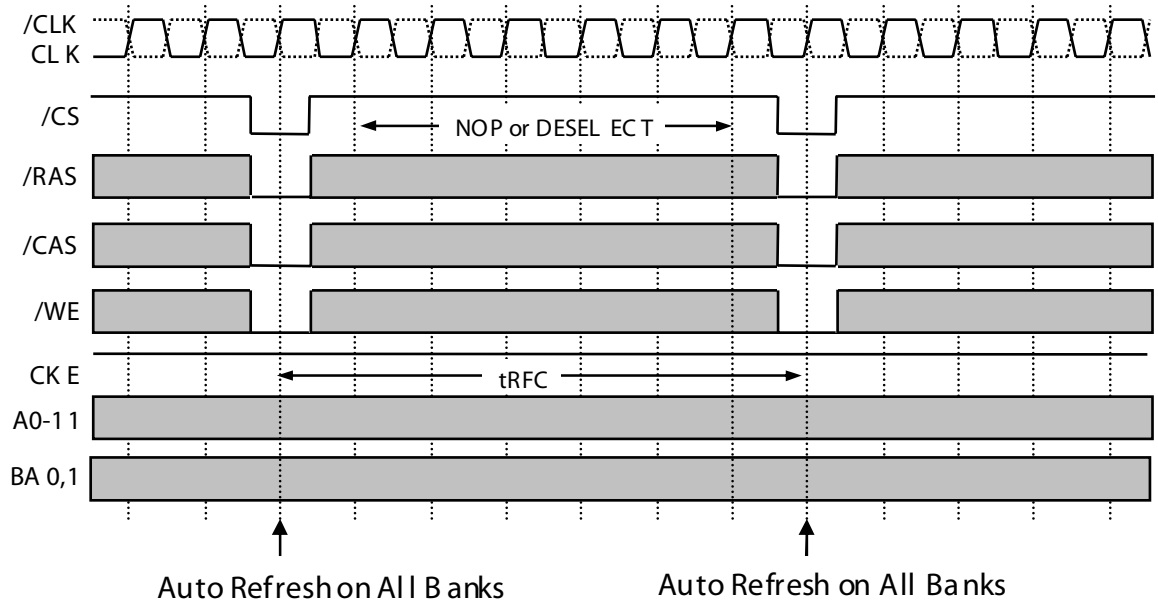
**Initialize and MRS**




### AUTO REFRESH

Single cycle of auto-refresh is initiated with a REFA( /CS=/RAS=/CAS=L, /WE=CKE=H) command. The refresh address is generated internally. 4096 REFA cycles within 64ms refresh 256Mbits memory cells. The auto-refresh is performed on 4 banks concurrently. Before performing an auto refresh, all banks must be in the idle state. Auto-refresh to auto-refresh interval is minimum tRFC . Any command must not be supplied to the device before tRFC from the REFA command.

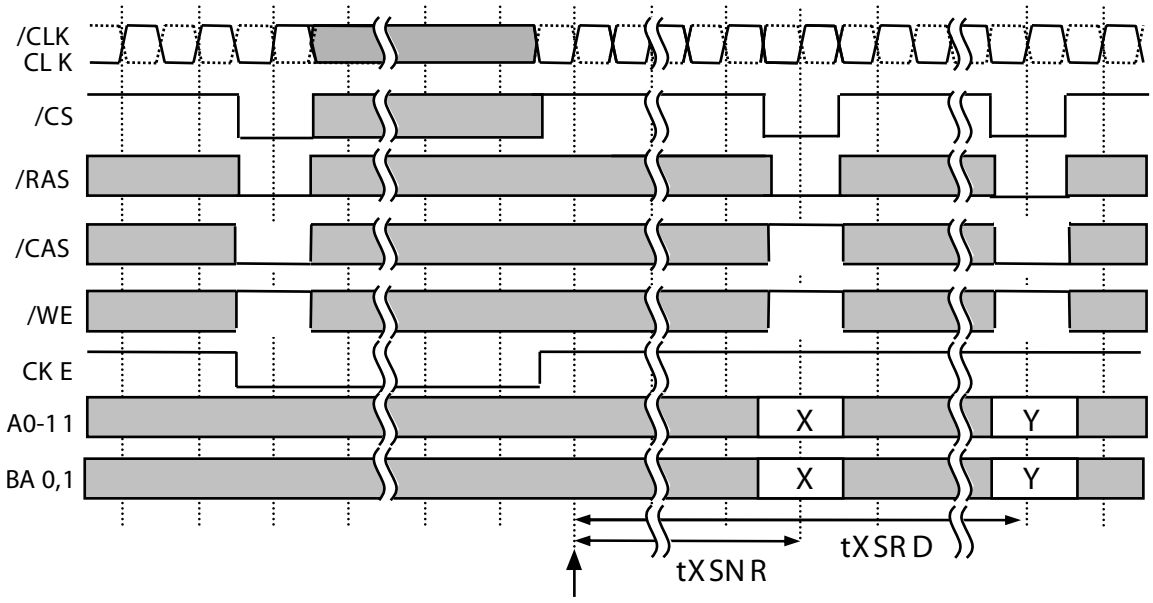
**Auto-Refresh**



## SELF REFRESH

Self-refresh mode is entered by issuing a REFS command (/CS=/RAS=/CAS=L,/WE=H,CKE=L). Once the self-refresh is initiated, it is maintained as long as CKE is kept low. During the self-refresh mode, CKE is asynchronous and the only enable input; all other inputs including CLK are disabled and ignored, so that power consumption due to synchronous inputs is saved. To exit the self-refresh, supplying stable CLK inputs, asserting DESEL or NOP command and then asserting CKE for longer than tXSNR/ tXSRD.

**Self-Refresh**

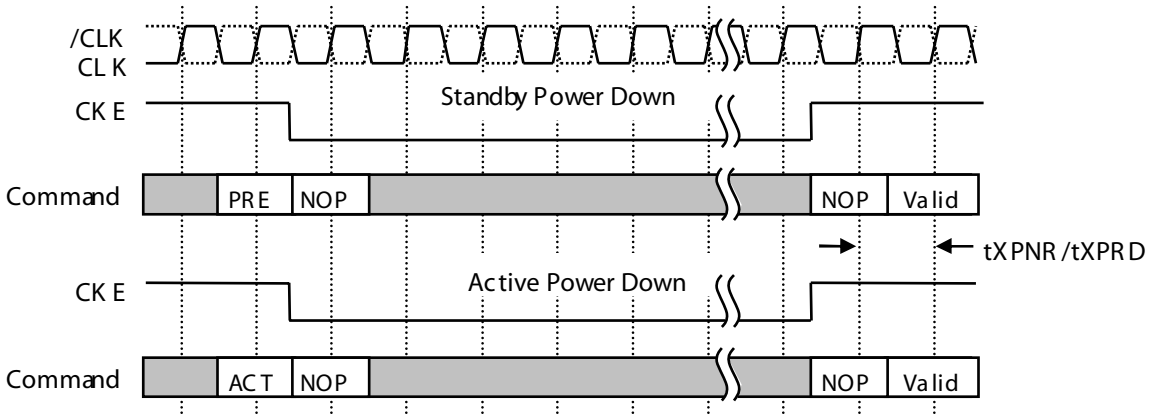



Self Refresh Exit

### Power DOWN

The purpose of CLK suspend is power down. CKE is synchronous input except during the self-refresh mode. A command at cycle is ignored. From CKE =H to normal function, DLL recovery time is NOT required in the condition of the stable CLK operation during the power down mode.

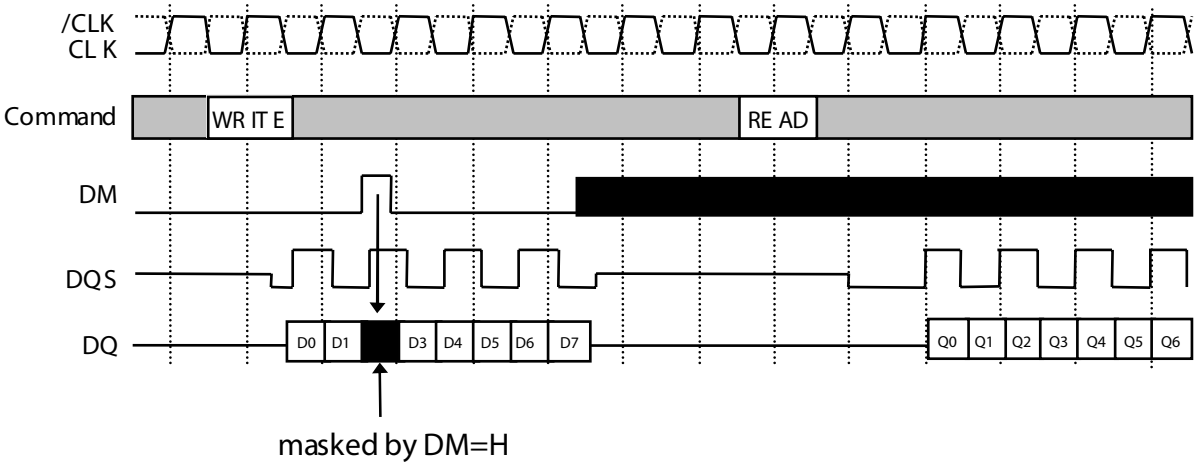
**Power Down by CKE**




### DMCONTROL

DM is defined as the data mask for writes. During writes, DM masks input data word by word. DM to write mask latency is 0.

**DM Function(BL=8, CL=2 )**



## ORDERING INFORMATION - $V_{DD}$ = 2.5V

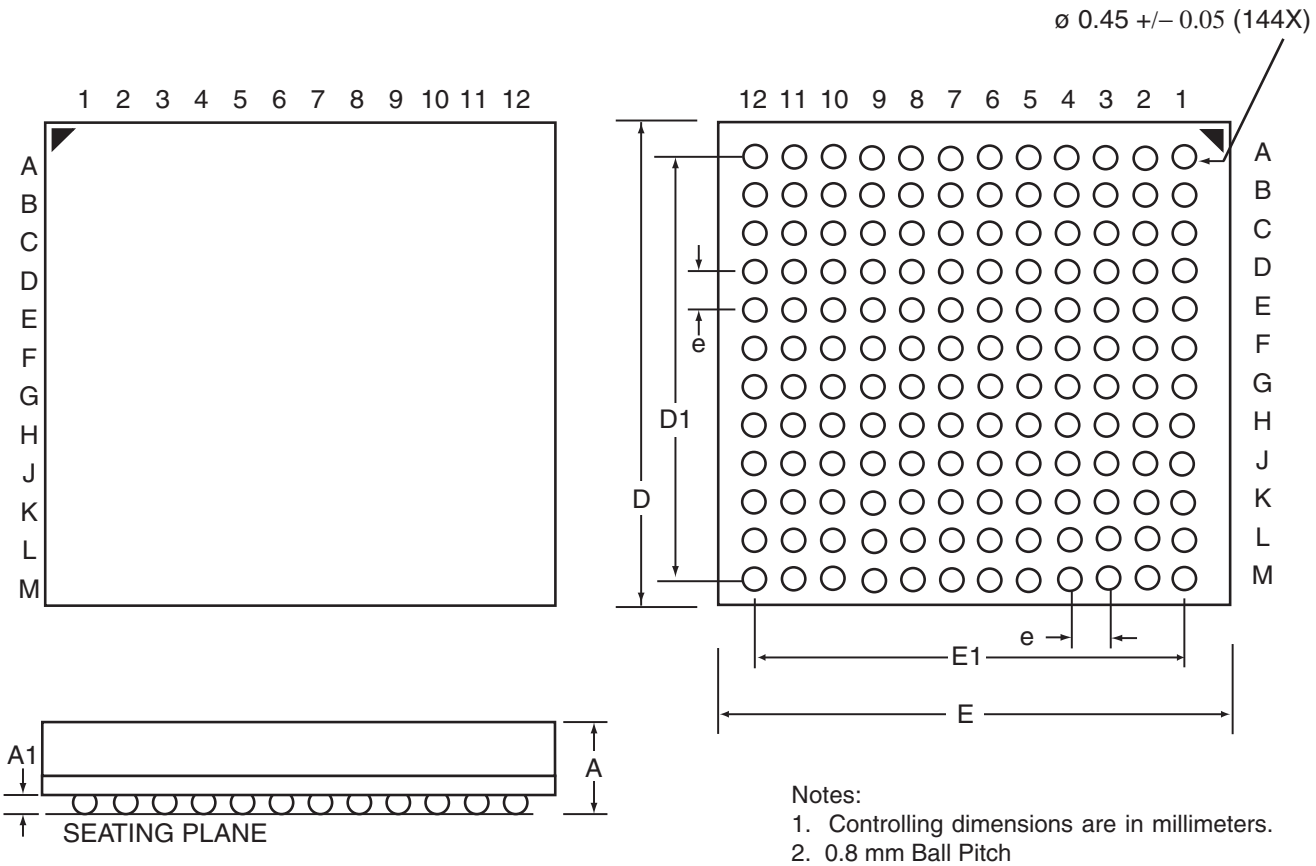
### Commercial Range: 0°C to +70°C

| Frequency | Speed (ns) | Order Part No. | Organization | Package |
|---|---|---|---|---|
| 200 MHz | 5 | IS43R32800B-5B | 8Mx32 | 144-ball fBGA |
| 200 MHz | 5 | IS43R32800B-5BL | 8Mx32 | 144-ball fBGA, Lead-free |
| 166 MHz | 6 | IS43R32800B-6B | 8Mx32 | 144-ball fBGA |
| 166 MHz | 6 | IS43R32800B-6BL | 8Mx32 | 144-ball fBGA, Lead-free |
| 133 MHz | 7.5 | IS43R32800B-75B | 8Mx32 | 144-ball fBGA |
| 133 MHz | 7.5 | IS43R32800B-75BL | 8Mx32 | 144-ball fBGA, Lead-free |

### Industrial Range: -40°C to +85°C

| Frequency | Speed (ns) | Order Part No. | Organization | Package |
|---|---|---|---|---|
| 200 MHz | 5 | IS43R32800B-5BI | 8Mx32 | 144-ball fBGA |
| 200 MHz | 5 | IS43R32800B-5BLI | 8Mx32 | 144-ball fBGA, Lead-free |
| 166 MHz | 6 | IS43R32800B-6BI | 8Mx32 | 144-ball fBGA |
| 166 MHz | 6 | IS43R32800B-6BLI | 8Mx32 | 144-ball fBGA, Lead-free |
| 133 MHz | 7.5 | IS43R32800B-75BI | 8Mx32 | 144-ball fBGA |
| 133 MHz | 7.5 | IS43R32800B-75BLI | 8Mx32 | 144-ball fBGA, Lead-free |

## Mini Ball Grid Array
## Package Code: B (144-Ball)




Notes:
1. Controlling dimensions are in millimeters.
2. 0.8 mm Ball Pitch

### mBGA - 12mm x 12mm

| | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| **Sym.** | **Min.** | **Typ.** | **Max.** | **Min.** | **Typ.** | **Max.** |
| N0. Leads | | **144** | | | | |
| A | 1.17 | 1.25 | 1.40 | 0.046 | 0.049 | 0.055 |
| A1 | 0.32 | 0.35 | 0.38 | 0.013 | 0.014 | 0.015 |
| D | 11.95 | 12.00 | 12.05 | 0.470 | 0.472 | 0.474 |
| D1 | — | 8.80 | — | — | 0.346 | — |
| E | 11.95 | 12.00 | 12.05 | 0.470 | 0.472 | 0.474 |
| E1 | — | 8.80 | — | — | 0.346 | — |
| e | — | 0.80 | — | — | 0.031 | — |

# Mouser Electronics

Authorized Distributor

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ISSI:
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