



August 2000

QFET™

FQB70N10 / FQI70N10

100V N-Channel MOSFET

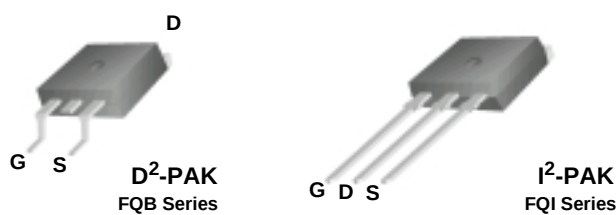
General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for low voltage applications such as audio amplifier, high efficiency switching DC/DC converters, and DC motor control.

Features

- 57A, 100V, $R_{DS(on)} = 0.023\Omega$ @ $V_{GS} = 10V$
- Low gate charge (typical 85 nC)
- Low C_{rss} (typical 150 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- 175°C maximum junction temperature rating



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FQB70N10 / FQI70N10	Units
V_{DSS}	Drain-Source Voltage	100	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$)	57	A
	- Continuous ($T_C = 100^\circ\text{C}$)	40.3	A
I_{DM}	Drain Current - Pulsed (Note 1)	228	A
V_{GSS}	Gate-Source Voltage	± 25	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	1300	mJ
I_{AR}	Avalanche Current (Note 1)	57	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	16	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	6.0	V/ns
P_D	Power Dissipation ($T_A = 25^\circ\text{C}$) *	3.75	W
	Power Dissipation ($T_C = 25^\circ\text{C}$)	160	W
	- Derate above 25°C	1.06	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +175	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	0.94	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	--	40	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	62.5	$^\circ\text{C/W}$

* When mounted on the minimum pad size recommended (PCB Mount)

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	100	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C	--	0.1	--	V/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	μA
		$V_{DS} = 80\text{ V}, T_C = 150^\circ\text{C}$	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 25\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -25\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 28.5\text{ A}$	--	0.019	0.023	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 28.5\text{ A}$ (Note 4)	--	45	--	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	2500	3300	pF
C_{oss}	Output Capacitance		--	720	940	pF
C_{rss}	Reverse Transfer Capacitance		--	150	200	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{ V}, I_D = 70\text{ A},$ $R_G = 25\text{ }\Omega$ (Note 4, 5)	--	30	70	ns
t_r	Turn-On Rise Time		--	470	950	ns
$t_{d(off)}$	Turn-Off Delay Time		--	130	270	ns
t_f	Turn-Off Fall Time		--	160	330	ns
Q_g	Total Gate Charge	$V_{DS} = 80\text{ V}, I_D = 70\text{ A},$ $V_{GS} = 10\text{ V}$ (Note 4, 5)	--	85	110	nC
Q_{gs}	Gate-Source Charge		--	16	--	nC
Q_{gd}	Gate-Drain Charge		--	42	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I _S	Maximum Continuous Drain-Source Diode Forward Current		--	--	57	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	228	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 57 A	--	--	1.5	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 70 A,	--	110	--	ns
Q _{rr}	Reverse Recovery Charge	dI _F / dt = 100 A/μs (Note 4)	--	430	--	nC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L = 0.6\text{ mH}$, $I_{AS} = 57\text{ A}$, $V_{DD} = 25\text{ V}$, $R_G = 25\text{ }\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 70\text{ A}$, $di/dt \leq 300\text{ A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
5. Essentially independent of operating temperature

Typical Characteristics

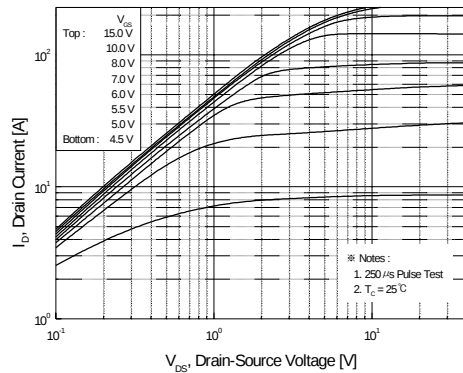


Figure 1. On-Region Characteristics

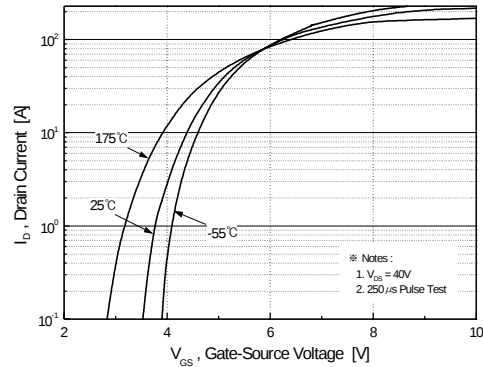


Figure 2. Transfer Characteristics

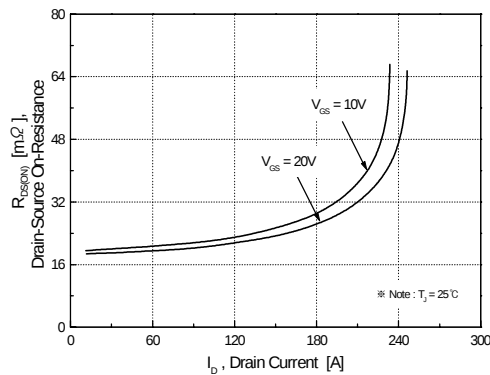


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

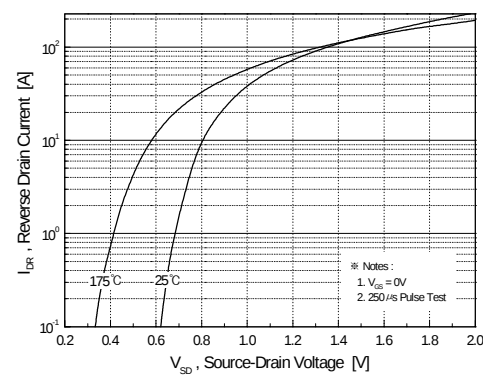


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

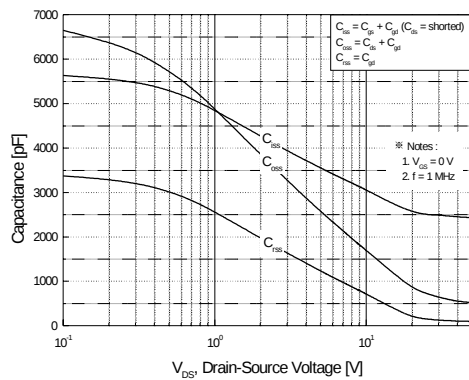


Figure 5. Capacitance Characteristics

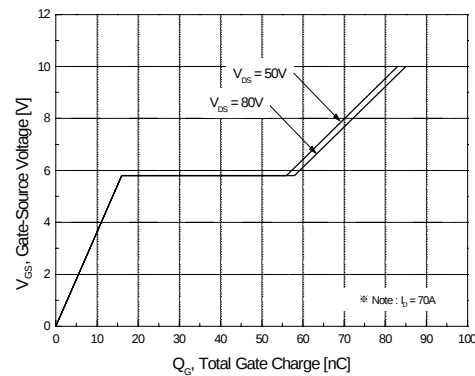


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

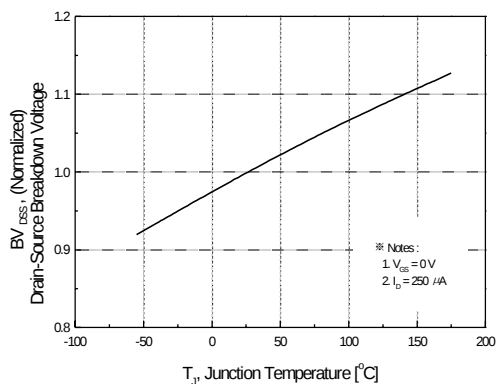


Figure 7. Breakdown Voltage Variation vs. Temperature

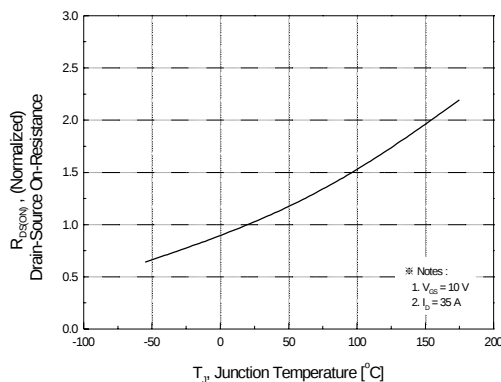


Figure 8. On-Resistance Variation vs. Temperature

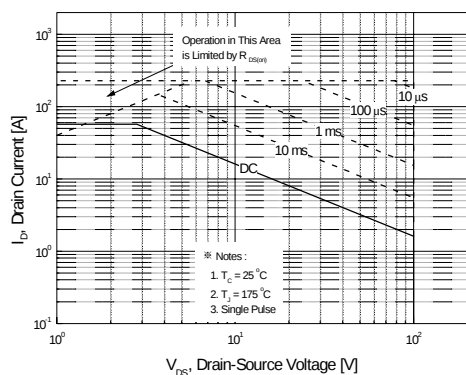


Figure 9. Maximum Safe Operating Area

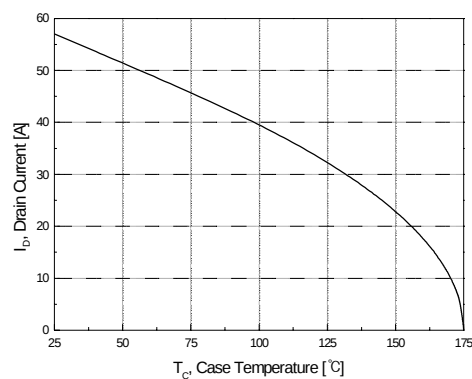


Figure 10. Maximum Drain Current vs. Case Temperature

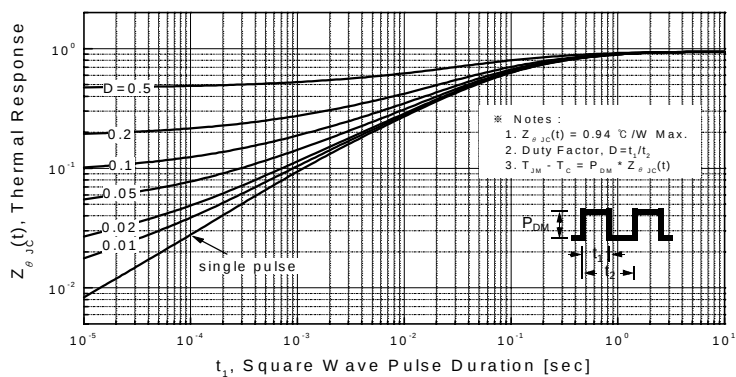


Figure 11. Transient Thermal Response Curve

Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms



Technical drawing of a 10-pin D-sub connector showing front, side, and top views with dimensions in millimeters.

Front View Dimensions:

- Overall Width: 9.90 ± 0.20
- Pin Spacing (Typical): 2.54 TYP
- Pin 1 to Pin 5 Distance: 1.27 ± 0.10
- Pin 5 to Pin 10 Distance: 0.80 ± 0.10
- Pin 1 to Pin 10 Distance: 1.40 ± 0.20
- Pin 1 to Pin 5 Distance: 1.20 ± 0.20
- Pin 5 to Pin 10 Distance: 9.20 ± 0.20
- Pin 1 to Pin 10 Distance: 15.30 ± 0.30
- Pin 1 to Pin 5 Distance: 4.90 ± 0.20

Side View Dimensions:

- Overall Height: 4.50 ± 0.20
- Pin 1 to Pin 5 Distance: $1.30^{+0.10}_{-0.05}$
- Pin 5 to Pin 10 Distance: 0.10 ± 0.15
- Pin 1 to Pin 5 Distance: 2.00 ± 0.10
- Pin 5 to Pin 10 Distance: 2.40 ± 0.20
- Pin 1 to Pin 5 Distance: 2.54 ± 0.30
- Pin 5 to Pin 10 Distance: $0.50^{+0.10}_{-0.05}$
- Pin 1 to Pin 5 Distance: 0.75
- Pin 5 to Pin 10 Distance: $0^\circ \sim 3^\circ$

Top View Dimensions:

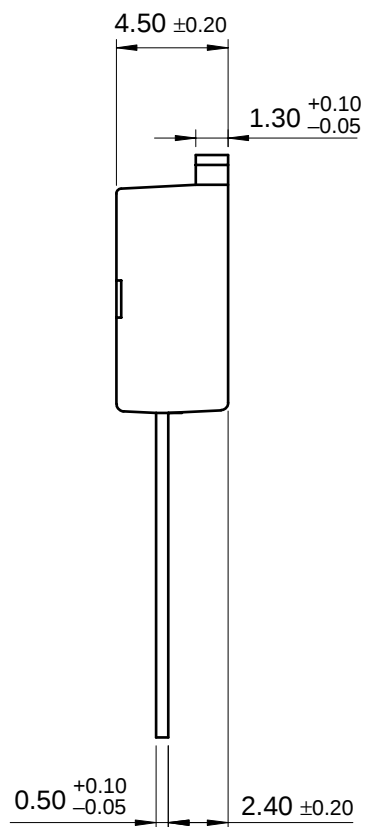
- Overall Width: 10.00 ± 0.20
- Pin 1 to Pin 5 Distance: 10.00 ± 0.20

Bottom View Dimensions:

- Overall Width: 10.00 ± 0.20
- Pin 1 to Pin 5 Distance: 10.00 ± 0.20
- Pin 5 to Pin 10 Distance: 0.80 ± 0.10
- Pin 1 to Pin 5 Distance: 15.30 ± 0.30
- Pin 5 to Pin 10 Distance: 9.20 ± 0.20
- Pin 1 to Pin 5 Distance: 4.90 ± 0.20
- Pin 5 to Pin 10 Distance: 0.75
- Pin 1 to Pin 5 Distance: 1.75
- Pin 5 to Pin 10 Distance: 7.20
- Pin 1 to Pin 5 Distance: 10.00 ± 0.20
- Pin 5 to Pin 10 Distance: 8.00
- Pin 1 to Pin 5 Distance: 4.40
- Pin 5 to Pin 10 Distance: $(2XR0.45)$

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Technical drawing of a 3-pin connector. The drawing shows a top view and a side view. The top view dimensions are: overall width 9.90 ± 0.20 mm, overall height 13.08 ± 0.20 mm, pin pitch 2.54 TYP, pin diameter 1.27 ± 0.10 mm, pin length 1.47 ± 0.10 mm, and pin thickness 0.80 ± 0.10 mm. The side view dimensions are: overall height 13.40 mm, pin length 9.20 ± 0.20 mm, pin diameter 1.20 ± 0.20 mm, and pin thickness 1.20 ± 0.20 mm. The drawing also includes a 45° chamfer on the pin and a 0.40 mm dimension for the top of the connector body.



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