



# BUK9E04-30B

N-channel TrenchMOS logic level FET

Rev. 02 — 16 February 2011

Product data sheet

## 1. Product profile

### 1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

### 1.2 Features and benefits

- AEC Q101 compliant
- Low conduction losses due to low on-state resistance
- Suitable for logic level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

### 1.3 Applications

- 12 V loads
- Automotive systems
- General purpose power switching
- Motors, lamps and solenoids

### 1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25 \text{ }^\circ\text{C}; T_j \leq 175 \text{ }^\circ\text{C}$	-	-	30	V
$I_D$	drain current	$V_{GS} = 5 \text{ V}; T_{mb} = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a>	[1]	-	-	75 A
$P_{tot}$	total power dissipation	$T_{mb} = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 2</a>	-	-	254	W
Static characteristics						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A};$ $T_j = 25 \text{ }^\circ\text{C}$	-	2.7	3	$\text{m}\Omega$
		$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A};$ $T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 11</a> ; see <a href="#">Figure 12</a>	-	3.4	4	$\text{m}\Omega$



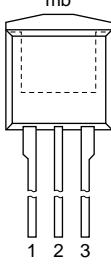
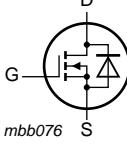
**Table 1.** Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 75 \text{ A}$ ; $V_{sup} \leq 30 \text{ V}$ ; $R_{GS} = 50 \Omega$ ; $V_{GS} = 5 \text{ V}$ ; $T_{j(init)} = 25 \text{ }^\circ\text{C}$ ; unclamped	-	-	1.3	J
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 5 \text{ V}$ ; $I_D = 25 \text{ A}$ ; $V_{DS} = 24 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 13</a>	-	22	-	nC

[1] Continuous current is limited by package.

## 2. Pinning information

**Table 2.** Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

**SOT226 (I2PAK)**

## 3. Ordering information

**Table 3.** Ordering information

Type number	Package		
	Name	Description	Version
BUK9E04-30B	I2PAK	plastic single-ended package (I2PAK); TO-262	SOT226

## 4. Limiting values

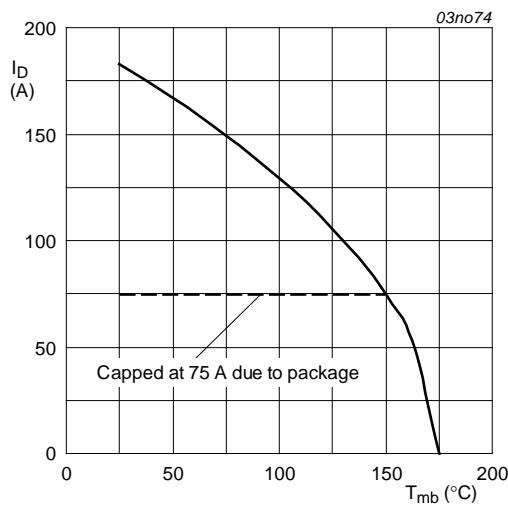
**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25^\circ\text{C}; T_j \leq 175^\circ\text{C}$	-	30	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	30	V
$V_{GS}$	gate-source voltage		-15	15	V
$I_D$	drain current	$T_{mb} = 100^\circ\text{C}; V_{GS} = 5\text{ V}$ ; see <a href="#">Figure 1</a>	[1] -	75	A
		$T_{mb} = 25^\circ\text{C}; V_{GS} = 5\text{ V}$ ; see <a href="#">Figure 1</a> ; <a href="#">see Figure 3</a>	[2] -	183	A
			[1] -	75	A
$I_{DM}$	peak drain current	$T_{mb} = 25^\circ\text{C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; <a href="#">see Figure 3</a>	-	732	A
$P_{tot}$	total power dissipation	$T_{mb} = 25^\circ\text{C}$ ; see <a href="#">Figure 2</a>	-	254	W
$T_{stg}$	storage temperature		-55	175	°C
$T_j$	junction temperature		-55	175	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25^\circ\text{C}$	[1] -	75	A
			[2] -	183	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}; T_{mb} = 25^\circ\text{C}$	-	732	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 75\text{ A}; V_{sup} \leq 30\text{ V}; R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 5\text{ V}; T_{j(init)} = 25^\circ\text{C}$ ; unclamped	-	1.3	J

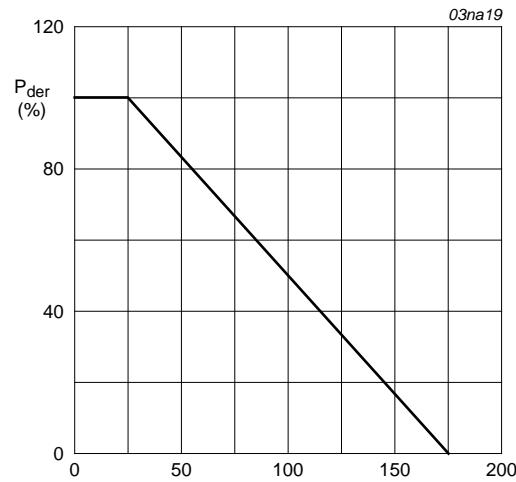
[1] Continuous current is limited by package.

[2] Current is limited by power dissipation chip rating.



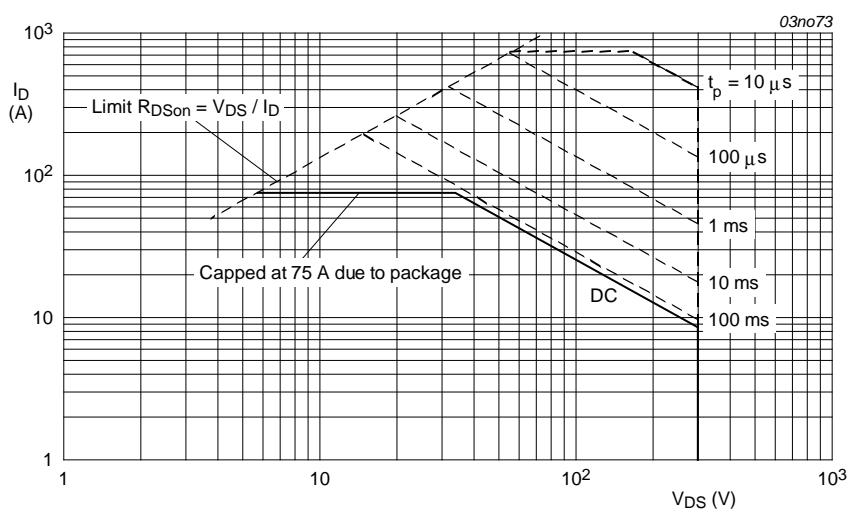
$$V_{GS} \geq 5\text{ V}$$

**Fig 1. Normalized continuous drain current as a function of mounting base temperature**



$$P_{der} = \frac{P_{tot}}{P_{tot}(25^\circ\text{C})} \times 100\text{ %}$$

**Fig 2. Normalized total power dissipation as a function of mounting base temperature**



$T_{mb} = 25^\circ\text{C}$ ;  $I_{DM}$  is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	-	0.59	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in still air	-	60	-	K/W

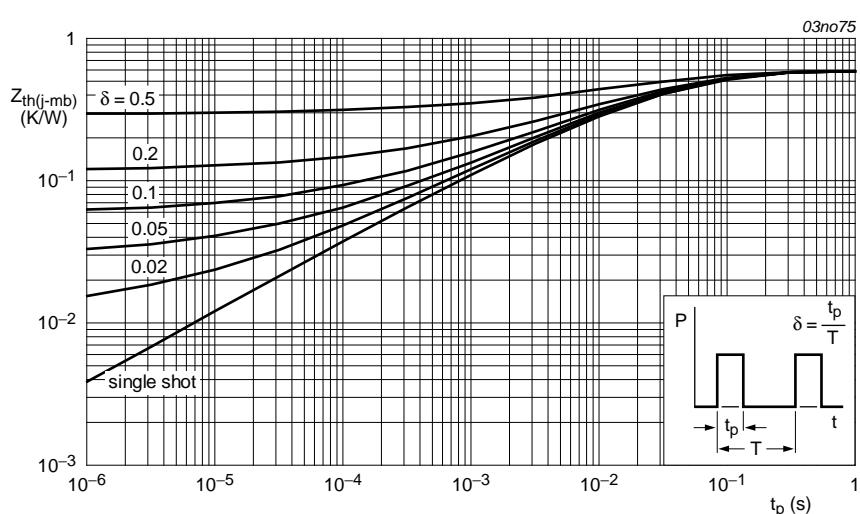


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

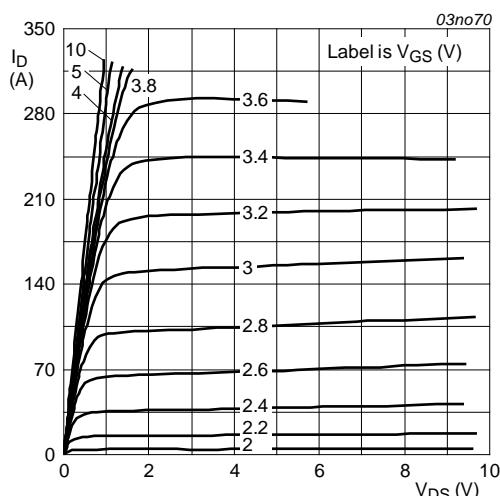
## 6. Characteristics

**Table 6. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ $I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	30	-	-	V
$V_{GS(\text{th})}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 10</a> $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ see <a href="#">Figure 10</a> $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see <a href="#">Figure 10</a>	1.1	1.5	2	V
$I_{DSS}$	drain leakage current	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$ $V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	500	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 15 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ $V_{GS} = -15 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$ $V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$ $V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ see <a href="#">Figure 11</a> ; see <a href="#">Figure 12</a> $V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 11</a> ; see <a href="#">Figure 12</a>	-	-	4.4	$\text{m}\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(\text{tot})}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 24 \text{ V}; V_{GS} = 5 \text{ V};$	-	56	-	nC
$Q_{GS}$	gate-source charge	$T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 13</a>	-	10	-	nC
$Q_{GD}$	gate-drain charge		-	22	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$	-	4895	6526	pF
$C_{oss}$	output capacitance	$T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 14</a>	-	1257	1508	pF
$C_{rss}$	reverse transfer capacitance		-	527	721	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 1.2 \text{ } \Omega; V_{GS} = 5 \text{ V};$	-	30	-	ns
$t_r$	rise time	$R_{G(\text{ext})} = 10 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}$	-	76	-	ns
$t_{d(off)}$	turn-off delay time		-	236	-	ns
$t_f$	fall time		-	143	-	ns
$L_D$	internal drain inductance	from upper edge of drain mounting base to centre of die; $T_j = 25 \text{ }^\circ\text{C}$	-	2.5	-	nH
		from drain lead 6 mm from package to centre of die; $T_j = 25 \text{ }^\circ\text{C}$	-	4.5	-	nH
$L_S$	internal source inductance	from source lead to source bond pad; $T_j = 25 \text{ }^\circ\text{C}$	-	7.5	-	nH

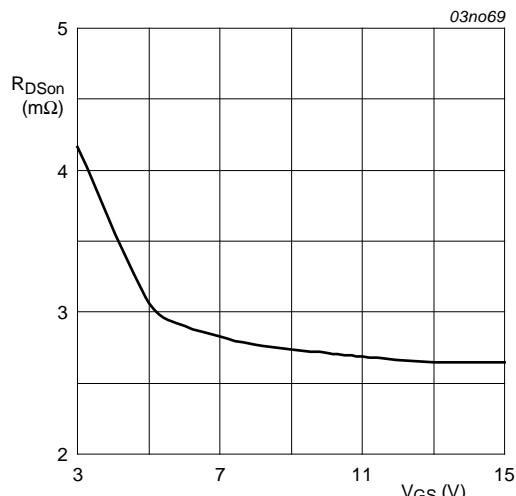
Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 40 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 15</a>	-	0.85	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s}$	-	68	-	ns
$Q_r$	recovered charge	$V_{GS} = -10 \text{ V}; V_{DS} = 20 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	53	-	nC



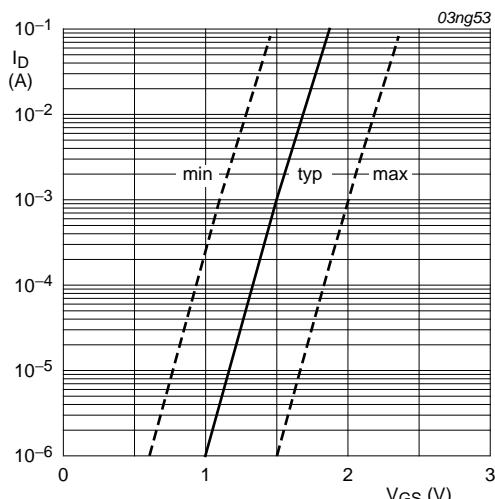
$T_j = 25 \text{ }^\circ\text{C}; t_p = 300 \mu\text{s}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



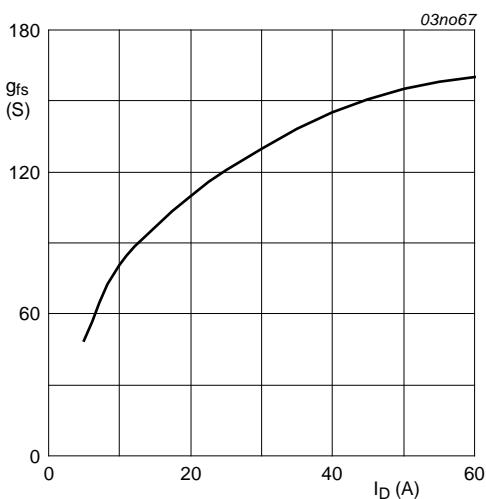
$T_j = 25 \text{ }^\circ\text{C}; I_D = 25 \text{ A}$

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values



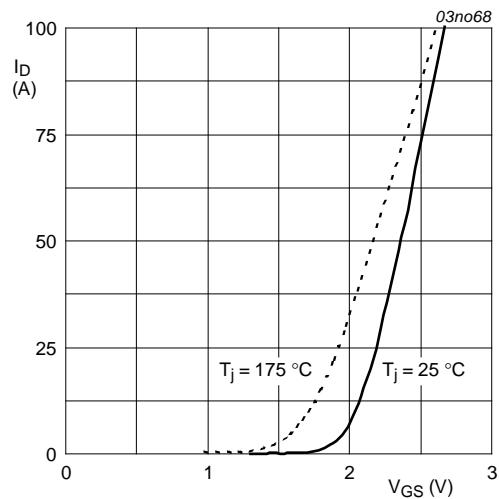
$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = V_{GS}$

Fig 7. Sub-threshold drain current as a function of gate-source voltage



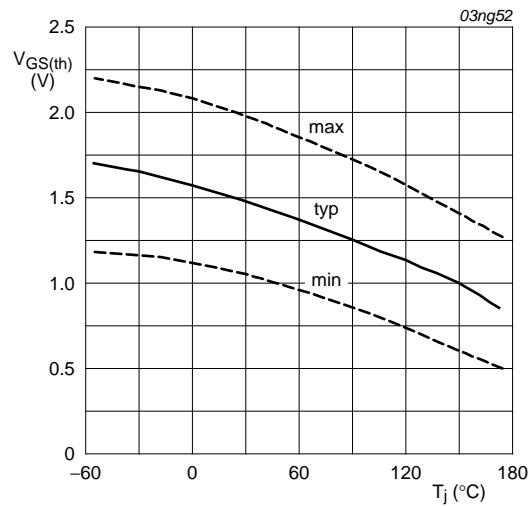
$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = 25 \text{ V}$

Fig 8. Forward transconductance as a function of drain current; typical values



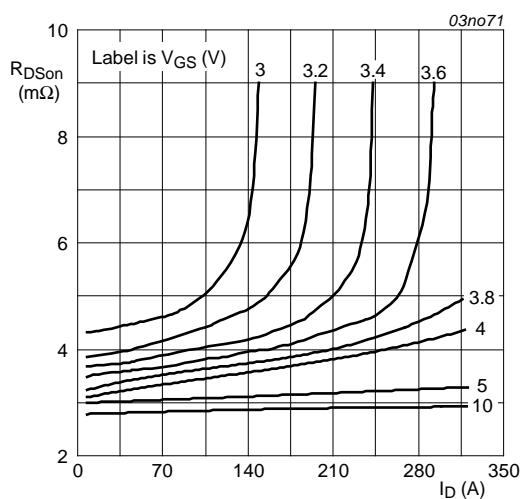
$V_{DS} = 25V$

**Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



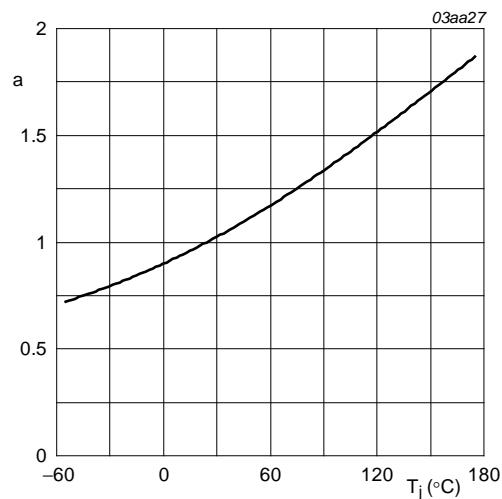
$I_D = 1mA; V_{DS} = V_{GS}$

**Fig 10. Gate-source threshold voltage as a function of junction temperature**



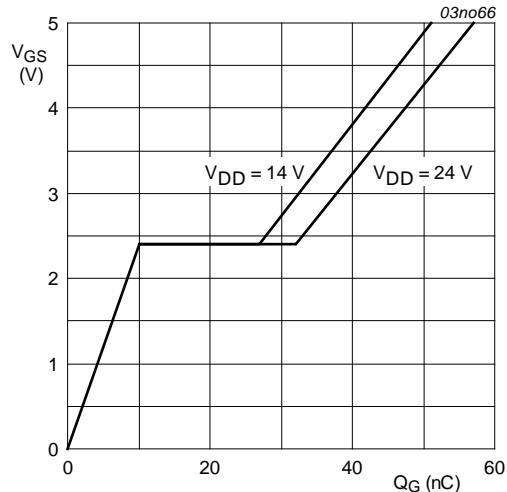
$T_j = 25^{\circ}C$

**Fig 11. Drain-source on-state resistance as a function of drain current; typical values**



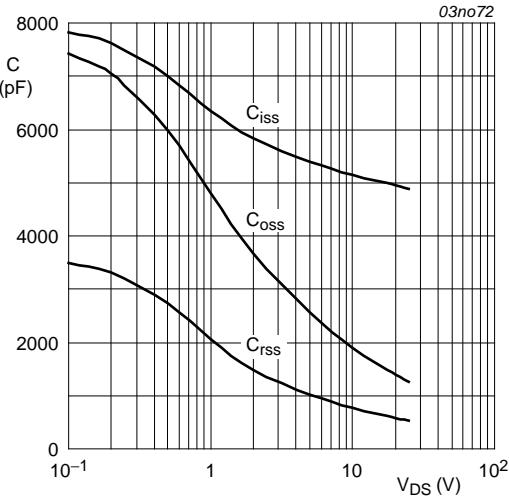
$$a = \frac{R_{DSon}}{R_{DSon}(25^{\circ}C)}$$

**Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature**



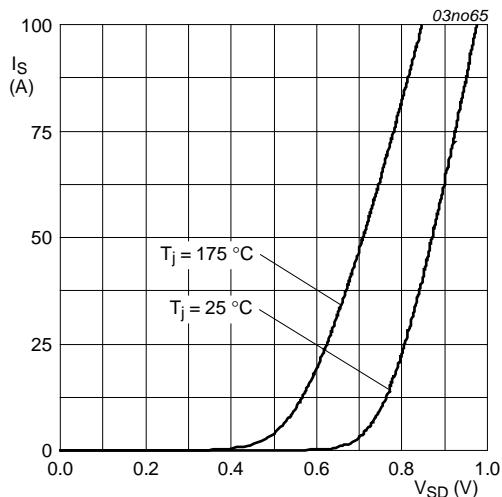
$T_j = 25^\circ\text{C}$ ;  $I_D = 25\text{A}$

**Fig 13. Gate-source voltage as a function of gate charge; typical values**



$V_{GS} = 0\text{V}$ ;  $f = 1\text{MHz}$

**Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



$V_{GS} = 0\text{V}$

**Fig 15. Source current as a function of source-drain voltage; typical values**

## 7. Package outline

Plastic single-ended package (I2PAK); low-profile 3-lead TO-262

SOT226

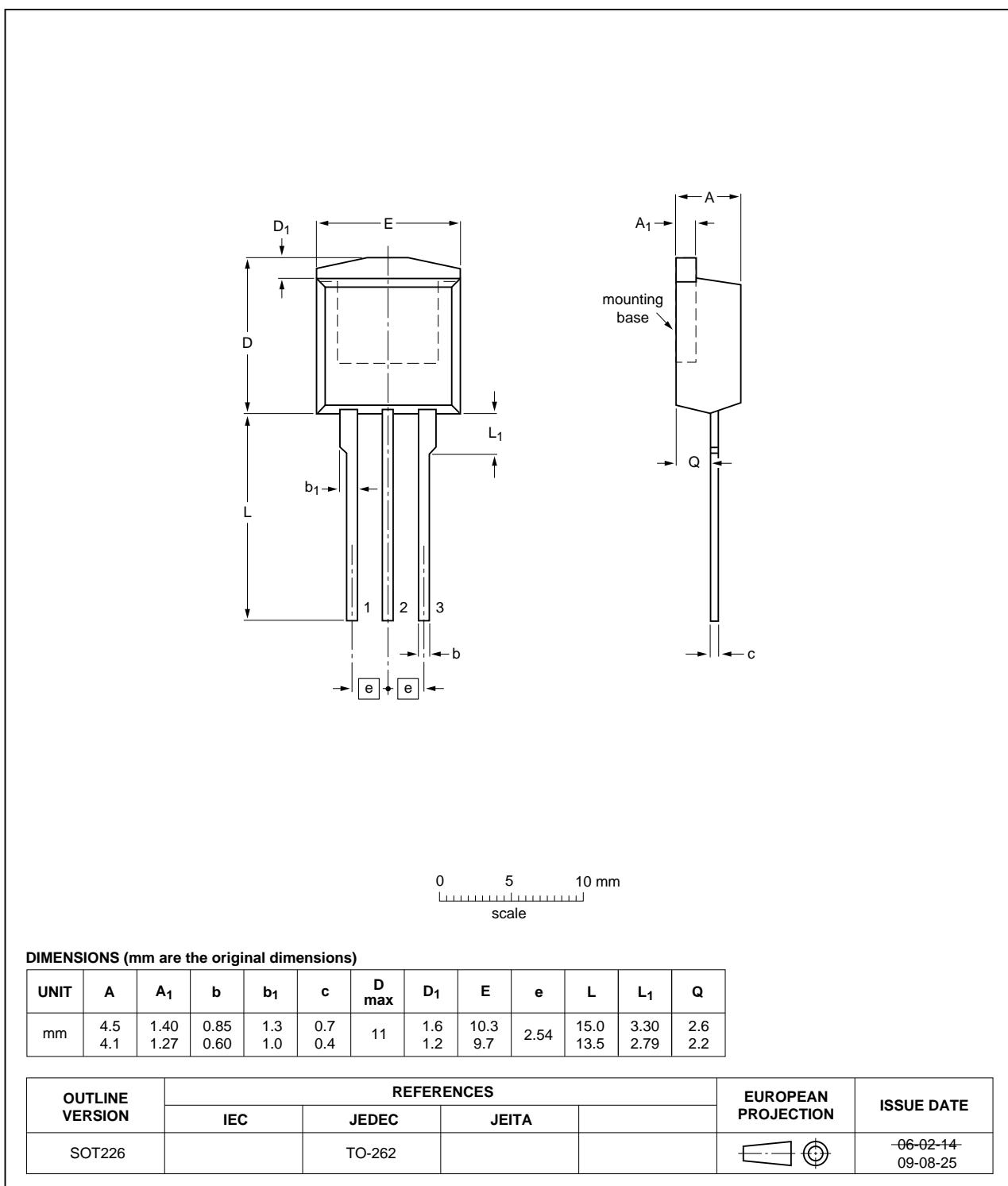


Fig 16. Package outline SOT226 (I2PAK)

## 8. Revision history

**Table 7. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9E04-30B v.2	20110216	Product data sheet	-	BUK9E04-30B v.1
Modifications:	<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li><li>• Various changes to content.</li></ul>			
BUK9E04-30B v.1 (9397 750 12108)	20031114	Product data	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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