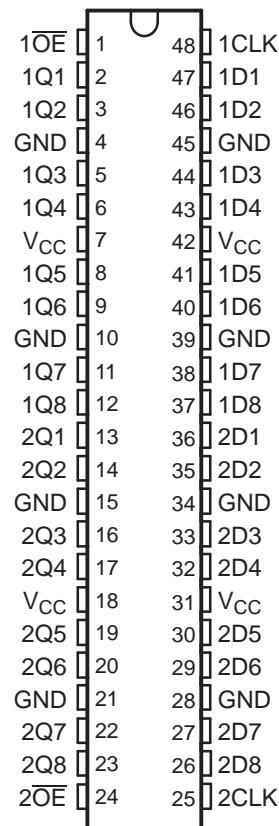


FEATURES

- Members of the Texas Instruments Widebus™ Family
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- I_{off} and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

SN54LVTH16374... WD PACKAGE
 SN74LVTH16374... DGG OR DL PACKAGE
 (TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The 'LVTH16374 devices are 16-bit edge-triggered D-type flip-flops with 3-state outputs designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK), the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

\overline{OE} does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

**SN54LVTH16374, SN74LVTH16374
3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH 3-STATE OUTPUTS**

SCBS145R–MAY 1992–REVISED AUGUST 2007



DESCRIPTION/ORDERING INFORMATION (CONTINUED)

When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $O\bar{E}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

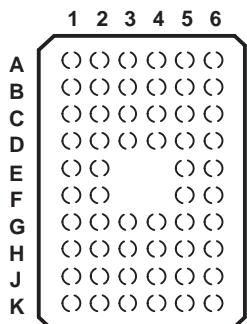
ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	FBGA – GRD	Reel of 1000	SN74LVTH16374GRDR	LL374
	FBGA – ZRD (Pb-free)		SN74LVTH16374ZRDR	
	SSOP – DL	Tube of 25	SN74LVTH16374DL	LVTH16374
			74LVTH16374DLG4	
		Reel of 1000	SN74LVTH16374DLR	
			74LVTH16374DLRG4	
	TSSOP – DGG	Reel of 2000	SN74LVTH16374DGGR	LVTH16374
	VFBGA – GQL		74LVTH16374DGGRG4	
	VFBGA – ZQL (Pb-free)	Reel of 1000	SN74LVTH16374KR	LL374
	CFP – WD		SN74LVTH16374ZQLR	
-55°C to 125°C	Tube	SNJ54LVTH16374WD	SNJ54LVTH16374WD	

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

**GQL OR ZQL PACKAGE
(TOP VIEW)**

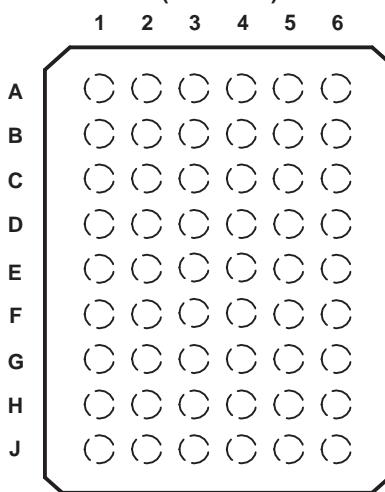


**TERMINAL ASSIGNMENTS⁽¹⁾
(56-Ball GQL/ZQL Package)**

	1	2	3	4	5	6
A	1 \overline{OE}	NC	NC	NC	NC	1CLK
B	1Q2	1Q1	GND	GND	1D1	1D2
C	1Q4	1Q3	V_{CC}	V_{CC}	1D3	1D4
D	1Q6	1Q5	GND	GND	1D5	1D6
E	1Q8	1Q7			1D7	1D8
F	2Q1	2Q2			2D2	2D1
G	2Q3	2Q4	GND	GND	2D4	2D3
H	2Q5	2Q6	V_{CC}	V_{CC}	2D6	2D5
J	2Q7	2Q8	GND	GND	2D8	2D7
K	2 \overline{OE}	NC	NC	NC	NC	2CLK

(1) NC – No internal connection

**GRD OR ZRD PACKAGE
(TOP VIEW)**



**TERMINAL ASSIGNMENTS⁽¹⁾
(54-Ball GRD/ZRD Package)**

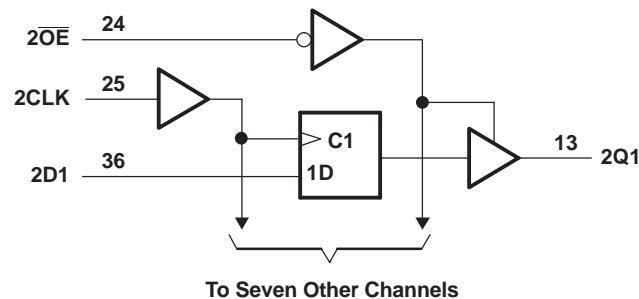
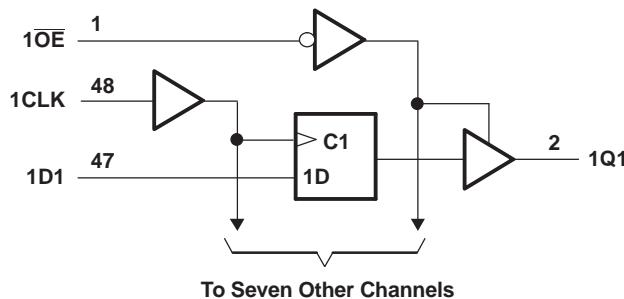
	1	2	3	4	5	6
A	1Q1	NC	1 \overline{OE}	1CLK	NC	1D1
B	1Q3	1Q2	NC	NC	1D2	1D3
C	1Q5	1Q4	V_{CC}	V_{CC}	1D4	1D5
D	1Q7	1Q6	GND	GND	1D6	1D7
E	2Q1	1Q8	GND	GND	1D8	2D1
F	2Q3	2Q2	GND	GND	2D2	2D3
G	2Q5	2Q4	V_{CC}	V_{CC}	2D4	2D5
H	2Q7	2Q6	NC	NC	2D6	2D7
J	2Q8	NC	2 \overline{OE}	2CLK	NC	2D8

(1) NC – No internal connection

**FUNCTION TABLE
(EACH FLIP-FLOP)**

INPUTS	OUTPUT			Q
	\overline{OE}	CLK	D	
L	↑	H		H
L	↑	L		L
L	H or L	X		Q_0
H	X	X		Z

LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the DGG, DL, and WD packages.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	4.6	V
V_I	Input voltage range ⁽²⁾	-0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	7	V
V_O	Voltage range applied to any output in the high state ⁽²⁾	-0.5	$V_{CC} + 0.5$	V
I_O	Current into any output in the low state	SN54LVTH16374	96	mA
		SN74LVTH16374	128	
I_O	Current into any output in the high state ⁽³⁾	SN54LVTH16374	48	mA
		SN74LVTH16374	64	
I_{IK}	Input clamp current	$V_I < 0$	-50	mA
I_{OK}	Output clamp current	$V_O < 0$	-50	mA
θ_{JA}	Package thermal impedance ⁽⁴⁾	DGG package	70	°C/W
		DL package	63	
		GQL/ZQL package	42	
		GRD/ZRD package	36	
T_{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(3) This current flows only when the output is in the high state and $V_O > V_{CC}$.

(4) The package thermal impedance is calculated in accordance with JEDEC 51-7.

Recommended Operating Conditions⁽¹⁾

		SN54LVTH16374		SN74LVTH16374		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage		5.5		5.5	V
I _{OH}	High-level output current		-24		-32	mA
I _{OL}	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate	200		200		μs/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54LVTH16374			SN74LVTH16374			UNIT
		MIN	TYP ⁽¹⁾	MAX	MIN	TYP ⁽¹⁾	MAX	
V_{IK}	$V_{CC} = 2.7 \text{ V}$, $I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$, $I_{OH} = -100 \mu\text{A}$	$V_{CC} - 0.2$			$V_{CC} - 0.2$			V
	$V_{CC} = 2.7 \text{ V}$, $I_{OH} = -8 \text{ mA}$	2.4			2.4			
	$V_{CC} = 3 \text{ V}$	$I_{OH} = -24 \text{ mA}$	2					
		$I_{OH} = -32 \text{ mA}$			2			
V_{OL}	$V_{CC} = 2.7 \text{ V}$	$I_{OL} = 100 \mu\text{A}$		0.2			0.2	V
		$I_{OL} = 24 \text{ mA}$		0.5			0.5	
	$V_{CC} = 3 \text{ V}$	$I_{OL} = 16 \text{ mA}$		0.4			0.4	
		$I_{OL} = 32 \text{ mA}$		0.5			0.5	
		$I_{OL} = 48 \text{ mA}$		0.55				
		$I_{OL} = 64 \text{ mA}$					0.55	
I_I	$V_{CC} = 0 \text{ or } 3.6 \text{ V}$, $V_I = 5.5 \text{ V}$			10			10	μA
	Control inputs	$V_{CC} = 3.6 \text{ V}$, $V_I = V_{CC} \text{ or GND}$		± 1			± 1	
		$V_{CC} = 3.6 \text{ V}$	$V_I = V_{CC}$	1			1	
I_{off}	Data inputs	$V_{CC} = 3.6 \text{ V}$	$V_I = 0$	-5			-5	μA
	$V_{CC} = 0$, $V_I \text{ or } V_O = 0 \text{ to } 4.5 \text{ V}$						± 100	
	Data inputs	$V_{CC} = 3 \text{ V}$	$V_I = 0.8 \text{ V}$	75			75	
			$V_I = 2 \text{ V}$	-75			-75	
		$V_{CC} = 3.6 \text{ V}$, ⁽²⁾	$V_I = 0 \text{ to } 3.6 \text{ V}$				500 -750	
I_{OZH}	$V_{CC} = 3.6 \text{ V}$, $V_O = 3 \text{ V}$			5			5	μA
	$V_{CC} = 3.6 \text{ V}$, $V_O = 0.5 \text{ V}$			-5			-5	μA
I_{OZL}	$V_{CC} = 0 \text{ to } 1.5 \text{ V}$, $V_O = 0.5 \text{ V to } 3 \text{ V}$, $\overline{OE} = \text{don't care}$			± 100 ⁽³⁾			± 100	μA
	$V_{CC} = 1.5 \text{ V to } 0$, $V_O = 0.5 \text{ V to } 3 \text{ V}$, $\overline{OE} = \text{don't care}$			± 100 ⁽³⁾			± 100	μA
I_{OZPU}	$V_{CC} = 3.6 \text{ V}$, $I_O = 0$, $V_I = V_{CC} \text{ or GND}$	Outputs high		0.19			0.19	mA
		Outputs low		5			5	
		Outputs disabled		0.19			0.19	
ΔI_{CC} ⁽⁴⁾	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, One input at $V_{CC} - 0.6 \text{ V}$, Other inputs at V_{CC} or GND			0.2			0.2	mA
C_I	$V_I = 3 \text{ V or } 0$			3			3	pF
C_O	$V_O = 3 \text{ V or } 0$			9			9	pF

(1) All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

(3) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

			SN54LVTH16374		SN74LVTH16374		UNIT	
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V			
			MIN	MAX	MIN	MAX		
f _{clock}	Clock frequency		160		160		160	MHz
t _w	Pulse duration, CLK high or low		3		3		3	ns
t _{su}	Setup time, data before CLK↑	High or low	2.9		3.3		1.8	2
t _h	Hold time, data after CLK↑	High or low	0.8		0.2		0.8	0.1
								ns

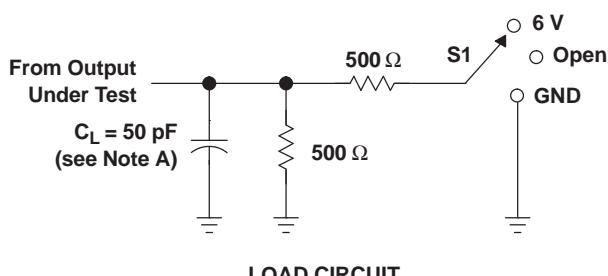
Switching Characteristics

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see [Figure 1](#))

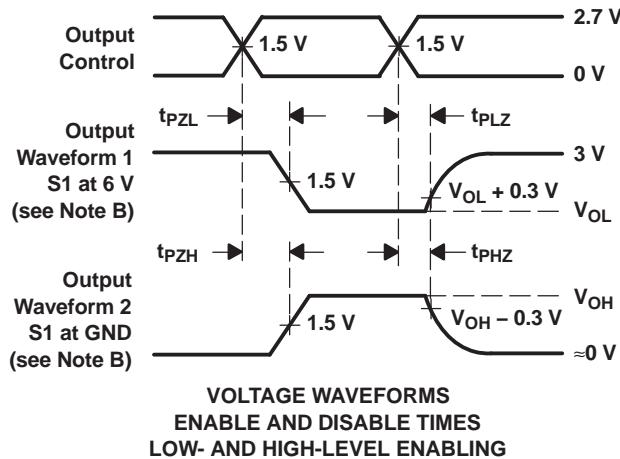
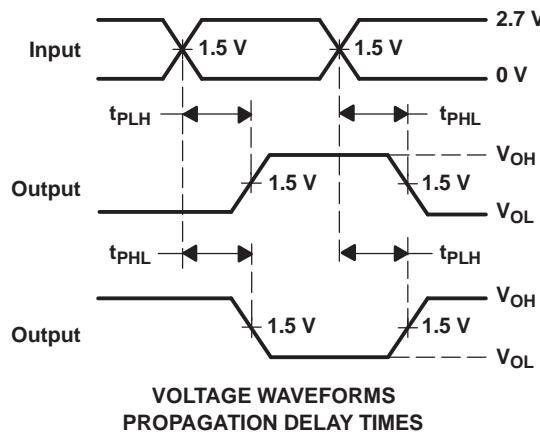
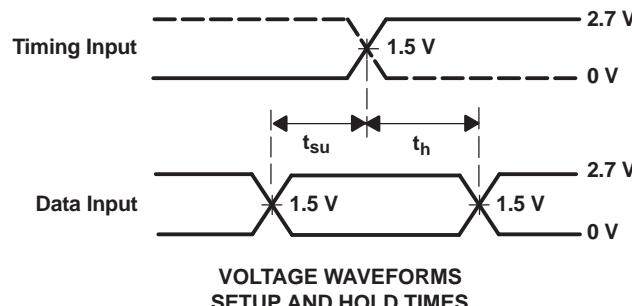
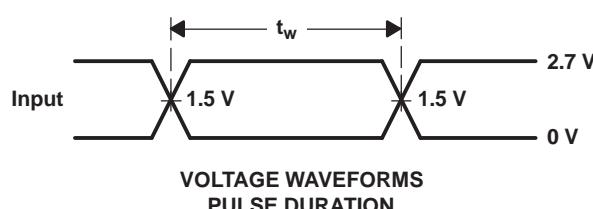
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH16374		SN74LVTH16374		UNIT	
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V			
			MIN	MAX	MIN	MAX		
f _{max}			160		160		160	MHz
t _{PLH}	CLK	Q	1.4	5.6	6.2	1.9	3	4.5
t _{PHL}			1.7	4.8	5	2.1	2.9	4
t _{PZH}	OE	Q	1	5.6	6.4	1.5	2.8	4.5
t _{PZL}			1.4	5.5	6.2	1.5	2.8	4.4
t _{PHZ}	OE	Q	1	6.4	6.9	2.4	3.5	5
t _{PLZ}			1.7	5	5.2	2	3.2	4.6
t _{sk(LH)}							0.5	ns
t _{sk(HL)}							0.5	

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9564701QXA	ACTIVE	CFP	WD	48	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9564701QXA SNJ54LVTH16374 WD	Samples
74LVTH16374DLRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16374	Samples
SN74LVTH16374DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16374	Samples
SN74LVTH16374DL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16374	Samples
SN74LVTH16374DLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16374	Samples
SN74LVTH16374DLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16374	Samples
SN74LVTH16374GQLR	OBsolete	BGA MICROSTAR JUNIOR	GQL	56		TBD	Call TI	Call TI	-40 to 85		
SN74LVTH16374GRDR	OBsolete	BGA MICROSTAR JUNIOR	GRD	54		TBD	Call TI	Call TI	-40 to 85	LL374	
SNJ54LVTH16374WD	ACTIVE	CFP	WD	48	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9564701QXA SNJ54LVTH16374 WD	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

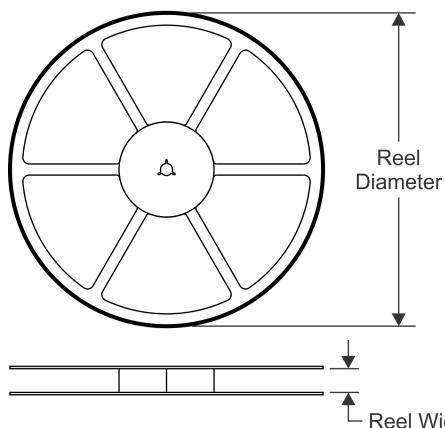
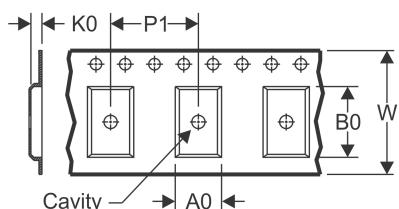
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54LVTH16374, SN74LVTH16374 :

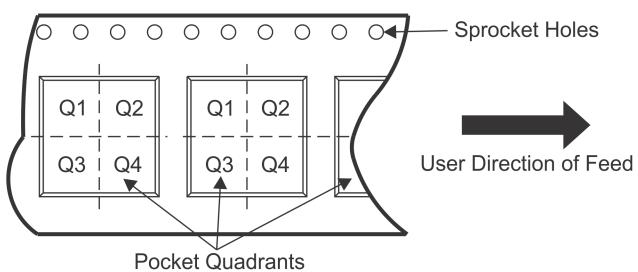
- Catalog: [SN74LVTH16374](#)
- Enhanced Product: [SN74LVTH16374-EP](#), [SN74LVTH16374-EP](#)
- Military: [SN54LVTH16374](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

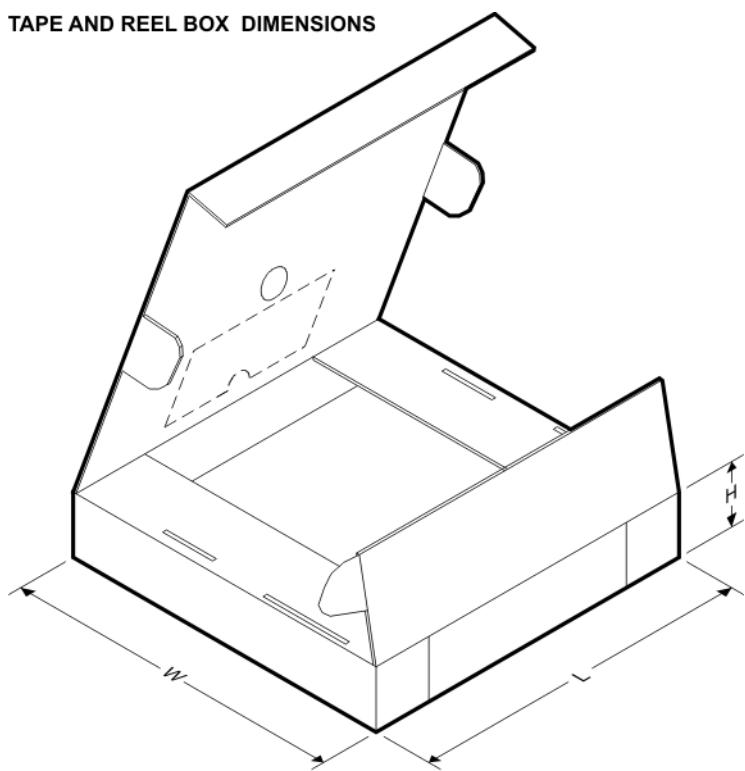
TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVTH16374DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
SN74LVTH16374DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS


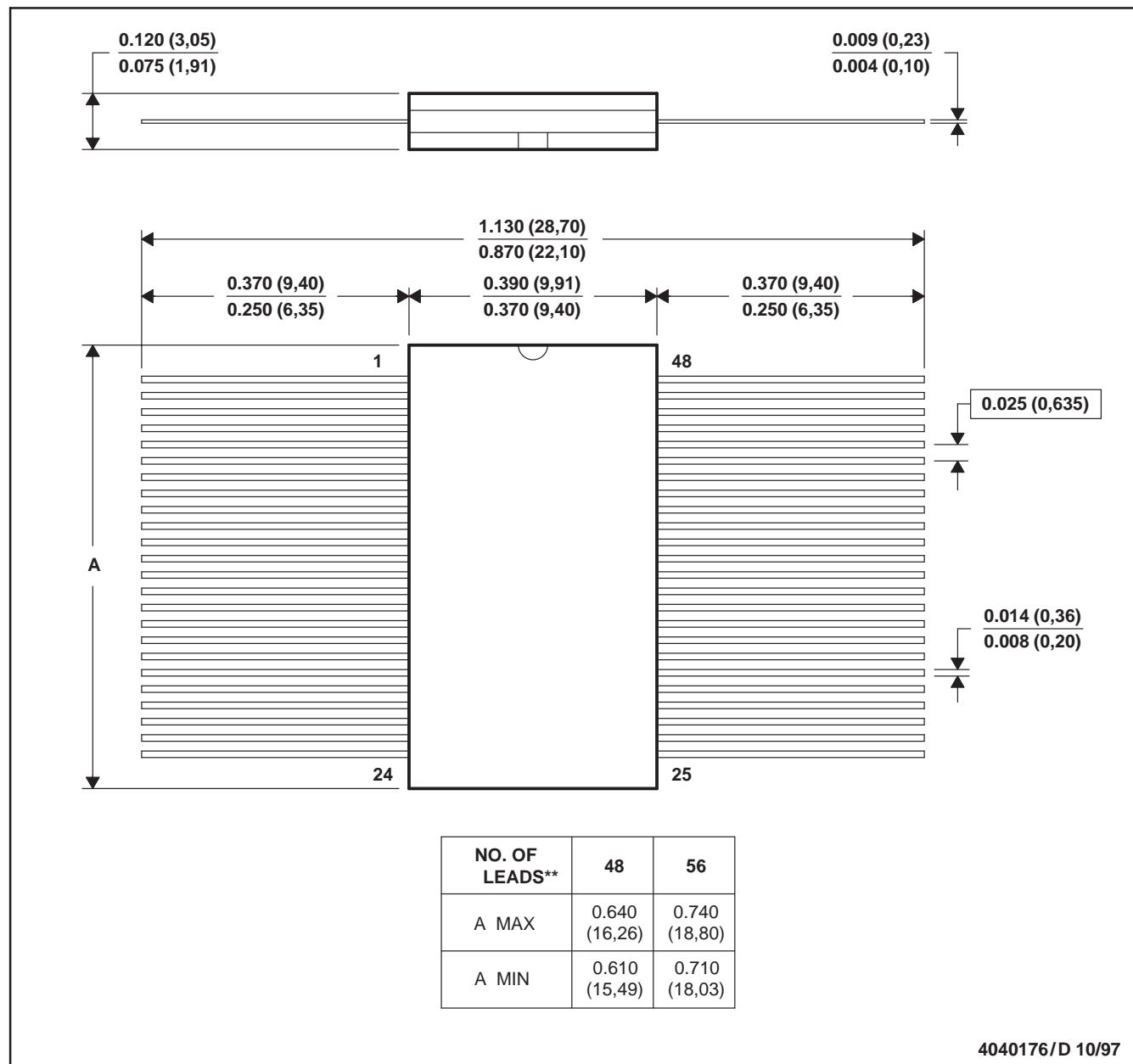
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVTH16374DGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74LVTH16374DLR	SSOP	DL	48	1000	367.0	367.0	55.0

WD (R-GDFP-F**)

CERAMIC DUAL FLATPACK

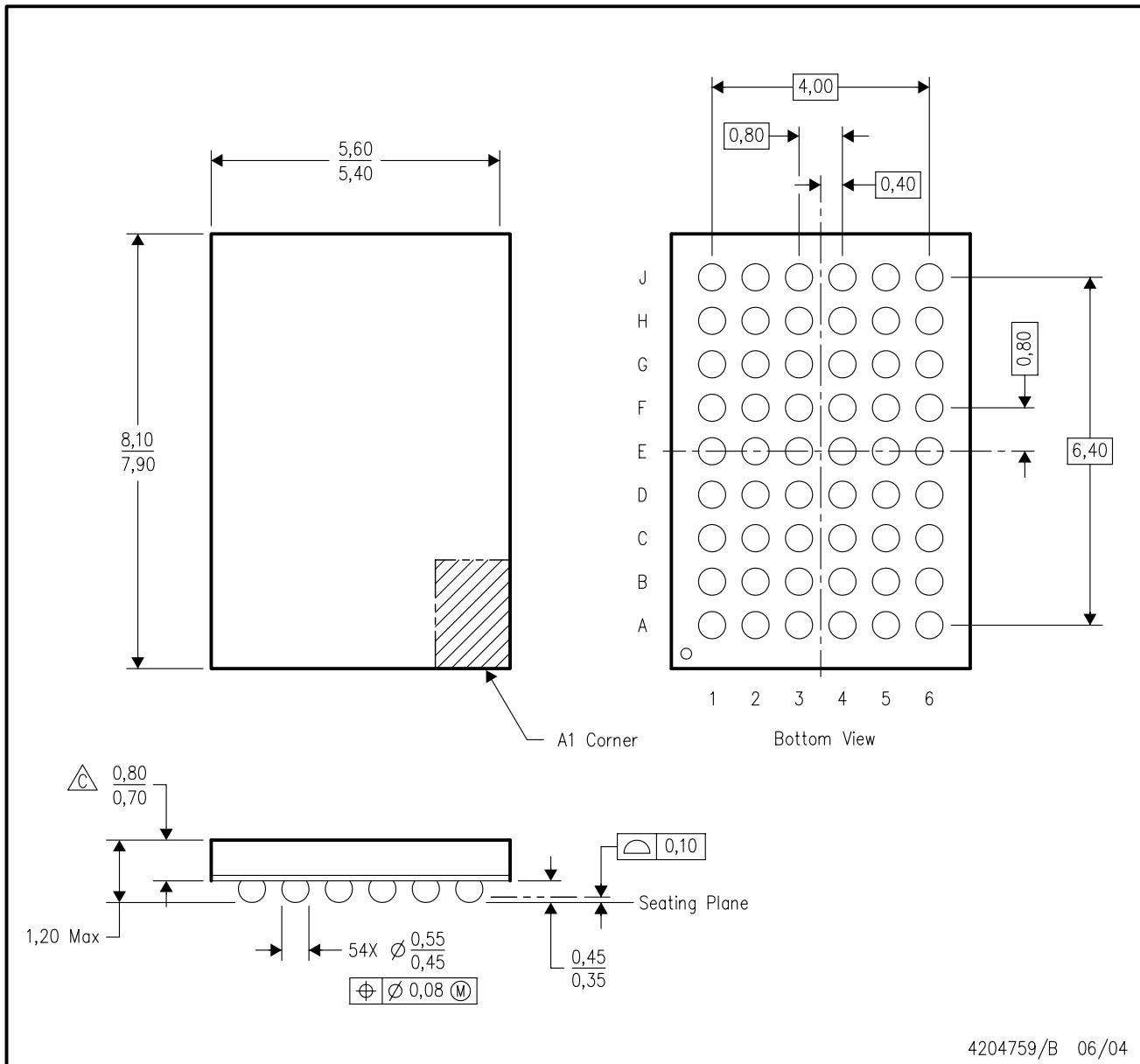
48 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only.
 E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA
 GDFP1-F56 and JEDEC MO-146AB

GRD (R-PBGA-N54)

PLASTIC BALL GRID ARRAY



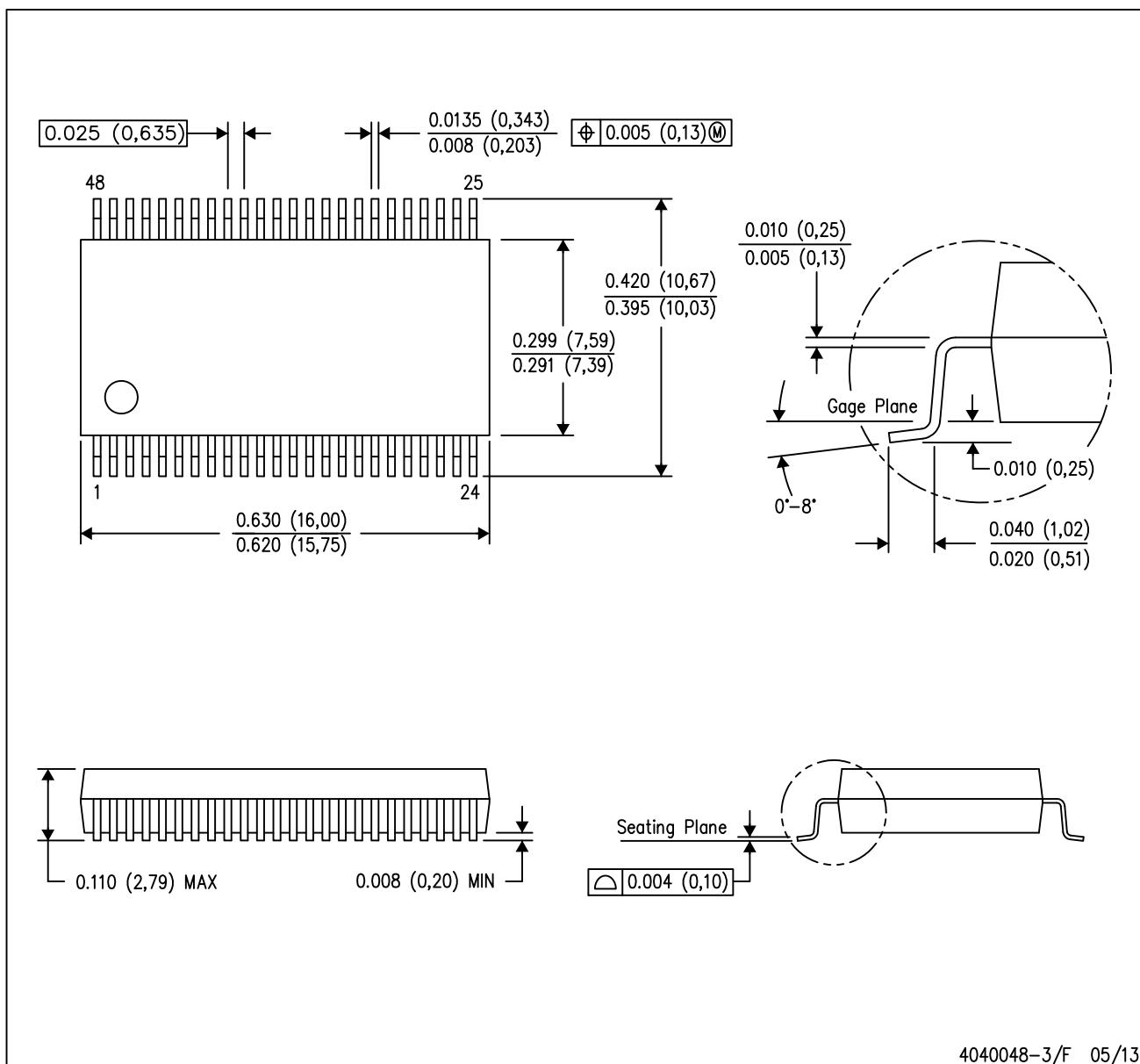
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

Falls within JEDEC MO-205 variation DD.

D. This package is tin-lead (SnPb). Refer to the 54 ZRD package (drawing 4204760) for lead-free.

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE

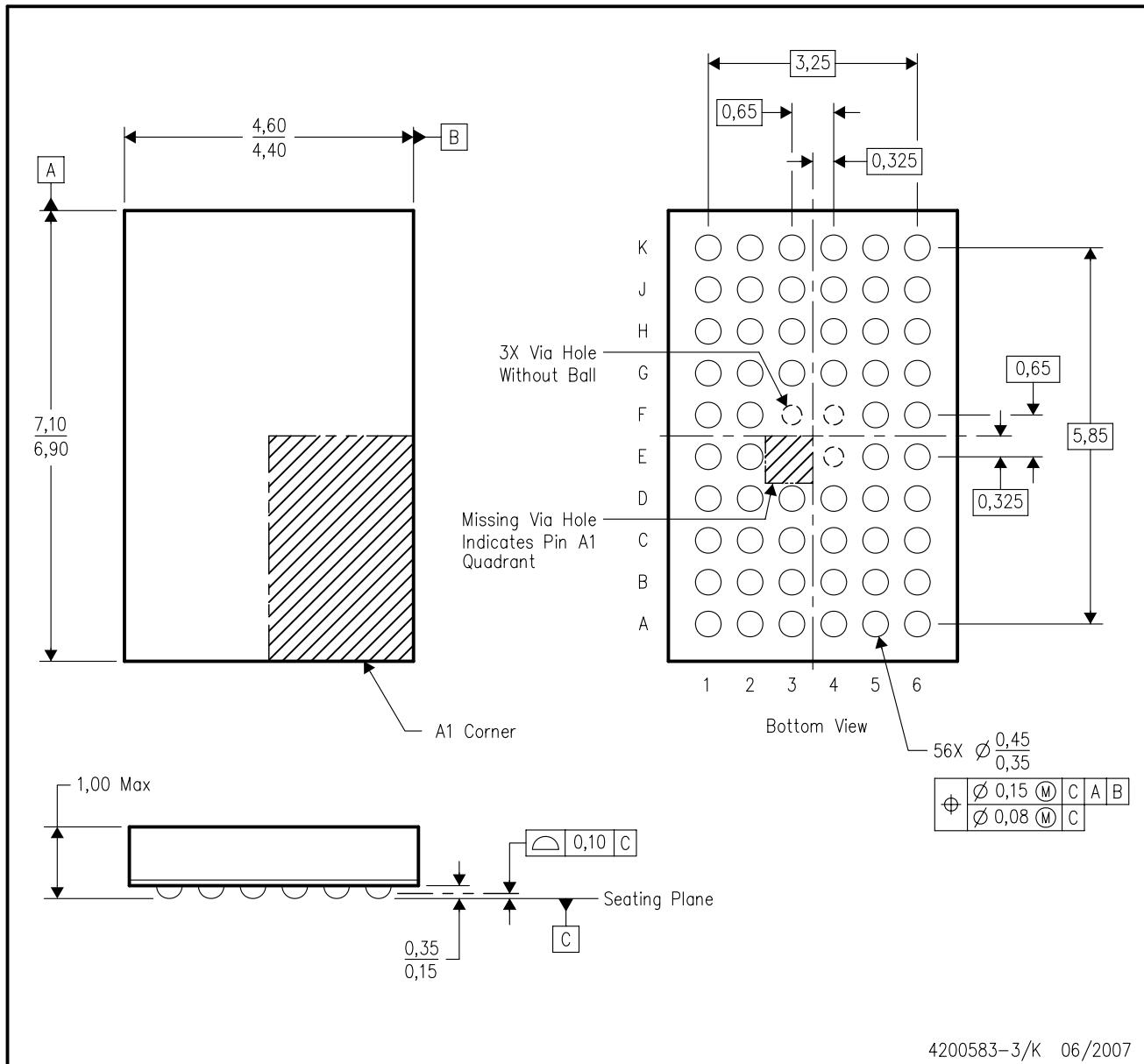


- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MO-118

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GQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



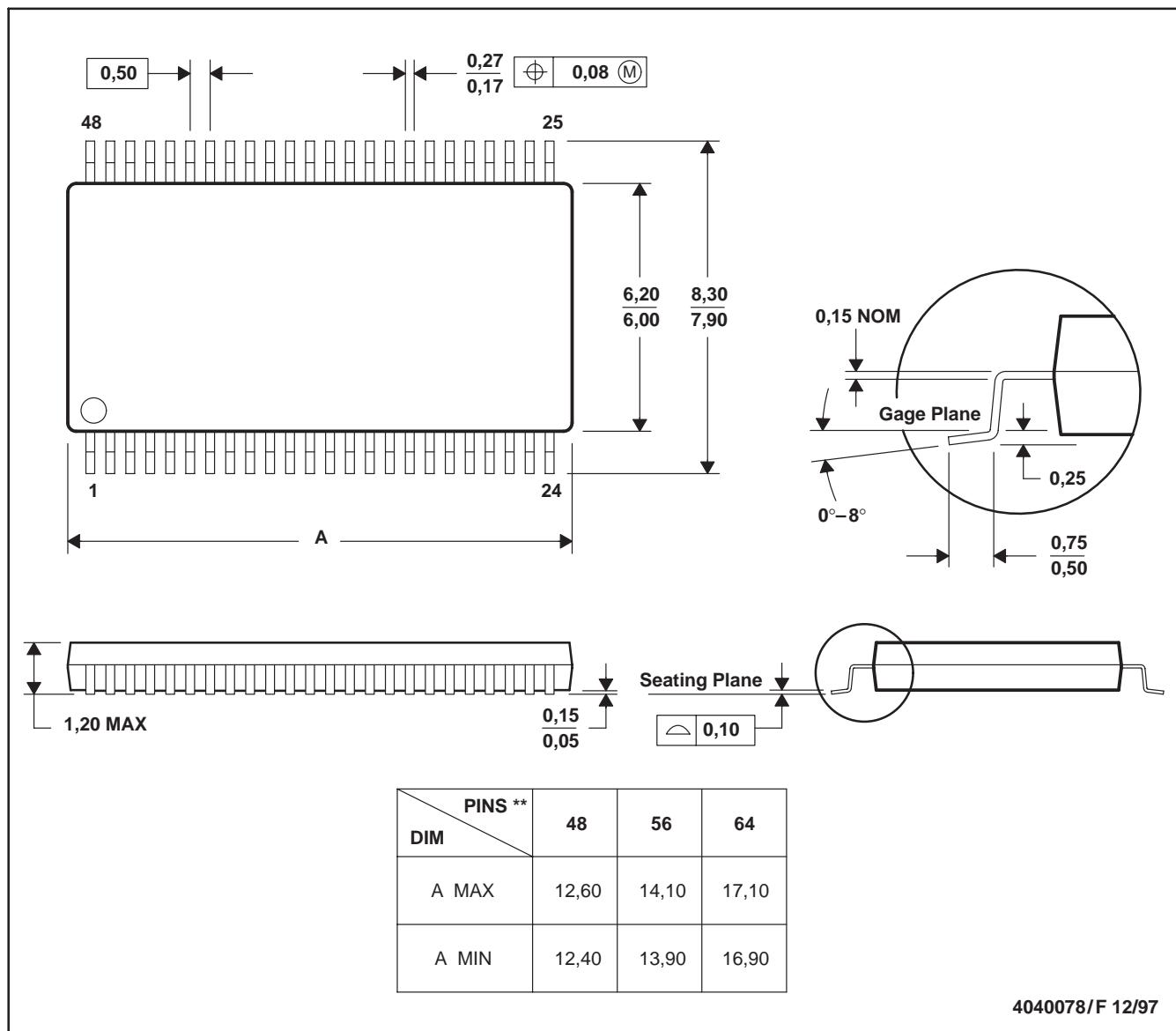
4200583-3/K 06/2007

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Falls within JEDEC MO-285 variation BA-2.
 - This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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