

N-Channel 20-V (D-S) MOSFET with Trench Schottky Diode

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ.)
20	0.053 at $V_{GS} = 4.5$ V	4.5	4.1 nC
	0.063 at $V_{GS} = 2.5$ V	4.5	
	0.077 at $V_{GS} = 1.8$ V	4.5	

SCHOTTKY PRODUCT SUMMARY		
V_{KA} (V)	V_f (V) Diode Forward Voltage	I_F (A) ^a
20	0.45 at 1 A	2

FEATURES

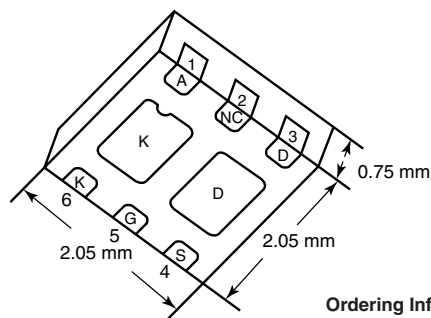
- Halogen-free
- LITTLE FOOT® Plus Schottky Power MOSFET
- New Thermally Enhanced PowerPAK® SC-70 Package
 - Small Footprint Area
 - Low On-Resistance
 - Thin 0.75 mm profile
- Low V_f Trench Schottky Diode


RoHS
COMPLIANT

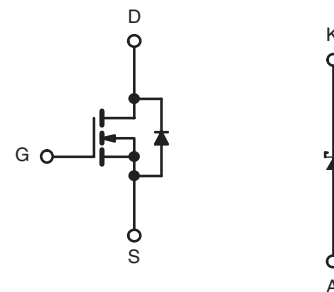
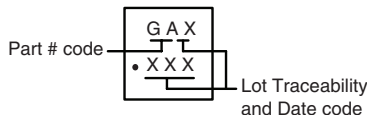
APPLICATIONS

- Load Switch for Portable Devices (MP3/Cellular)
- Boost Converter

PowerPAK SC-70-6 Dual



Marking Code



Ordering Information: SiA810DJ-T1-GE3 (Lead (Pb)-free and Halogen-free)

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage (MOSFET)	V_{DS}	20	V	
Reverse Voltage (Schottky)	V_{KA}	20		
Gate-Source Voltage (MOSFET)	V_{GS}	± 8		
Continuous Drain Current ($T_J = 150$ °C) (MOSFET)	I_D	$T_C = 25$ °C	4.5 ^a	A
		$T_C = 70$ °C	4.5 ^a	
		$T_A = 25$ °C	4.5 ^{a, b, c}	
		$T_A = 70$ °C	3.8 ^{b, c}	
Pulsed Drain Current (MOSFET)	I_{DM}	20		
Continuous Source-Drain Diode Current (MOSFET Diode Conduction)	I_S	$T_C = 25$ °C	4.5 ^a	
		$T_A = 25$ °C	1.6 ^{b, c}	
Average Forward Current (Schottky)	I_F	2 ^b		
Pulsed Forward Current (Schottky)	I_{FM}	5		
Maximum Power Dissipation (MOSFET)	P_D	$T_C = 25$ °C	6.5	W
		$T_C = 70$ °C	5	
		$T_A = 25$ °C	1.9 ^{b, c}	
		$T_A = 70$ °C	1.2 ^{b, c}	
Maximum Power Dissipation (Schottky)	P_D	$T_C = 25$ °C	6.8	
		$T_C = 70$ °C	4.3	
		$T_A = 25$ °C	1.6 ^{b, c}	
		$T_A = 70$ °C	1.0 ^{b, c}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260		

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient (MOSFET) ^{b, f}	$t \leq 5$ s	R_{thJA}	52	65	°C/W
Maximum Junction-to-Case (Drain) (MOSFET)	Steady State	R_{thJC}	12.5	16	
Maximum Junction-to-Ambient (Schottky) ^{b, g}	$t \leq 5$ s	R_{thJA}	62	76	
Maximum Junction-to-Case (Drain) (Schottky)	Steady State	R_{thJC}	15	18.5	

Notes:

a. Package limited.

b. Surface Mounted on 1" x 1" FR4 board.

c. $t = 5$ s.d. See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under Steady State conditions is 110 °C/W.

g. Maximum under Steady State conditions is 110 °C/W.

SPECIFICATIONS $T_J = 25$ °C, unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0$ V, $I_D = 250$ μ A	20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250$ μ A		1		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 2.8		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250$ μ A	0.4		1	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 8$ V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20$ V, $V_{GS} = 0$ V			1	μ A
		$V_{DS} = 20$ V, $V_{GS} = 0$ V, $T_J = 55$ °C			10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq 5$ V, $V_{GS} = 4.5$ V	20			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 4.5$ V, $I_D = 3.7$ A		0.043	0.053	Ω
		$V_{GS} = 2.5$ V, $I_D = 3.4$ A		0.052	0.063	
		$V_{GS} = 1.8$ V, $I_D = 1.1$ A		0.062	0.077	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10$ V, $I_D = 3.7$ A		15		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 10$ V, $V_{GS} = 0$ V, $f = 1$ MHz		400		pF
Output Capacitance	C_{oss}			70		
Reverse Transfer Capacitance	C_{rss}			40		
Total Gate Charge	Q_g	$V_{DS} = 10$ V, $V_{GS} = 8$ V, $I_D = 4.8$ A		7	11.5	nC
Gate-Source Charge	Q_{gs}	$V_{DS} = 10$ V, $V_{GS} = 4.5$ V, $I_D = 4.8$ A		4.1	7	
Gate-Drain Charge	Q_{gd}			0.65		
Gate Resistance	R_g			0.8		
Turn-On Delay Time	$t_{d(on)}$	$f = 1$ MHz $V_{DD} = 10$ V, $R_L = 2.6$ Ω $I_D \cong 3.8$ A, $V_{GEN} = 4.5$ V, $R_g = 1$ Ω		2.5		Ω
Rise Time	t_r			5	10	
Turn-Off Delay Time	$t_{d(off)}$			32	50	
Fall Time	t_f			30	45	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10$ V, $R_L = 2.6$ Ω $I_D \cong 3.8$ A, $V_{GEN} = 8$ V, $R_g = 1$ Ω		53	80	
Rise Time	t_r			5	10	
Turn-Off Delay Time	$t_{d(off)}$			12	20	
Fall Time	t_f			15	25	
				10	15	



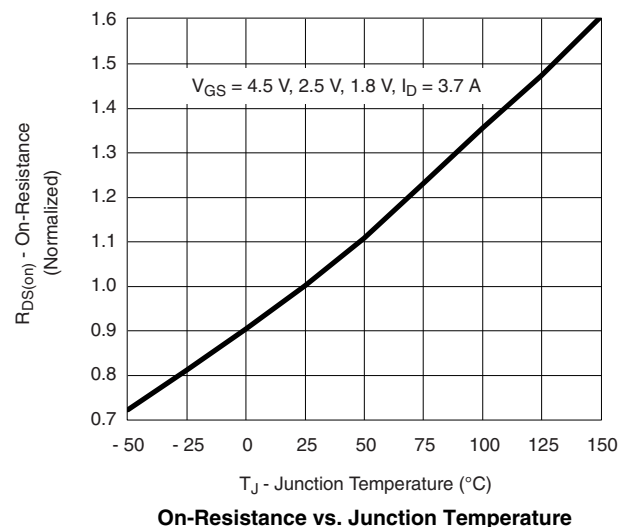
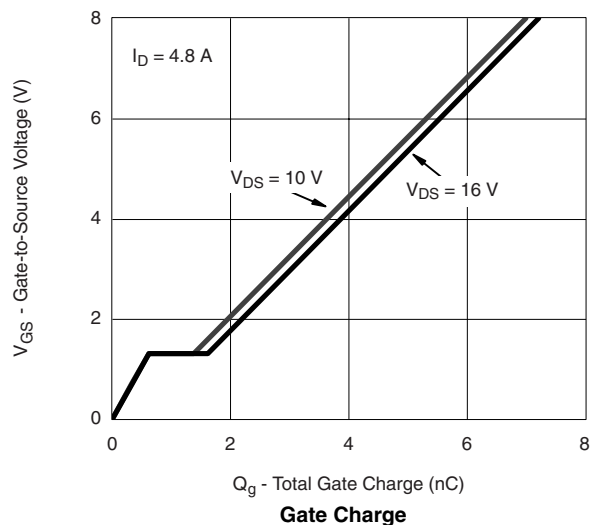
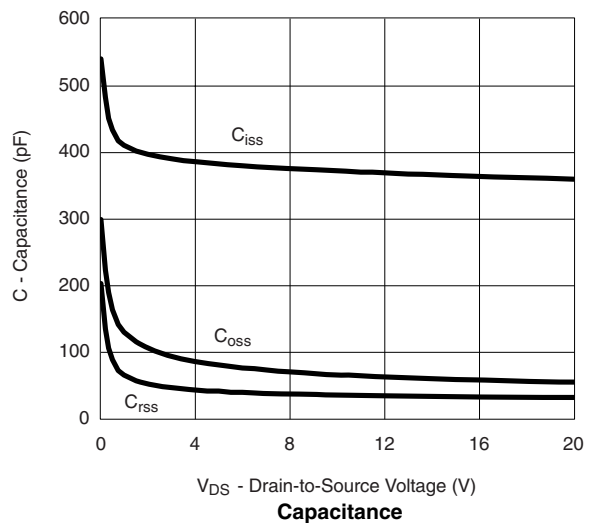
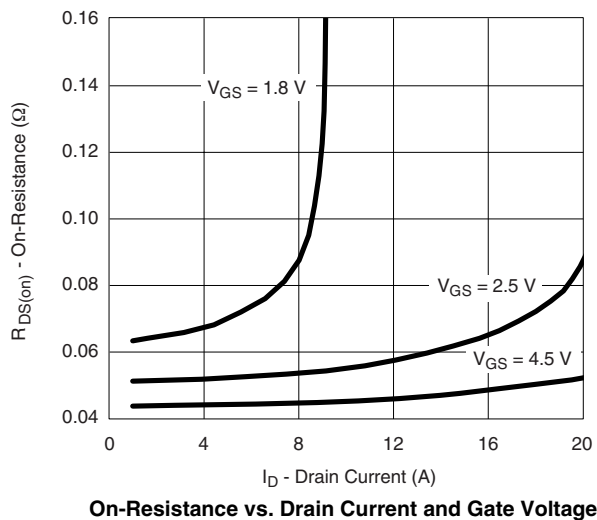
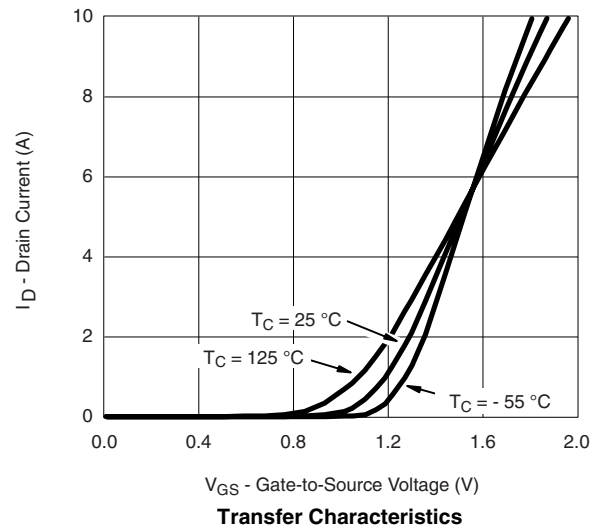
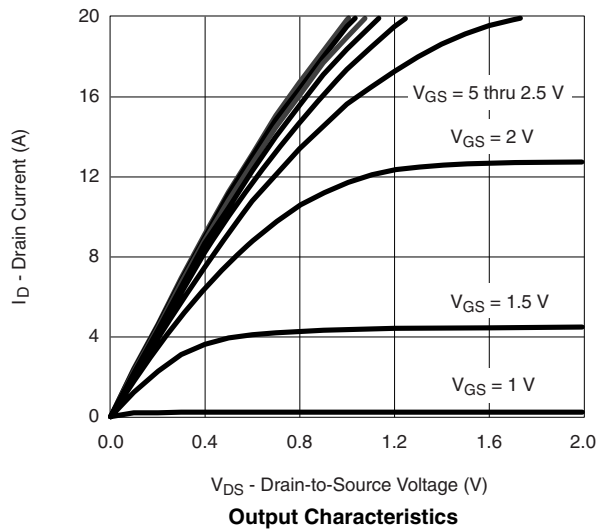
SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^{\circ}\text{C}$			4.5	A
Pulse Diode Forward Current	I_{SM}				20	
Body Diode Voltage	V_{SD}	$I_S = 3.8\text{ A}$, $V_{GS} = 0\text{ V}$		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 3.8\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^{\circ}\text{C}$		15	30	ns
Body Diode Reverse Recovery Charge	Q_{rr}			8.5	20	nC
Reverse Recovery Fall Time	t_a			10		ns
Reverse Recovery Rise Time	t_b			5		

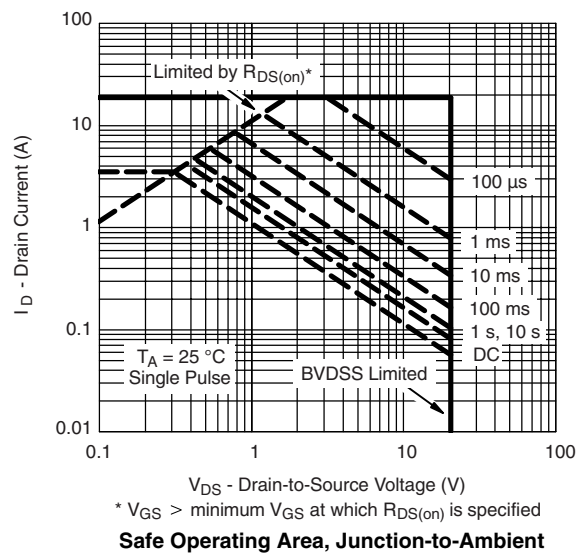
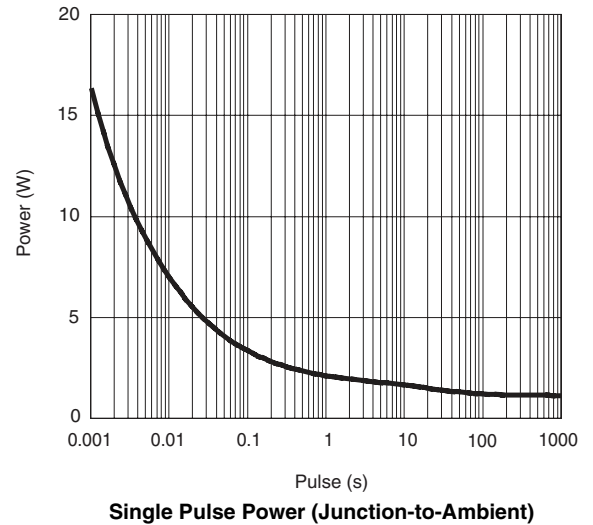
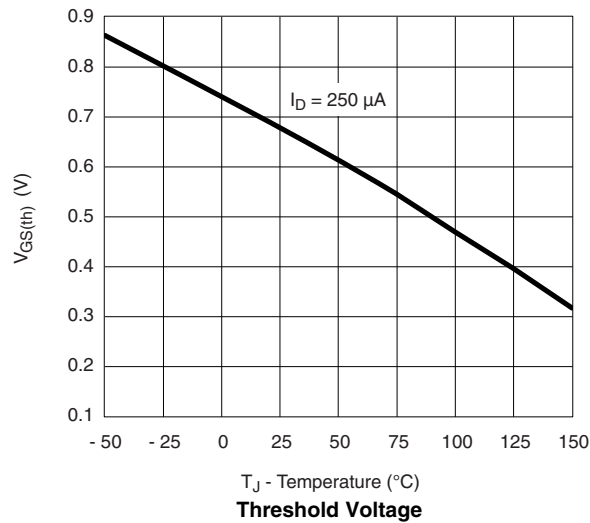
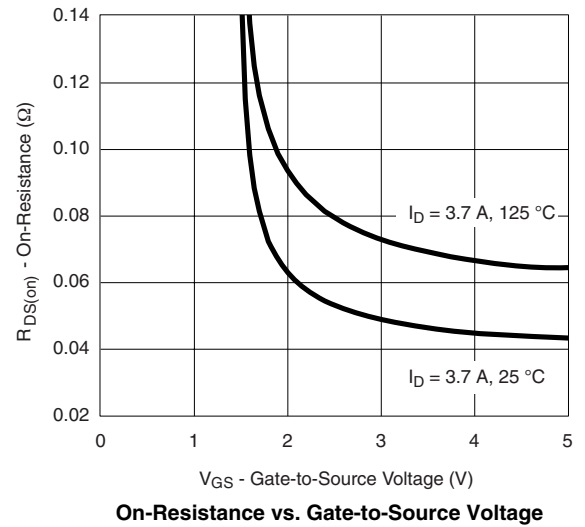
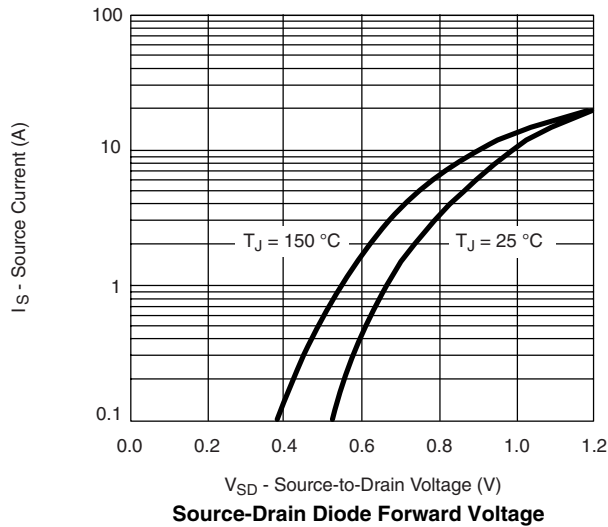
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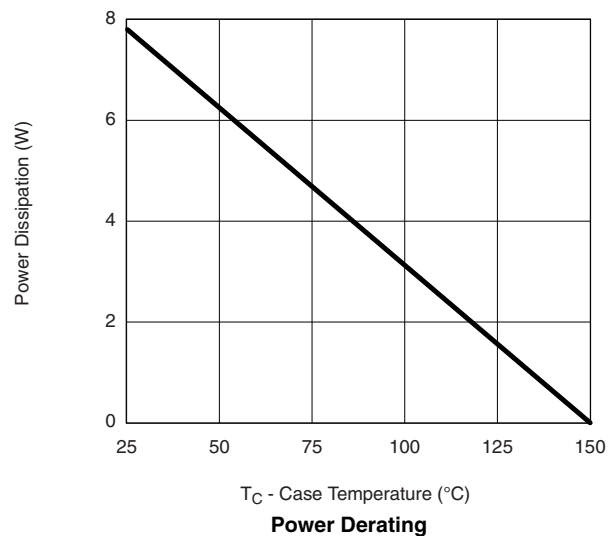
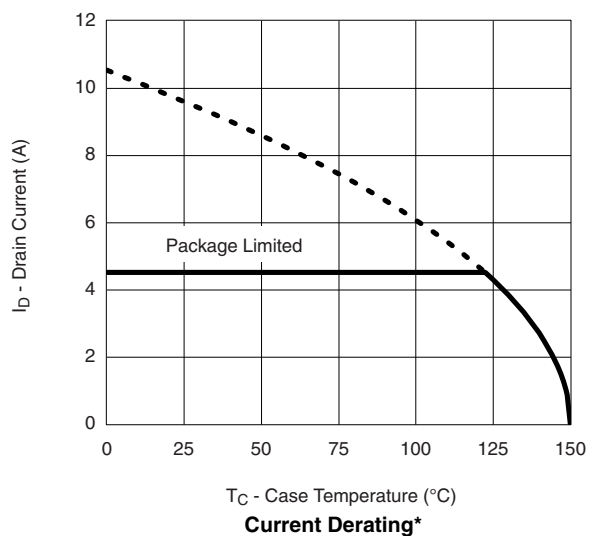
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

SCHOTTKY SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Forward Voltage Drop	V_F	$I_F = 1\text{ A}$		0.41	0.45	V
		$I_F = 1\text{ A}$, $T_J = 125\text{ }^{\circ}\text{C}$		0.36	0.41	
Maximum Reverse Leakage Current	I_{rm}	$V_r = 5\text{ V}$		0.015	0.08	mA
		$V_r = 5\text{ V}$, $T_J = 85\text{ }^{\circ}\text{C}$		0.50	5.00	
		$V_r = 20\text{ V}$		0.02	0.10	
		$V_r = 20\text{ V}$, $T_J = 85\text{ }^{\circ}\text{C}$		0.7	7	
		$V_r = 20\text{ V}$, $T_J = 125\text{ }^{\circ}\text{C}$		5	50	
Junction Capacitance	C_T	$V_r = 10\text{ V}$		60		pF

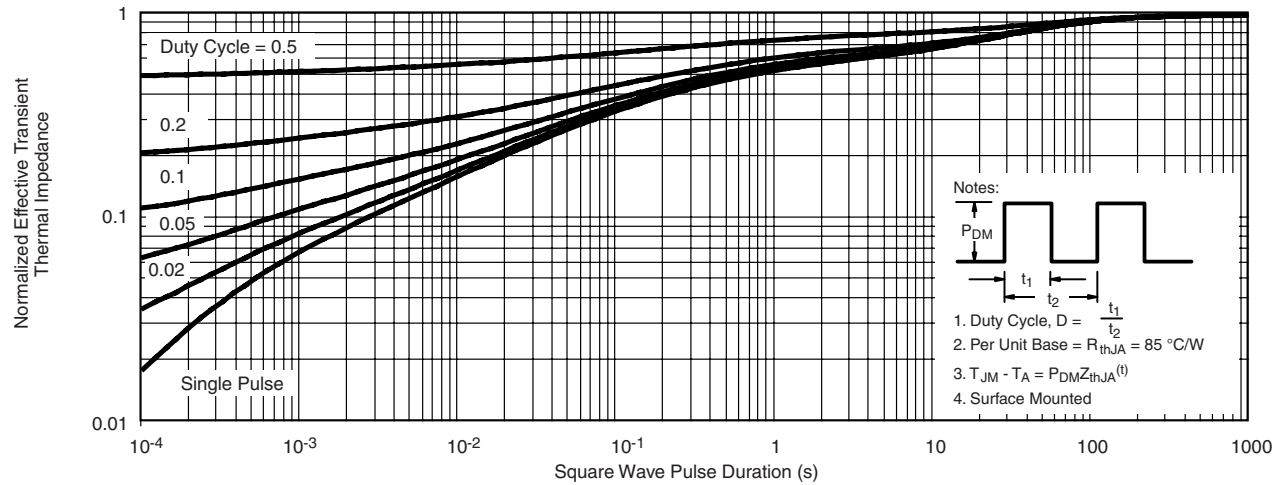
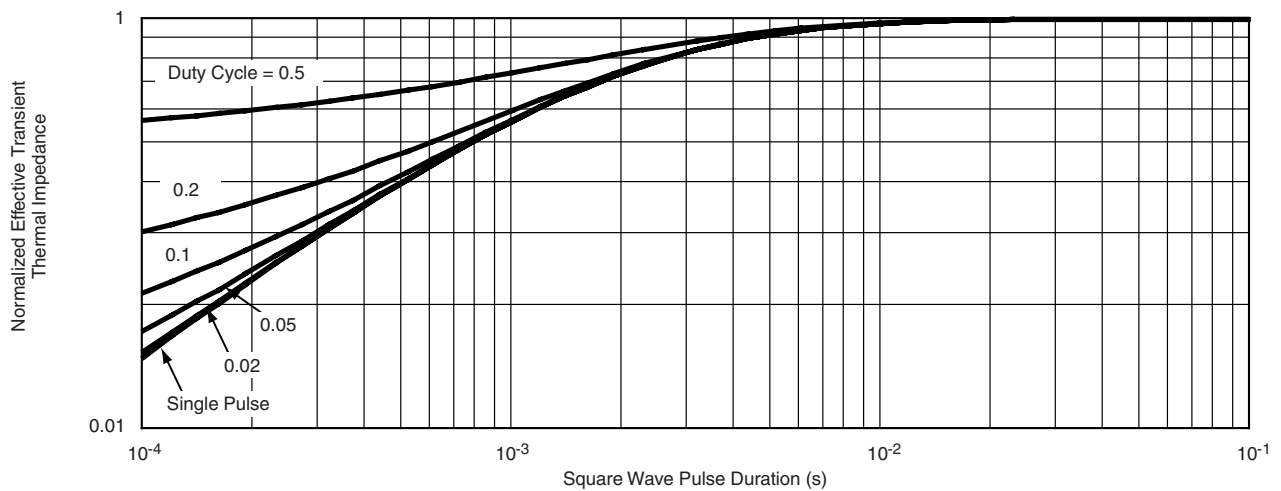
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

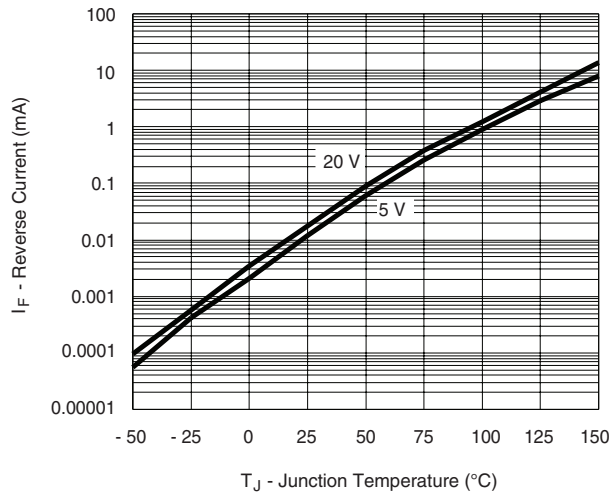
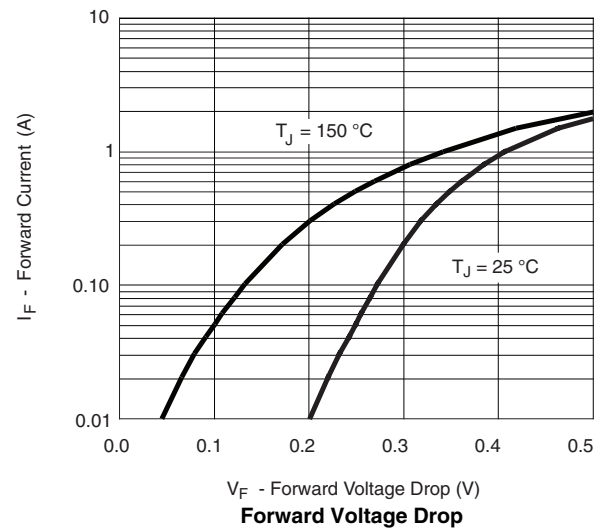
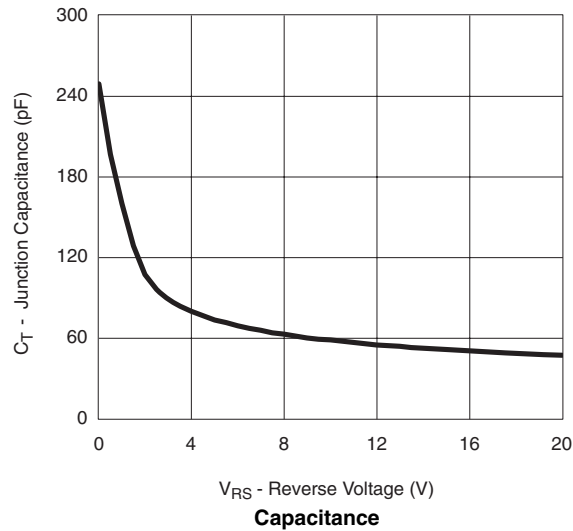
MOSFET TYPICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, unless otherwise noted


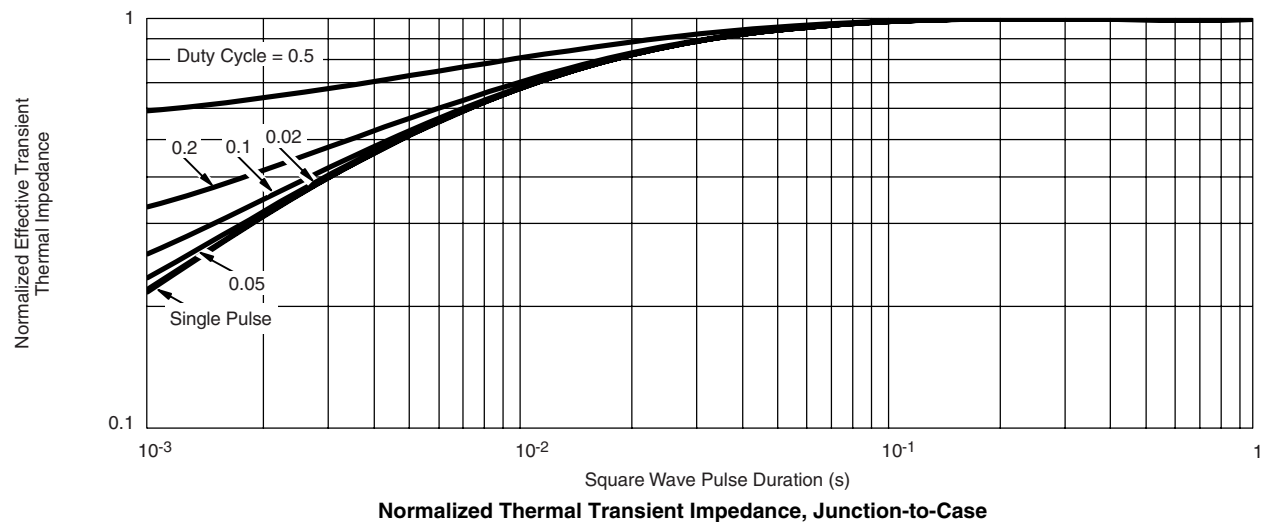
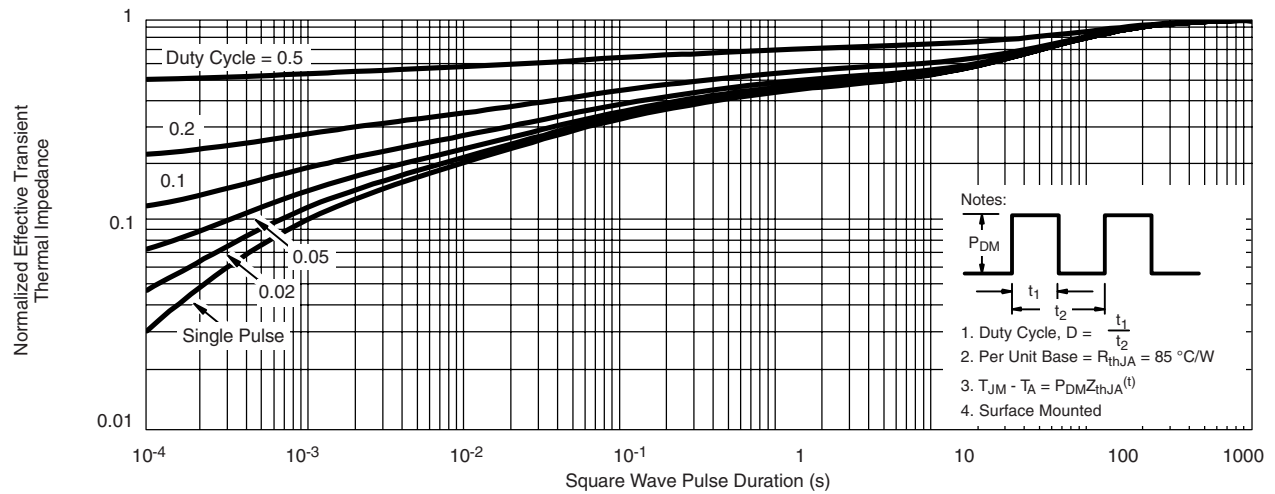
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* The power dissipation P_D is based on $T_{J(max)} = 150\text{ }^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**MOSFET TYPICAL CHARACTERISTICS** $T_A = 25^\circ\text{C}$, unless otherwise noted**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Case**

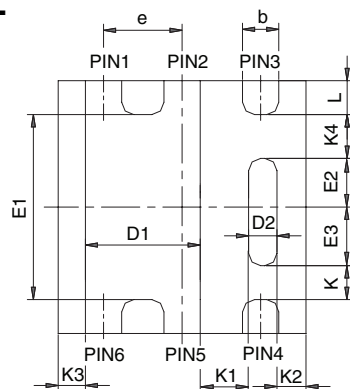
SCHOTTKY TYPICAL CHARACTERISTICS $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

Reverse Current vs. Junction Temperature

Forward Voltage Drop

Capacitance

**SCHOTTKY TYPICAL CHARACTERISTICS** $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

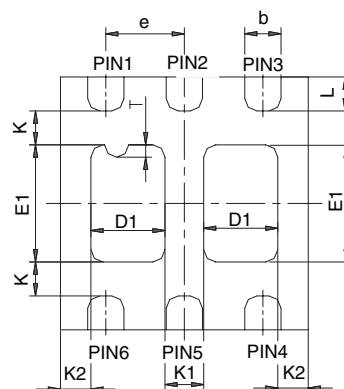
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?74957>.



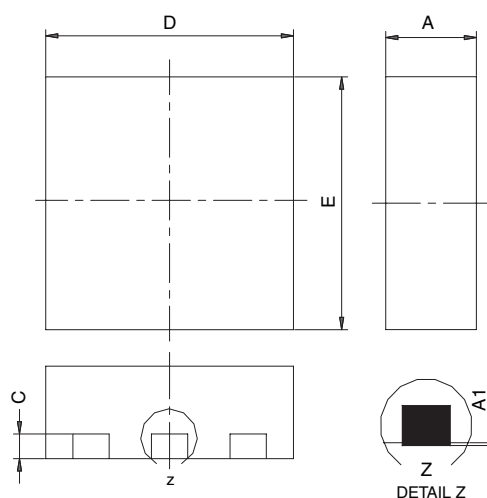
PowerPAK® SC70-6L



BACKSIDE VIEW OF SINGLE



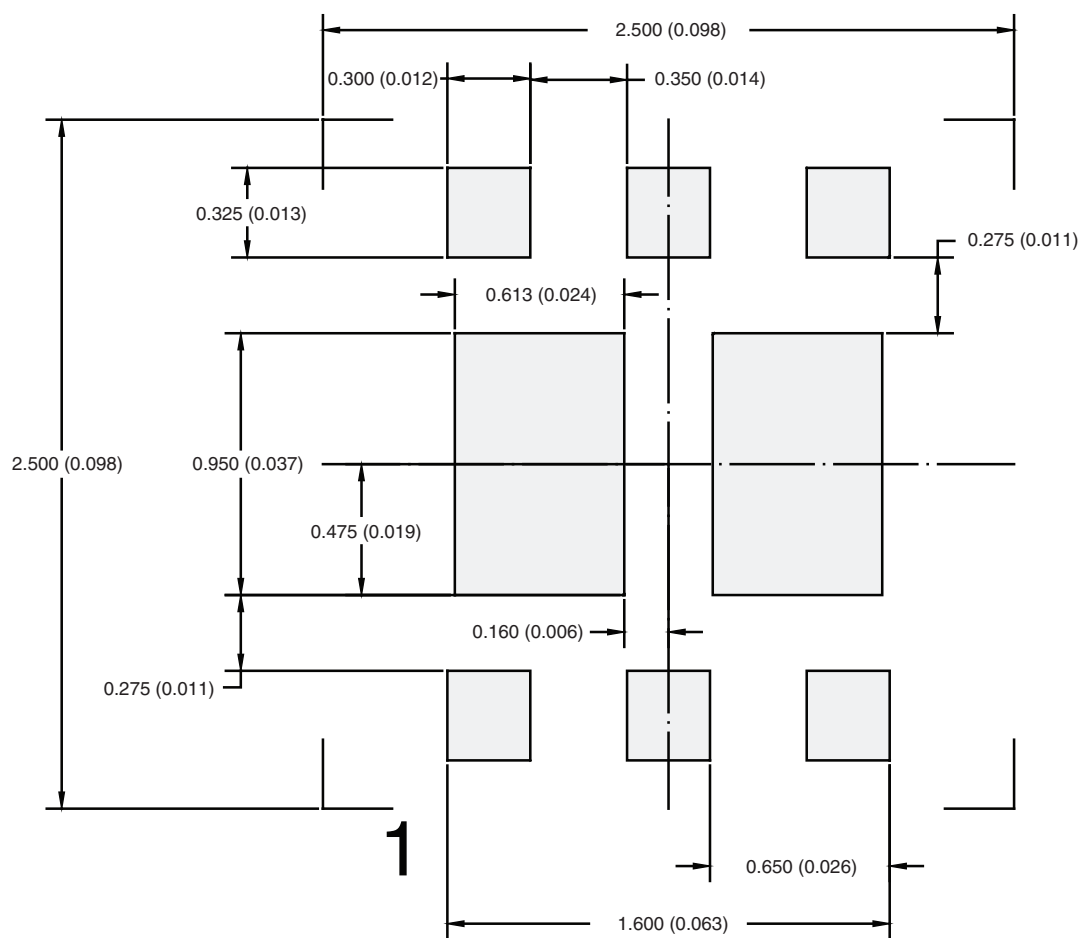
BACKSIDE VIEW OF DUAL



- Notes:
1. All dimensions are in millimeters
 2. Package outline exclusive of mold flash and metal burr
 3. Package outline inclusive of plating

DIM	SINGLE PAD						DUAL PAD					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015
C	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028
D2	0.135	0.235	0.335	0.005	0.009	0.013						
E	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041
E2	0.345	0.395	0.445	0.014	0.016	0.018						
E3	0.425	0.475	0.525	0.017	0.019	0.021						
e	0.65 BSC			0.026 BSC			0.65 BSC			0.026 BSC		
K	0.275 TYP			0.011 TYP			0.275 TYP			0.011 TYP		
K1	0.400 TYP			0.016 TYP			0.320 TYP			0.013 TYP		
K2	0.240 TYP			0.009 TYP			0.252 TYP			0.010 TYP		
K3	0.225 TYP			0.009 TYP								
K4	0.355 TYP			0.014 TYP								
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015
T							0.05	0.10	0.15	0.002	0.004	0.006
ECN: C-07431 – Rev. C, 06-Aug-07												
DWG: 5934												

RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Dual



Dimensions in mm (inches)



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Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

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