



Precision CMOS Analog Switches

FEATURES

- $\pm 15\text{-V}$ Analog Signal Range
- On-Resistance— $r_{DS(on)}$: $15\ \Omega$
- Fast Switching Action— t_{ON} : 100 ns
- TTL and CMOS Compatible
- MSOP-8 and SOIC-8 Packaging

BENEFITS

- Wide Dynamic Range
- Low Signal Errors and Distortion
- Break-Before-Make Switching Action
- Simple Interfacing
- Reduced Board Space
- Improved Reliability

APPLICATIONS

- Precision Test Equipment
- Precision Instrumentation
- Battery Powered Systems
- Sample-and-Hold Circuits
- Military Radios
- Guidance and Control Systems
- Hard Disk Drives

DESCRIPTION

The DG417B/418B/419B monolithic CMOS analog switches were designed to provide high performance switching of analog signals. Combining low power, low leakages, high speed, low on-resistance and small physical size, the DG417B series is ideally suited for portable and battery powered industrial and military applications requiring high performance and efficient use of board space.

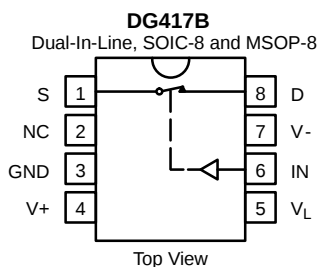
high voltage silicon gate (HVSG) process. Break-before-make is guaranteed for the DG419B, which is an SPDT configuration. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

To achieve high-voltage ratings and superior switching performance, the DG417B series is built on Vishay Siliconix's

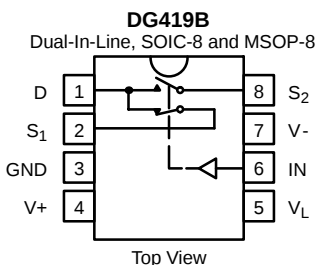
The DG417B and DG418B respond to opposite control logic levels as shown in the Truth Table.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE		
Logic	DG417B	DG418B
0	ON	OFF
1	OFF	ON

Logic "0" = $\leq 0.8\text{ V}$, Logic "1" = $\geq 2.4\text{ V}$



TRUTH TABLE—DG419B		
Logic	SW ₁	SW ₂
0	ON	OFF
1	OFF	ON

Logic "0" = $\leq 0.8\text{ V}$, Logic "1" = $\geq 2.4\text{ V}$

ORDERING INFORMATION		
Temp Range	Package	Part Number
DG417B/418B		
- 40 to 85°C	8-Pin Plastic MiniDIP	DG417BDJ
		DG418BDJ
	8-Pin Narrow SOIC	DG417BDY
		DG418BDY
	8-Pin MSOP	DG417BDQ
		DG418BDQ
- 55 to 125°C	8-Pin CerDIP	DG417BAK, DG417BAK/883
		DG418BAK, DG418BAK/883
DG419B		
- 40 to 85°C	8-Pin Plastic MiniDIP	DG419BDJ
	8-Pin Narrow SOIC	DG419BDY
	8-Pin MSOP	DG419BDQ
- 55 to 125°C	8-Pin CerDIP	DG419BAK, DG419BAK/883

NOTE: SMD product is dual marked with /883 number.

ABSOLUTE MAXIMUM RATINGS

V-	-20 V
V+	20 V
GND	25 V
V _L	(GND -0.3 V) to (V+) + 0.3 V
Digital Inputs ^a V _S , V _D	(V-) -2 V to (V+) + 2 V or 30 mA, whichever occurs first
Current, (Any Terminal) Continuous	30 mA
Current (S or D) Pulsed 1 ms, 10% duty cycle	100 mA
Storage Temperature	-65 to 150 °C
Power Dissipation (Package) ^b	

8-Pin Plastic MiniDIP ^c	400 mW
8-Pin Narrow SOIC ^c	400 mW
8-Pin MSOP ^d	400 mW
8-Pin CerDIP ^e	600 mW

Notes:

- Signals on S_X , D_X , or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 5.3 mW/°C above 75°C
- Derate 4 mW/°C above 70°C
- Derate 8 mW/°C above 75°C

SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

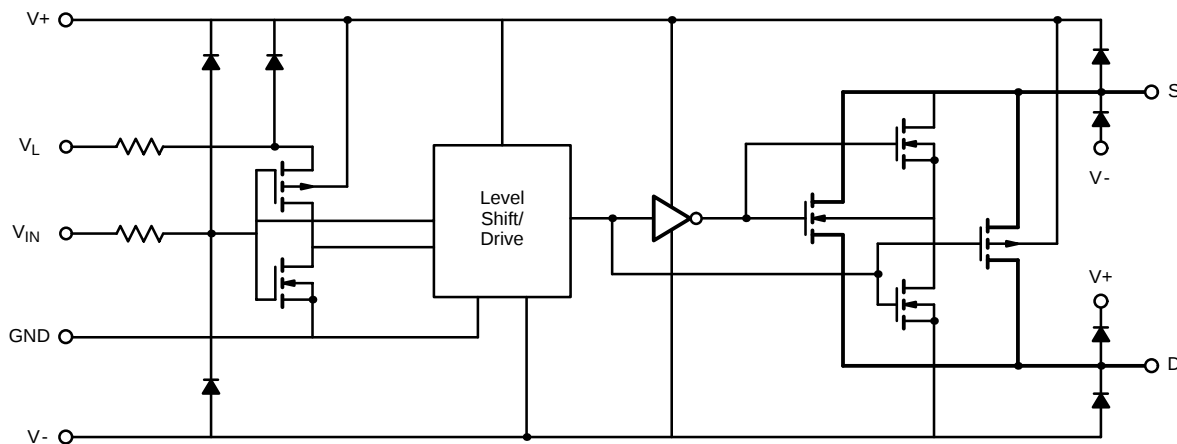


FIGURE 1.

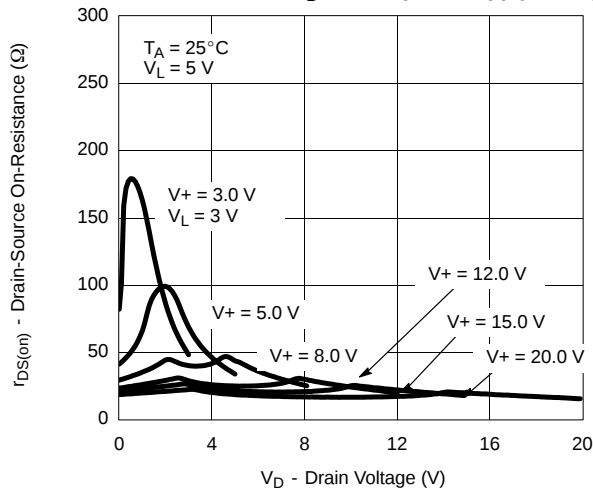
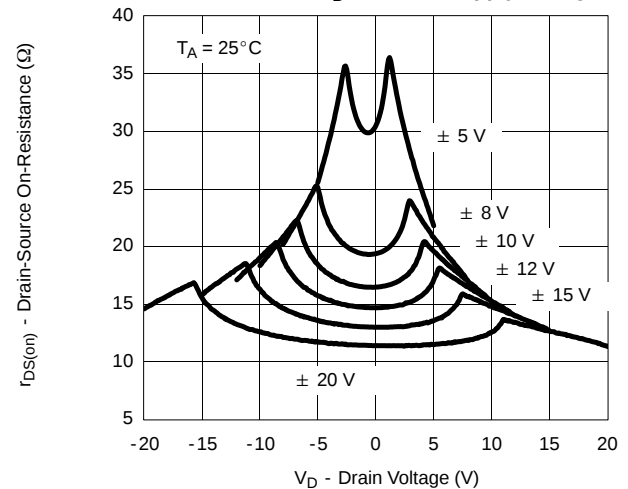
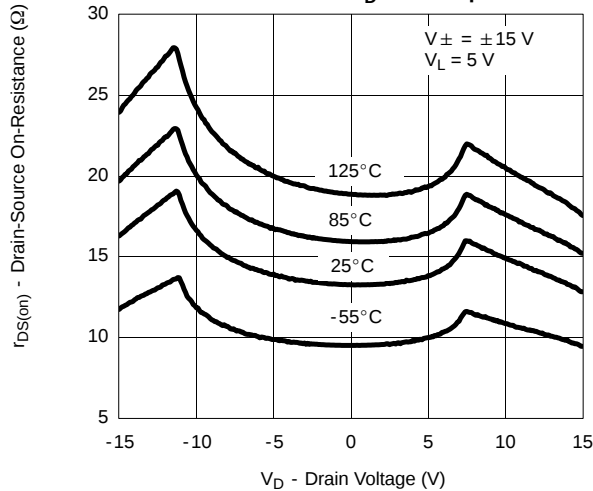
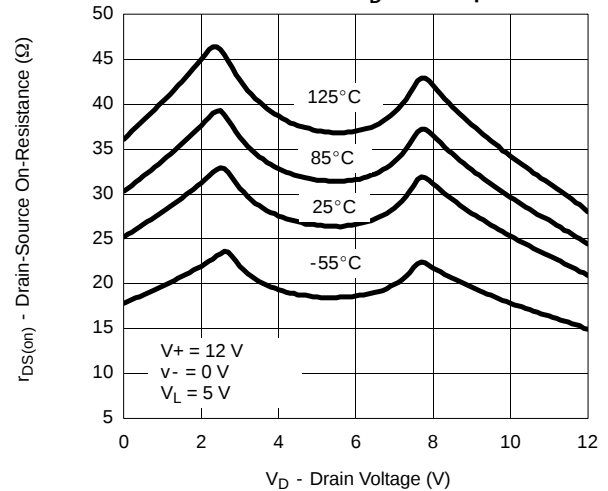
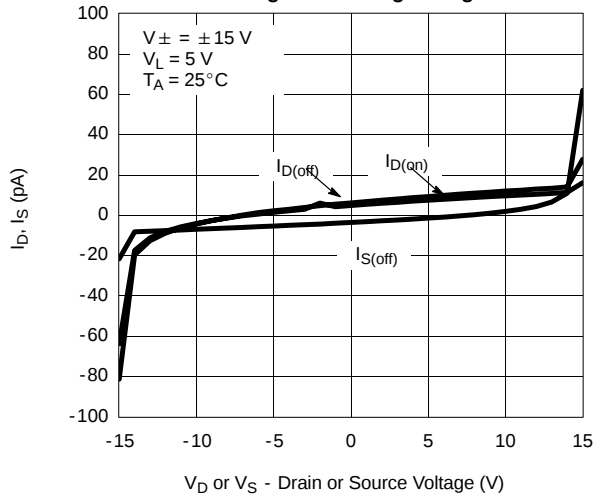
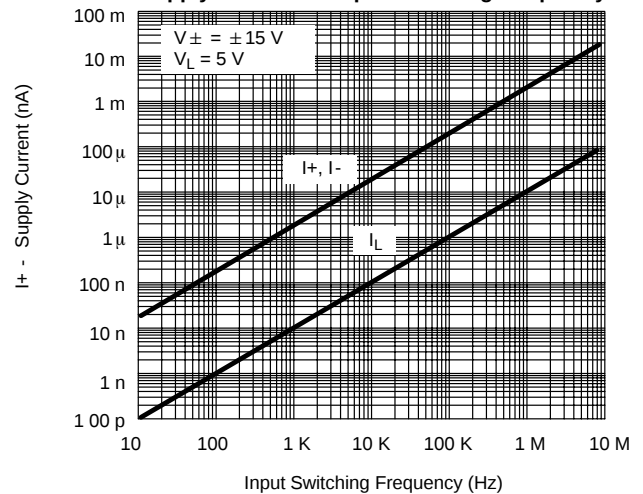


SPECIFICATIONS ^a										
Parameter	Symbol	Test Conditions Unless Otherwise Specified V ⁺ = 15 V, V ⁻ = -15 V V _L = 5 V, V _{IN} = 2.4 V, 0.8 V ^f		Temp ^b	Typ ^c	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
						Min ^d	Max ^d	Min ^d	Max ^d	
Analog Switch										
Analog Signal Range ^e	V _{ANALOG}			Full		-15	15	-15	15	V
Drain-Source On-Resistance	r _{DS(on)}	I _S = -10 mA, V _D = ±12.5 V V ⁺ = 13.5 V, V ⁻ = -13.5 V		Room Full	15		25 34		25 29	Ω
Switch Off Leakage Current	I _{S(off)}	V ⁺ = 16.5 V, V ⁻ = -16.5 V V _D = ∓15.5 V V _S = ±15.5 V	DG417B DG418B	Room Full	-0.1	-0.25 -20	0.25 20	-0.25 -5	0.25 5	nA
	DG419B		Room Full	-0.1	-0.75 -60	0.75 60	-0.75 -12	0.75 12		
	Channel On Leakage Current		I _{D(on)}	DG417B DG418B	Room Full	-0.4	-0.4 -40	0.4 40	-0.4 -10	
DG419B		Room Full		-0.4	-0.75 -60	0.75 60	-0.75 -12	0.75 12		
Digital Control										
Input Current V _{IN} Low	I _{IL}			Full		-0.5	0.5	-0.5	0.5	μA
Input Current V _{IN} High	I _{IH}			Full		-0.5	0.5	-0.5	0.5	
Dynamic Characteristics										
Turn-On Time	t _{ON}	R _L = 300 Ω, C _L = 35 pF V _S = ±10 V See Switching Time Test Circuit	DG417B DG418B	Room Full	62		89 106		89 99	ns
Turn-Off Time	t _{OFF}		DG417B DG418B	Room Full	53		80 88		80 86	
Transition Time	t _{TRANS}	R _L = 300 Ω, C _L = 35 pF V _{S1} = ±10 V, V _{S2} = ∓10 V	DG419B	Room Full	60		87 96		87 93	
Break-Before-Make Time Delay	t _D	R _L = 300 Ω, C _L = 35 pF V _{S1} = V _{S2} = ±10 V	DG419B	Room	16	3		3		
Charge Injection	Q	C _L = 10 nF, V _{gen} = 0 V, R _{gen} = 0 Ω		Room	4					pC
Off-Isolation ^e	OIRR	R _L = 50 Ω, C _L = 5 nF, f = 1 MHz		Room	-86					dB
Channel-To-Channel Crosstalk ^e	X _{TALK}		DG419B	Room	-87					
Source Off Capacitance	C _{S(off)}	f = 1 MHz, V _S = 0 V		Room	12					pF
Drain Off Capacitance	C _{D(off)}		DG417B DG418B	Room	12					
Channel On Capacitance	C _{D(on)}	f = 1 MHz, V _S = 0 V	DG417B DG418B	Room	50					
			DG419B	Room	57					
Power Supplies										
Positive Supply Current	I ⁺	V ⁺ = 16.5 V, V ⁻ = -16.5 V V _{IN} = 0 or 5 V		Room Full	0.001		1 5		1 5	μA
Negative Supply Current	I ⁻			Room Full	-0.001	-1 -5		-1 -5		
Logic Supply Current	I _L			Room Full	0.001		1 5		1 5	
Ground Current	I _{GND}			Room Full	-0.000 1	-1 -5		-1 -5		

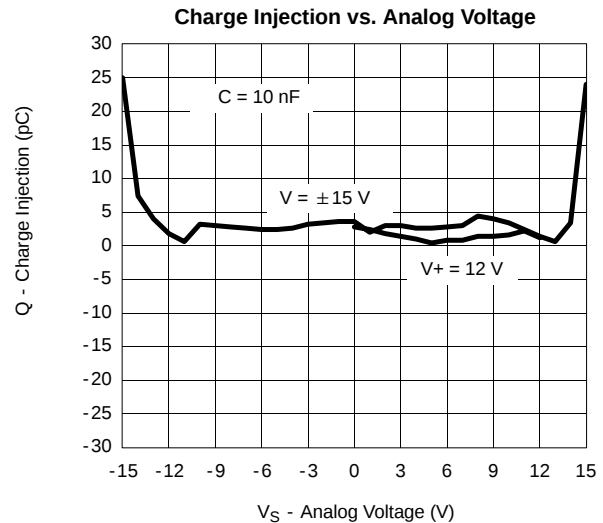
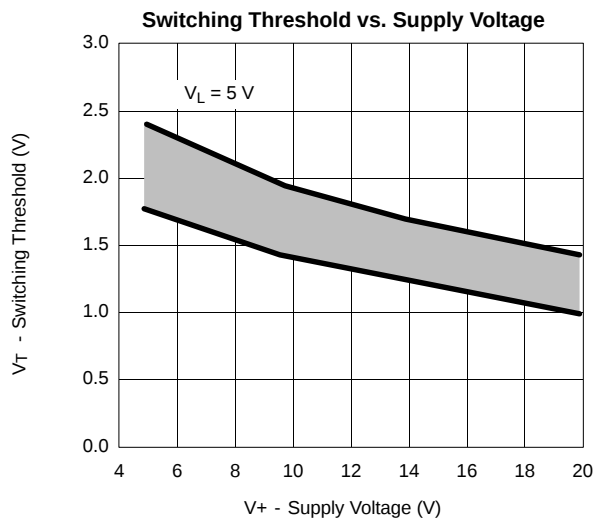
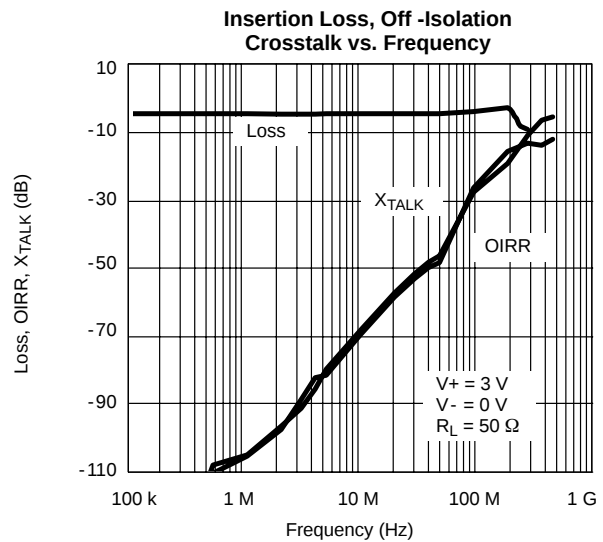
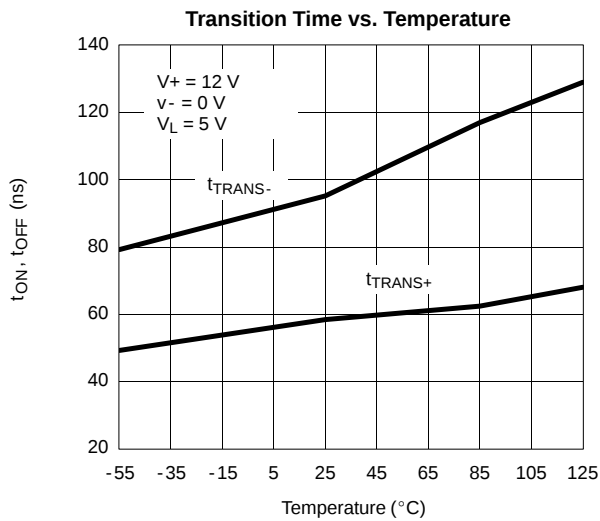
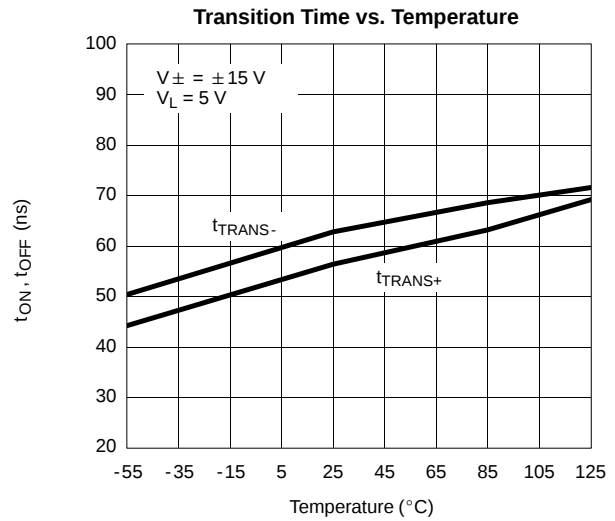
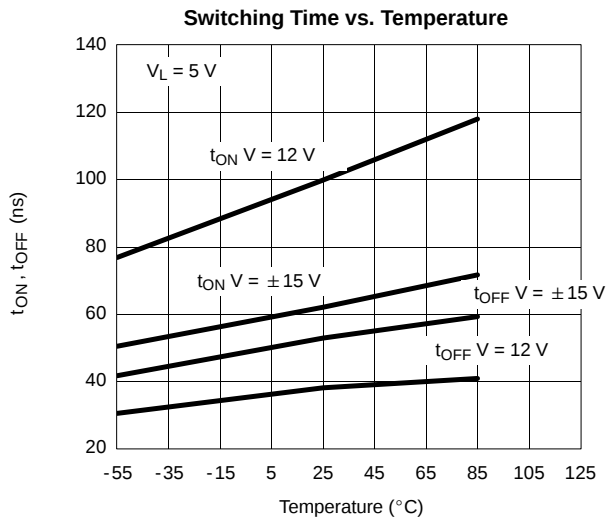
SPECIFICATIONS ^a FOR UNIPOLAR SUPPLIES										
Parameter	Symbol	Test Conditions Unless Otherwise Specified V ⁺ = 12 V, V ⁻ = 0 V V _L = 5 V, V _{IN} = 2.4 V, 0.8 V ^f	Temp ^b	Typ ^c	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit	
					Min ^d	Max ^d	Min ^d	Max ^d		
Analog Switch										
Analog Signal Range ^e	V _{ANALOG}		Full		0	12	0	12	V	
Drain-Source On-Resistance	r _{DS(on)}	I _S = -10 mA, V _D = 3.8 V V ⁺ = 10.8 V	Room Full	26		35 52		35 45	Ω	
Dynamic Characteristics										
Turn-On Time	t _{ON}	R _L = 300 Ω, C _L = 35 pF, V _S = 8 V See Switching Time Test Circuit		Room Full	100		125 155		125 143	ns
Turn-Off Time	t _{OFF}			Room Full	38		66 73		66 69	
Break-Before-Make Time Delay	t _D	R _L = 300 Ω, C _L = 35 pF	DG419B	Room	62	25		25		
Transition Time	t _{TRANS}	R _L = 300 Ω, C _L = 35 pF V _{S1} = 0 V, 8 V, V _{S2} = 8 V, 0 V		Room Full	95		119 153		119 141	
Charge Injection	Q	C _L = 10 nF, V _{gen} = 0 V, R _{gen} = 0 Ω		Room	3					pC
Power Supplies										
Positive Supply Current	I ⁺	V ⁺ = 13.2 V, V _L = 5.25 V V _{IN} = 0 or 5 V		Room Full	0.001		1 5		1 5	μA
Negative Supply Current	I ⁻			Room	-0.001	-1 -5		-1 -5		
Logic Supply Current	I _L			Room	0.001		1 5		1 5	
Ground Current	I _{GND}			Room	-0.001	-1 -5		-1 -5		

Notes:

- Refer to PROCESS OPTION FLOWCHART.
- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- V_{IN} = input voltage to perform proper function.

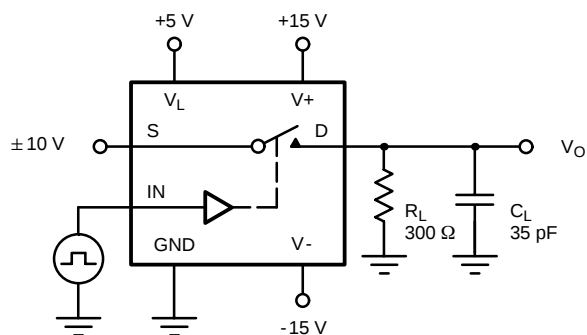
**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)****On-Resistance vs. V_D and Unipolar Supply Voltage****On-Resistance vs. V_D and Dual Supply Voltage****On-Resistance vs. V_D and Temperature****On-Resistance vs. V_D and Temperature****Leakage vs. Analog Voltage****Supply Current vs. Input Switching Frequency**

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



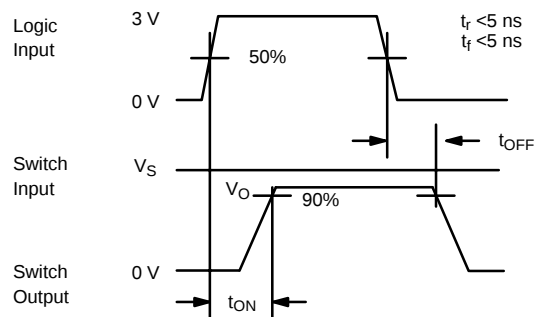
TEST CIRCUITS

V_O is the steady state output with the switch on.



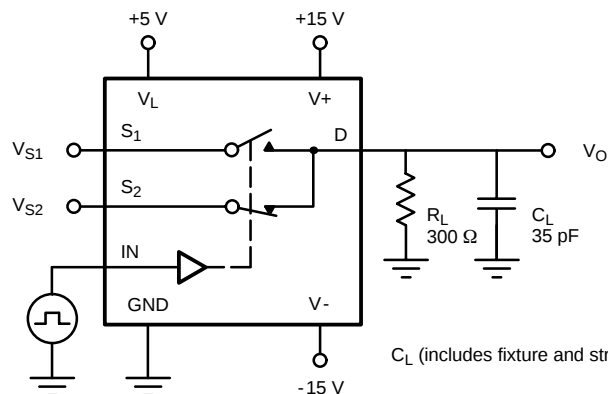
C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$



Note: Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 2. Switching Time (DG417B/418B)



C_L (includes fixture and stray capacitance)

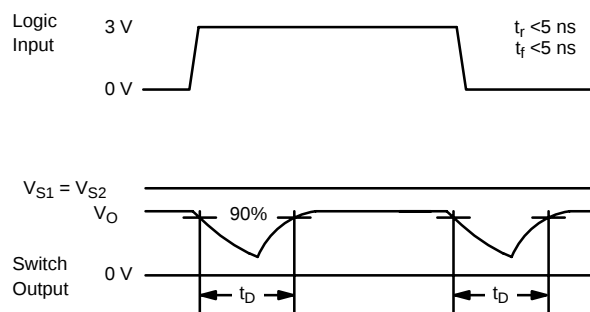
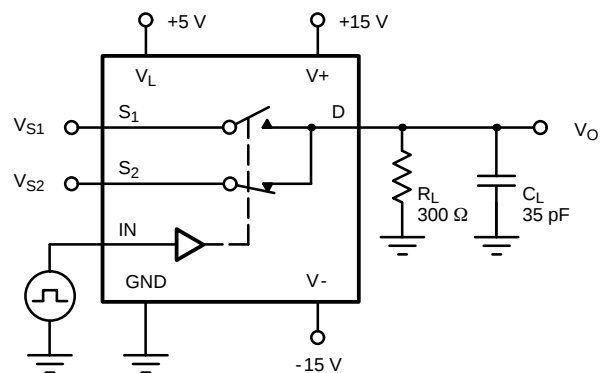


FIGURE 3. Break-Before-Make (DG419B)



C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

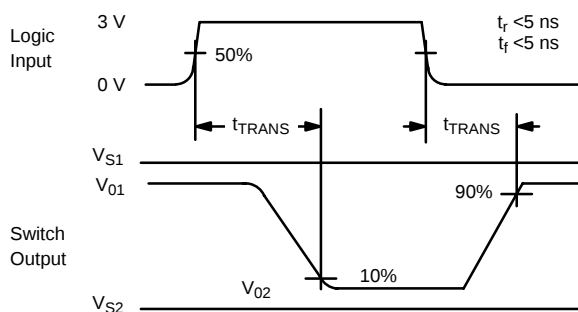


FIGURE 4. Transition Time (DG419B)



TEST CIRCUITS

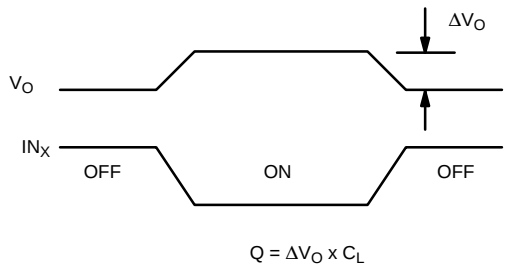
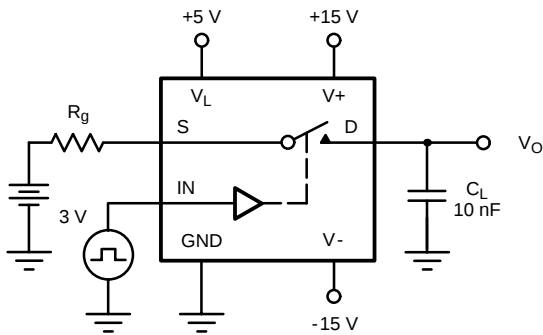


FIGURE 5. Charge Injection

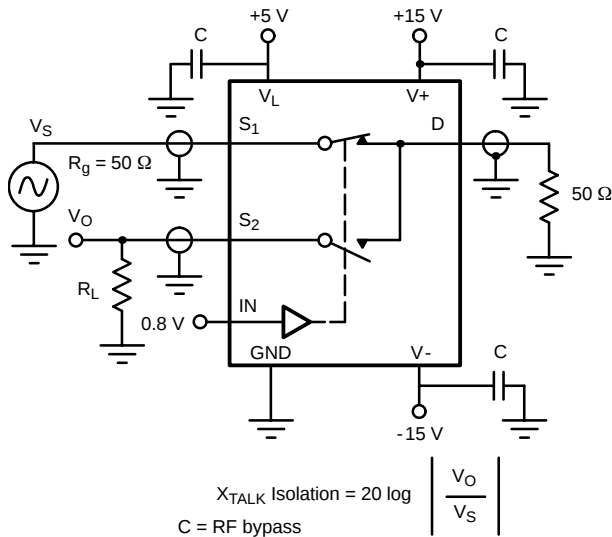


FIGURE 6. Crosstalk (DG419B)

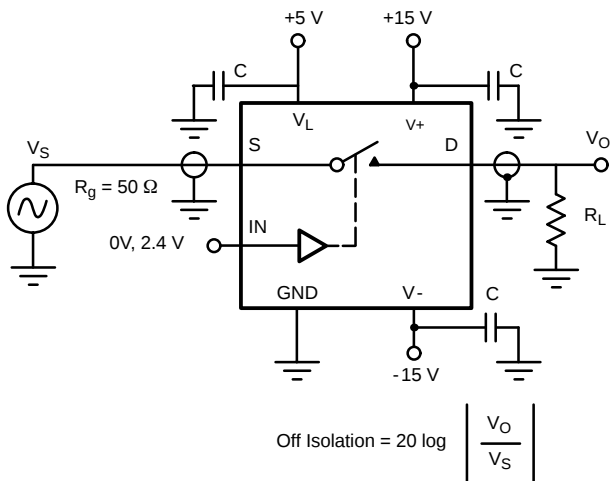


FIGURE 7. Off Isolation

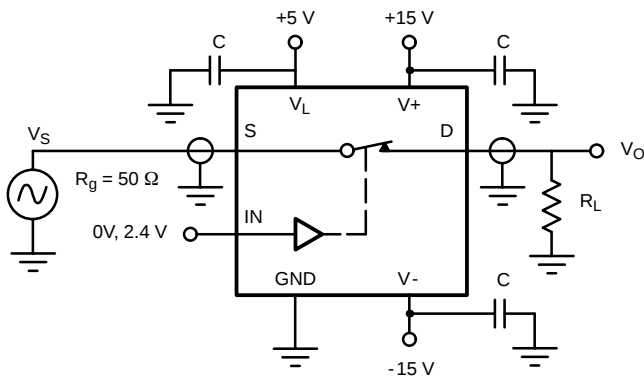
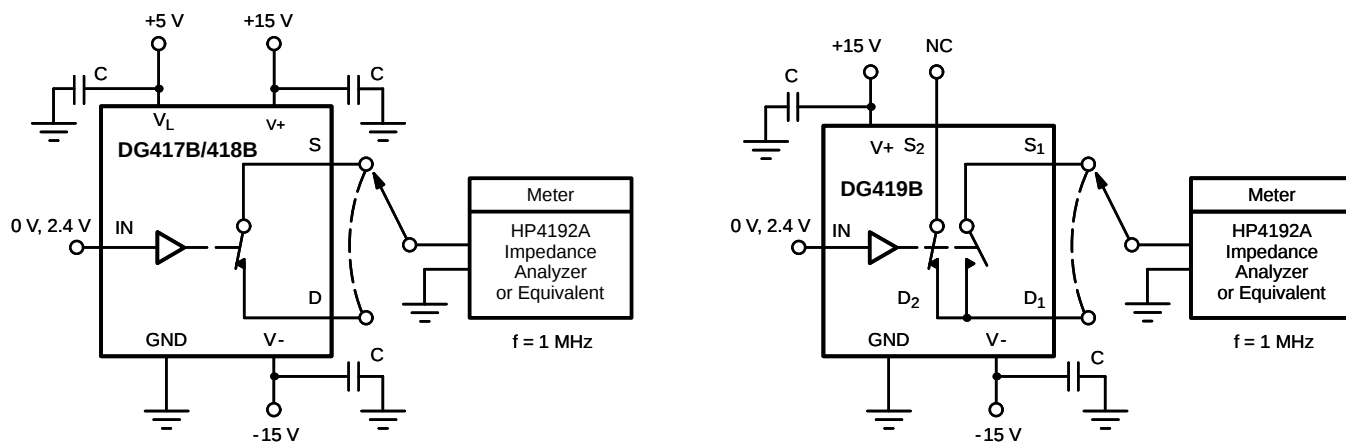


FIGURE 8. Insertion Loss

TEST CIRCUITS

FIGURE 9. Source/Drain Capacitances