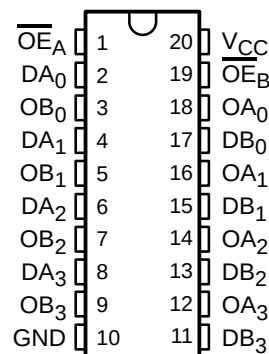


CY54FCT244T, CY74FCT244T 8-BIT BUFFERS/LINE DRIVERS WITH 3-STATE OUTPUTS

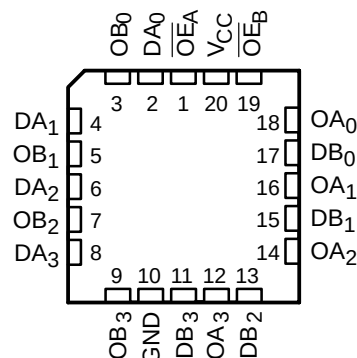
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- Function, Pinout, and Drive Compatible With FCT and F Logic
- Reduced V_{OH} (Typically = 3.3 V) Versions of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- I_{off} Supports Partial-Power-Down Mode Operation
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- Matched Rise and Fall Times
- Fully Compatible With TTL Input and Output Logic Levels
- CY54FCT244T
 - 48-mA Output Sink Current
 - 12-mA Output Source Current
- CY74FCT244T
 - 64-mA Output Sink Current
 - 32-mA Output Source Current
- 3-State Outputs

CY54FCT244T . . . D PACKAGE
CY74FCT244T . . . P, Q, OR SO PACKAGE
(TOP VIEW)



CY54FCT244T . . . L PACKAGE
(TOP VIEW)



description

The 'FCT244T devices are octal buffers and line drivers designed to be employed as memory address drivers, clock drivers, and bus-oriented transmitters/receivers. These devices provide speed and drive capabilities equivalent to their fastest bipolar logic counterparts, while reducing power consumption. The input and output voltage levels allow direct interface with TTL, NMOS, and CMOS devices without external components.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

CY54FCT244T, CY74FCT244T

8-BIT BUFFERS/LINE DRIVERS

WITH 3-STATE OUTPUTS

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ORDERING INFORMATION

T _A	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	QSOP – Q	Tape and reel	3.6	CY74FCT244DTQCT	FCT244D
	SOIC – SO	Tube	3.6	CY74FCT244DTSOC	FCT244D
		Tape and reel	3.6	CY74FCT244DTSOCT	
–40°C to 85°C	SOIC – SO	Tube	4.1	CY74FCT244CTSOC	FCT244C
		Tape and reel	4.1	CY74FCT244CTSOCT	
	QSOP – Q	Tape and reel	4.1	CY74FCT244CTQCT	FCT244C
	DIP – P	Tube	4.6	CY74FCT244ATPC	CY74FCT244ATPC
	SOIC – SO	Tube	4.6	CY74FCT244ATSOC	FCT244A
		Tape and reel	4.6	CY74FCT244ATSOCT	
	QSOP – Q	Tape and reel	4.6	CY74FCT244ATQCT	FCT244A
	SOIC – SO	Tube	6.5	CY74FCT244TSOC	FCT244
		Tape and reel	6.5	CY74FCT244TSOCT	
	QSOP – Q	Tape and reel	6.5	CY74FCT244TQCT	FCT244
–55°C to 125°C	CDIP – D	Tube	4.6	CY54FCT244CTDMB	
	LCC – L	Tube	4.6	CY54FCT244CTLMB	
	CDIP – D	Tube	5.1	CY54FCT244ATDMB	
	LCC – L	Tube	5.1	CY54FCT244ATLMB	
	CDIP – D	Tube	7	CY54FCT244TDMB	
	LCC – L	Tube	7	CY54FCT244TLMB	

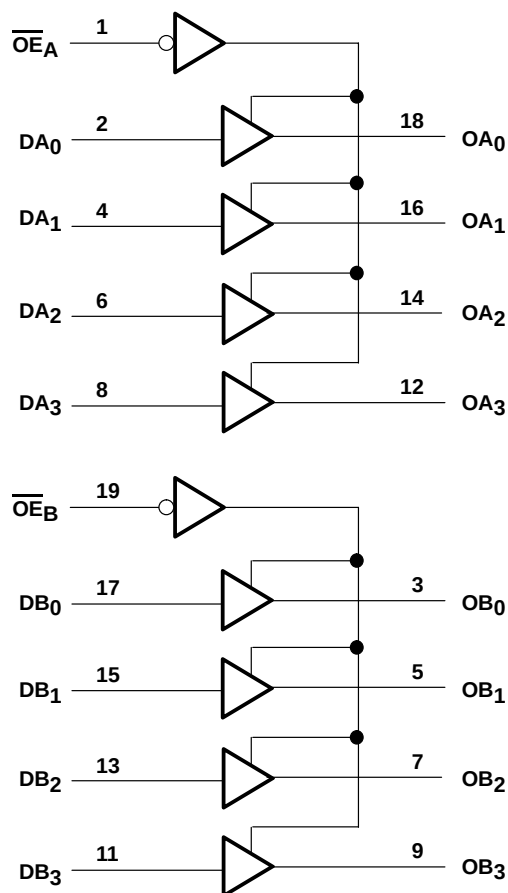
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS			OUTPUT O
$\overline{OE}_A$	$\overline{OE}_B$	D	
L	L	L	L
L	L	H	H
H	H	X	Z

H = High logic level, L = Low logic level,
X = Don't care, Z = High-impedance state

logic diagram (positive logic)



absolute maximum rating over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range to ground potential	–0.5 V to 7 V
DC input voltage range	–0.5 V to 7 V
DC output voltage range	–0.5 V to 7 V
DC output current (maximum sink current/pin)	120 mA
Package thermal impedance, θ_{JA} (see Note 1): P package	69°C/W
Q package	68°C/W
SO package	58°C/W
Ambient temperature range with power applied, T_A	–65°C to 135°C
Storage temperature range, T_{Stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

CY54FCT244T, CY74FCT244T

8-BIT BUFFERS/LINE DRIVERS

WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 2)

	CY54FCT244T			CY74FCT244DT			CY74FCT244T			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			2			V
V _{IL} Low-level input voltage			0.8			0.8			0.8	V
I _{OH} High-level output current			–12			–32			–32	mA
I _{OL} Low-level output current			48			64			64	mA
T _A Operating free-air temperature	–55		125	0		70	–40		85	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.



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CY54FCT244T, CY74FCT244T
8-BIT BUFFERS/LINE DRIVERS
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	CY54FCT244T			CY74FCT244T			UNIT
		MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
V_{IK}	$V_{CC} = 4.5 \text{ V}$, $I_{IN} = -18 \text{ mA}$		-0.7	-1.2				V
	$V_{CC} = 4.75 \text{ V}$, $I_{IN} = -18 \text{ mA}$					-0.7	-1.2	
V_{OH}	$V_{CC} = 4.5 \text{ V}$, $I_{OH} = -12 \text{ mA}$	2.4	3.3					V
	$V_{CC} = 4.75 \text{ V}$				2			
					2.4	3.3		
V_{OL}	$V_{CC} = 4.5 \text{ V}$, $I_{OL} = 48 \text{ mA}$	0.3	0.55					V
	$V_{CC} = 4.75 \text{ V}$, $I_{OL} = 64 \text{ mA}$				0.3	0.55		
V_{hys}	All inputs	0.2			0.2			V
I_I	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = V_{CC}$			5				μA
	$V_{CC} = 5.25 \text{ V}$, $V_{IN} = V_{CC}$						5	
I_{IH}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 2.7 \text{ V}$			± 1				μA
	$V_{CC} = 5.25 \text{ V}$, $V_{IN} = 2.7 \text{ V}$						± 1	
I_{IL}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 0.5 \text{ V}$			± 1				μA
	$V_{CC} = 5.25 \text{ V}$, $V_{IN} = 0.5 \text{ V}$						± 1	
I_{OZH}	$V_{CC} = 5.5 \text{ V}$, $V_{OUT} = 2.7 \text{ V}$			10				μA
	$V_{CC} = 5.25 \text{ V}$, $V_{OUT} = 2.7 \text{ V}$						10	
I_{OZL}	$V_{CC} = 5.5 \text{ V}$, $V_{OUT} = 0.5 \text{ V}$			-10				μA
	$V_{CC} = 5.25 \text{ V}$, $V_{OUT} = 0.5 \text{ V}$						-10	
$I_{OS}^{\ddagger}$	$V_{CC} = 5.5 \text{ V}$, $V_{OUT} = 0 \text{ V}$	-60	-120	-225				mA
	$V_{CC} = 5.25 \text{ V}$, $V_{OUT} = 0 \text{ V}$				-60	-120	-225	
I_{off}	$V_{CC} = 0 \text{ V}$, $V_{OUT} = 4.5 \text{ V}$			± 1			± 1	μA
I_{CC}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} \leq 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$	0.1	0.2					mA
	$V_{CC} = 5.25 \text{ V}$, $V_{IN} \leq 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$				0.1	0.2		
ΔI_{CC}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 3.4 \text{ V}^{\S}$, $f_1 = 0$, Outputs open	0.5	2					mA
	$V_{CC} = 5.25 \text{ V}$, $V_{IN} = 3.4 \text{ V}^{\S}$, $f_1 = 0$, Outputs open				0.5	2		
$I_{CCD}^{\P}$	$V_{CC} = 5.5 \text{ V}$, One input switching at 50% duty cycle, Outputs open, $\overline{OE}_A = \overline{OE}_B = \text{GND}$, $V_{IN} \leq 0.2 \text{ V}$ or $V_{IN} \geq V_{CC} - 0.2 \text{ V}$	0.06	0.12					mA/ MHz
	$V_{CC} = 5.25 \text{ V}$, One input switching at 50% duty cycle, Outputs open, $\overline{OE}_A = \overline{OE}_B = \text{GND}$, $V_{IN} \leq 0.2 \text{ V}$ or $V_{IN} \geq V_{CC} - 0.2 \text{ V}$				0.06	0.12		

[†] Typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

[‡] Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

[§] Per TTL-driven input ($V_{IN} = 3.4 \text{ V}$); all other inputs at V_{CC} or GND

[¶] This parameter is derived for use in total power-supply calculations.

CY54FCT244T, CY74FCT244T

8-BIT BUFFERS/LINE DRIVERS

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS			CY54FCT244T			CY74FCT244T			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
I _C [#]	V _{CC} = 5.5 V, Outputs open, OE _A = OE _B = GND	One bit switching at f ₁ = 10 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V	0.7	1.4				mA	
			V _{IN} = 3.4 V or GND	1	2.4					
		Eight bits switching at f ₁ = 2.5 MHz at 50% duty cycle	V _{IN} = 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V	1.3	2.6					
			V _{IN} = 3.4 V or GND	3.3	10.6					
	V _{CC} = 5.25 V, Outputs open, OE _A = OE _B = GND	One bit switching at f ₁ = 10 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V			0.7	1.4			
			V _{IN} = 3.4 V or GND			1	2.4			
		Eight bits switching at f ₁ = 2.5 MHz at 50% duty cycle	V _{IN} = 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V			1.3	2.6			
			V _{IN} = 3.4 V or GND			3.3	10.6			
C _i				5	10	5	10	pF		
C _O				9	12	9	12	pF		

† Typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

$I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$

Where:

I_C = Total supply current

I_{CC} = Power-supply current with CMOS input levels

ΔI_{CC} = Power-supply current for a TTL high input ($V_{IN} = 3.4 \text{ V}$)

D_H = Duty cycle for TTL inputs high

N_T = Number of TTL inputs at D_H

I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)

f_0 = Clock frequency for registered devices, otherwise zero

f_1 = Input signal frequency

N_1 = Number of inputs changing at f_1

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the I_{CC} formula.

switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY54FCT244T		CY54FCT244AT		CY54FCT244CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	D	O	1.5	7	1.5	5.1	1.5	4.6	ns
t _{PHL}			1.5	7	1.5	5.1	1.5	4.6	
t _{PZH}	$\overline{OE}$	O	1.5	8.5	1.5	6.5	1.5	6.5	ns
t _{PZL}			1.5	8.5	1.5	6.5	1.5	6.5	
t _{PHZ}	$\overline{OE}$	O	1.5	7.5	1.5	5.9	1.5	5.7	ns
t _{PLZ}			1.5	7.5	1.5	5.9	1.5	5.7	

switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY74FCT244T		CY74FCT244AT		CY74FCT244CT		CY74FCT244DT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	D	O	1.5	6.5	1.5	4.6	1.5	4.1	1.5	3.6	ns
t _{PHL}			1.5	6.5	1.5	4.6	1.5	4.1	1.5	3.6	
t _{PZH}	$\overline{OE}$	O	1.5	8	1.5	6.2	1.5	5.8	1.5	4.8	ns
t _{PZL}			1.5	8	1.5	6.2	1.5	5.8	1.5	4.8	
t _{PHZ}	$\overline{OE}$	O	1.5	7	1.5	5.6	1.5	5.2	1.5	4	ns
t _{PLZ}			1.5	7	1.5	5.6	1.5	5.2	1.5	4	

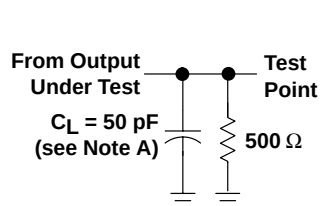
CY54FCT244T, CY74FCT244T

8-BIT BUFFERS/LINE DRIVERS

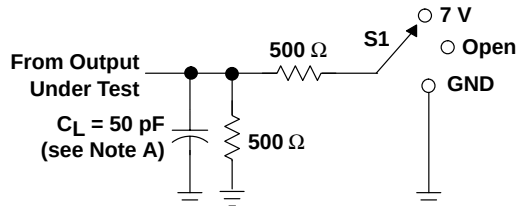
WITH 3-STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION

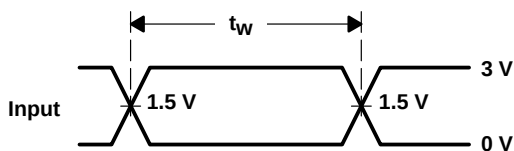


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

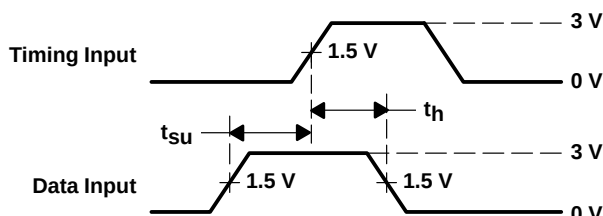


LOAD CIRCUIT FOR
3-STATE OUTPUTS

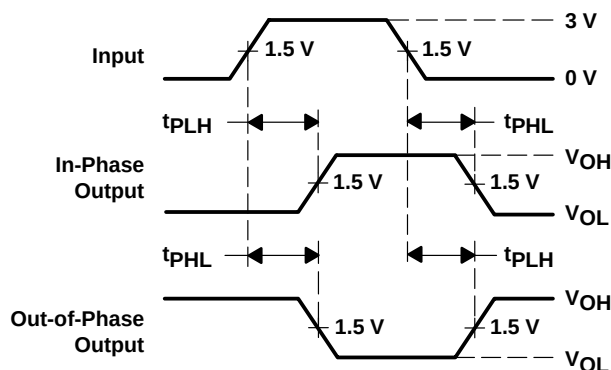
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



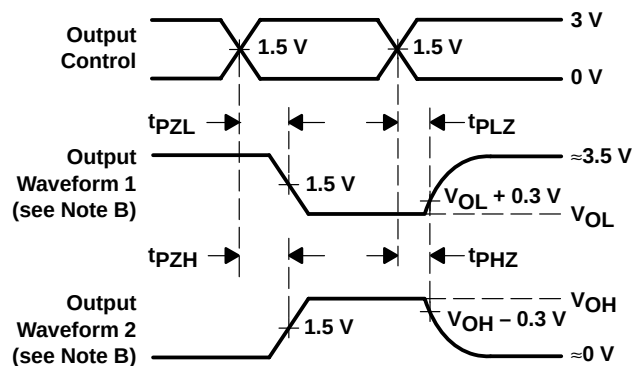
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9220301M2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9220301M2A CY54FCT 244TLMB
5962-9220301MRA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9220301MR A CY54FCT244TDMB
5962-9220301MSA	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9220301MS A CY54FCT244TW
5962-9220302M2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9220302M2A CY54FCT 244ATLMB
5962-9220302MRA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9220302MR A CY54FCT244ATDM B
5962-9220302MSA	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9220302MS A CY54FCT244ATW
5962-9220303M2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9220303M2A
5962-9220303MRA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9220303MR A CY54FCT244CTDM B
CY54FCT244ATDMB	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9220302MR A CY54FCT244ATDM B
CY54FCT244ATLMB	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9220302M2A CY54FCT 244ATLMB

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CY54FCT244ATW	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9220302MS A CY54FCT244ATW
CY54FCT244CTDMB	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9220303MR A CY54FCT244CTDM B
CY54FCT244TDMB	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9220301MR A CY54FCT244TDMB
CY54FCT244TLMB	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9220301M2A CY54FCT 244TLMB
CY54FCT244TW	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9220301MS A CY54FCT244TW
CY74FCT244ATPC	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	CY74FCT244ATPC
CY74FCT244ATPC.B	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	CY74FCT244ATPC
CY74FCT244ATQCT	Active	Production	SSOP (DBQ) 20	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT244A
CY74FCT244ATQCT.B	Active	Production	SSOP (DBQ) 20	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT244A
CY74FCT244ATQCTE4	Active	Production	SSOP (DBQ) 20	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT244A
CY74FCT244ATSOC	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT244A
CY74FCT244ATSOC.B	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT244A
CY74FCT244ATSOCT	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT244A
CY74FCT244ATSOCT.B	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT244A
CY74FCT244CTQCT	Active	Production	SSOP (DBQ) 20	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT244C
CY74FCT244CTQCT.B	Active	Production	SSOP (DBQ) 20	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT244C
CY74FCT244CTSOC	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT244C
CY74FCT244CTSOC.B	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT244C
CY74FCT244DTSOC	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT244D
CY74FCT244DTSOC.B	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT244D
CY74FCT244DTSOCT	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT244D
CY74FCT244DTSOCT.B	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT244D

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CY74FCT244TQCT	Active	Production	SSOP (DBQ) 20	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT244
CY74FCT244TQCT.B	Active	Production	SSOP (DBQ) 20	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT244
CY74FCT244TSOC	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT244
CY74FCT244TSOC.B	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT244
CY74FCT244TSOCG4	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT244
CY74FCT244TSOCG4.B	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT244
CY74FCT244TSOCT	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT244
CY74FCT244TSOCT.B	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT244

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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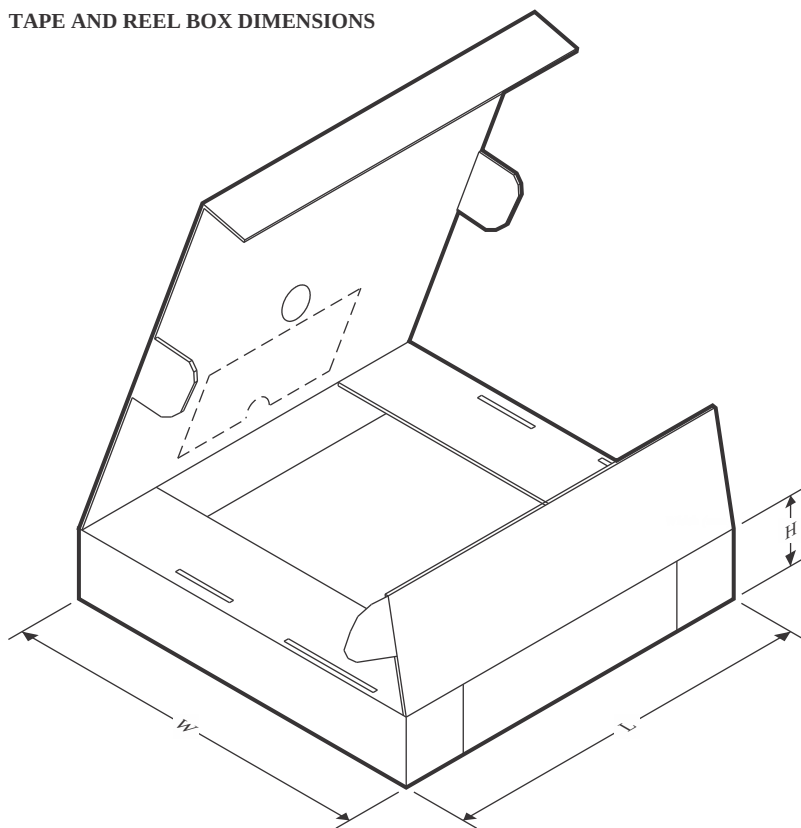
TAPE AND REEL INFORMATION



*All dimensions are nominal

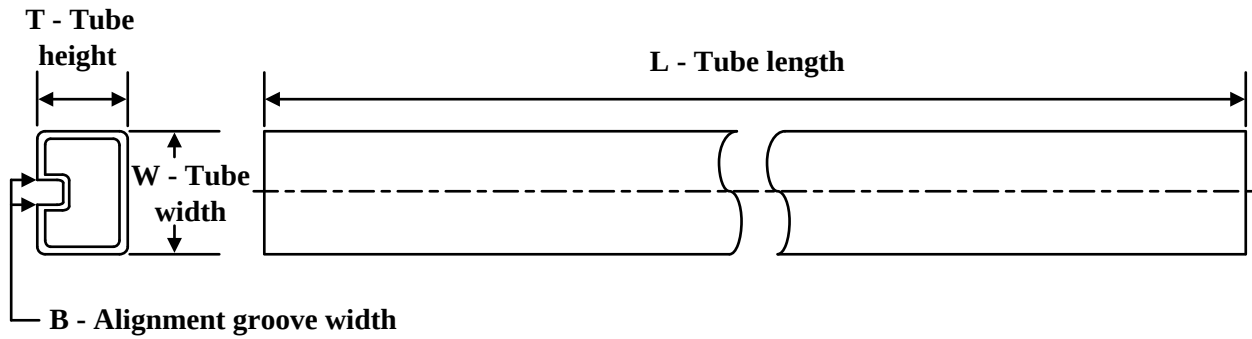
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT244ATQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT244ATSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CY74FCT244CTQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT244DTSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CY74FCT244TQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT244TSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT244ATQCT	SSOP	DBQ	20	2500	353.0	353.0	32.0
CY74FCT244ATSOCT	SOIC	DW	20	2000	356.0	356.0	45.0
CY74FCT244CTQCT	SSOP	DBQ	20	2500	353.0	353.0	32.0
CY74FCT244DTSOCT	SOIC	DW	20	2000	356.0	356.0	45.0
CY74FCT244TQCT	SSOP	DBQ	20	2500	353.0	353.0	32.0
CY74FCT244TSOCT	SOIC	DW	20	2000	356.0	356.0	45.0

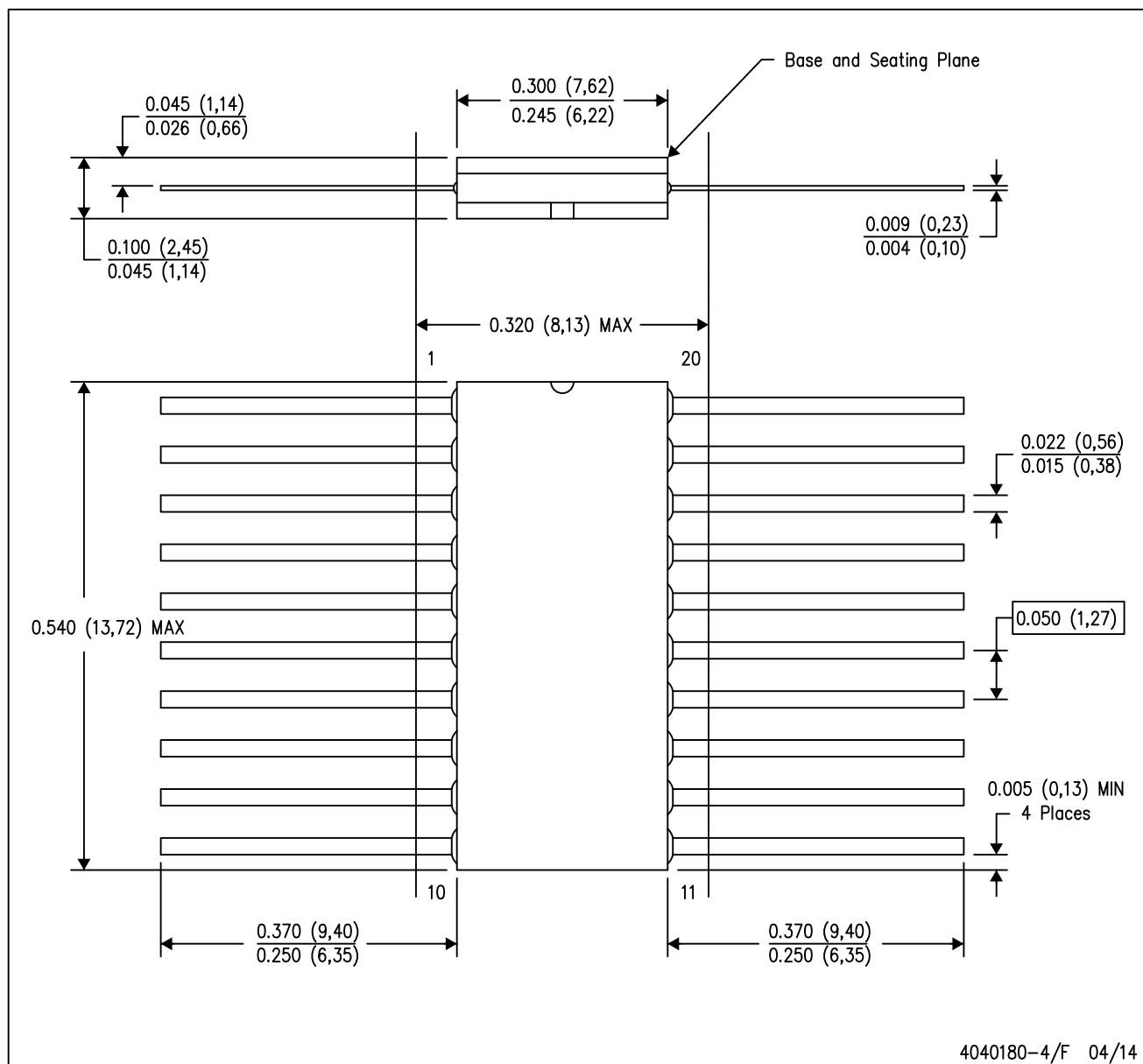
TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9220301M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9220301MSA	W	CFP	20	25	506.98	26.16	6220	NA
5962-9220302M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9220302MSA	W	CFP	20	25	506.98	26.16	6220	NA
5962-9220303M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
CY54FCT244ATLMB	FK	LCCC	20	55	506.98	12.06	2030	NA
CY54FCT244ATW	W	CFP	20	25	506.98	26.16	6220	NA
CY54FCT244TLMB	FK	LCCC	20	55	506.98	12.06	2030	NA
CY54FCT244TW	W	CFP	20	25	506.98	26.16	6220	NA
CY74FCT244ATPC	N	PDIP	20	20	506	13.97	11230	4.32
CY74FCT244ATPC.B	N	PDIP	20	20	506	13.97	11230	4.32
CY74FCT244ATSOC	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT244ATSOC.B	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT244CTSOC	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT244CTSOC.B	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT244DTSOC	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT244DTSOC.B	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT244TSOC	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT244TSOC.B	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT244TSOCG4	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT244TSOCG4.B	DW	SOIC	20	25	507	12.83	5080	6.6

W (R-GDFP-F20)

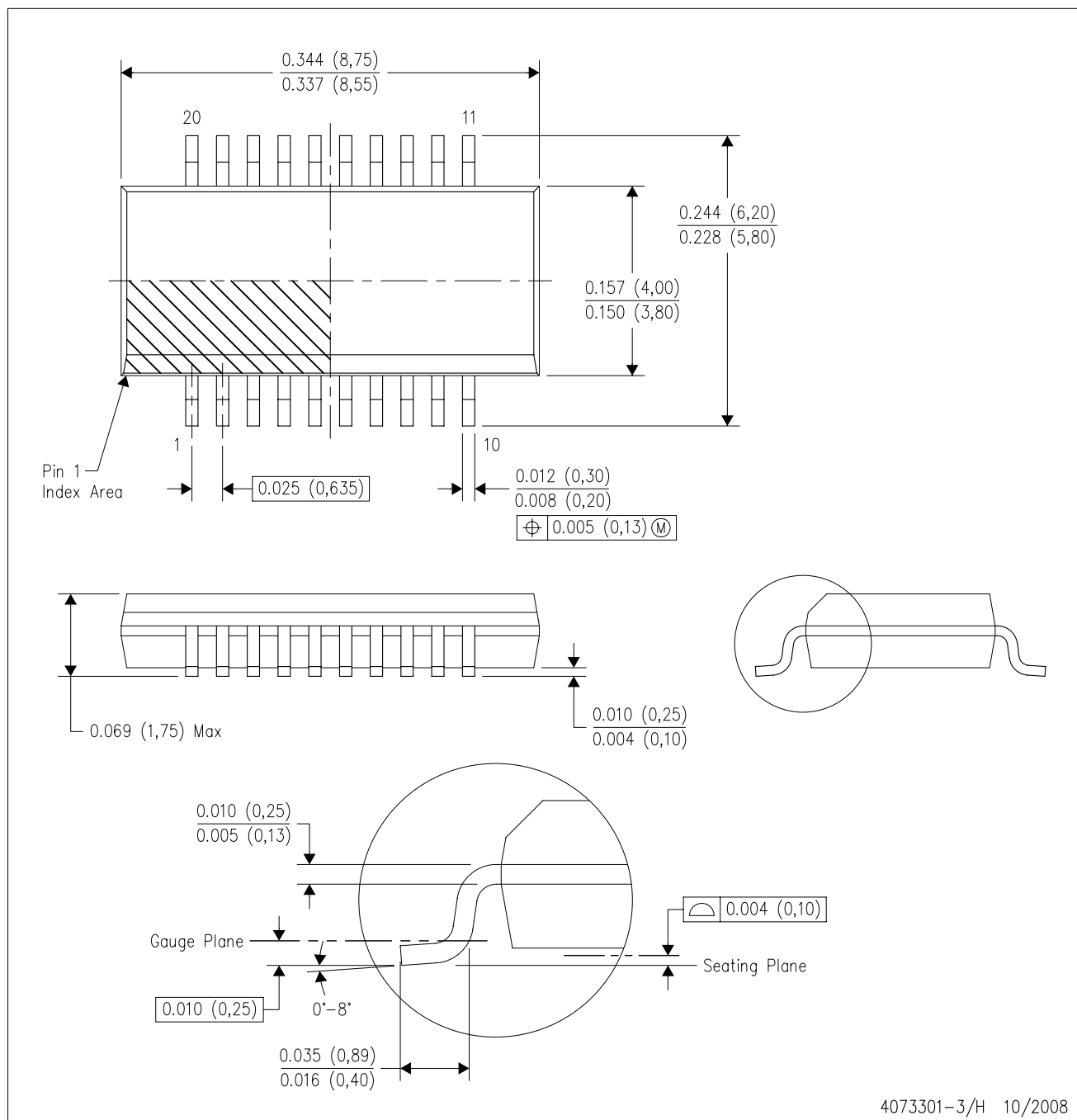
CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

DBQ (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



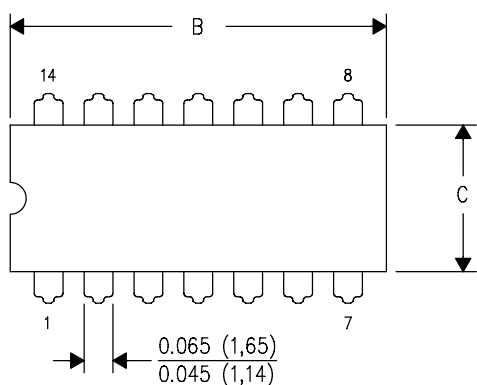
4073301-3/H 10/2008

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
 - D. Falls within JEDEC MO-137 variation AD.

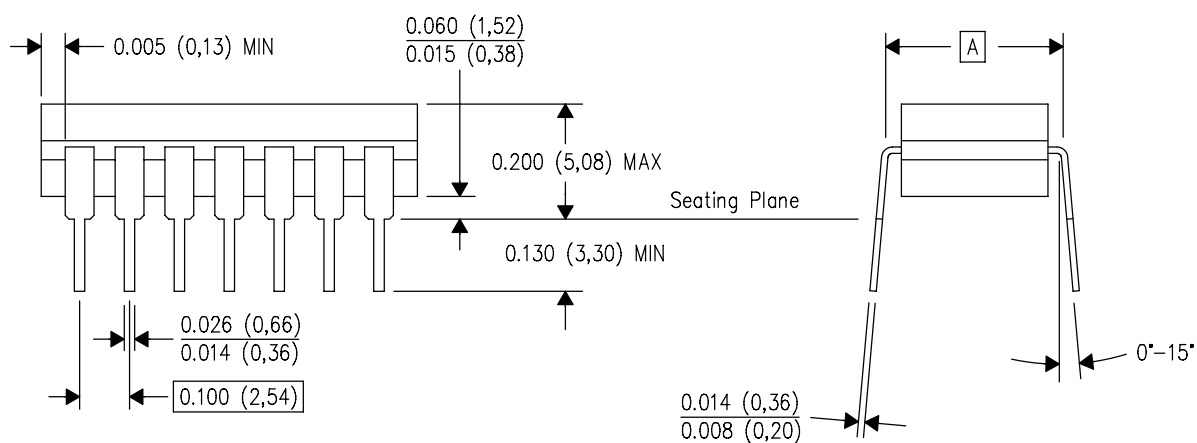
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

GENERIC PACKAGE VIEW

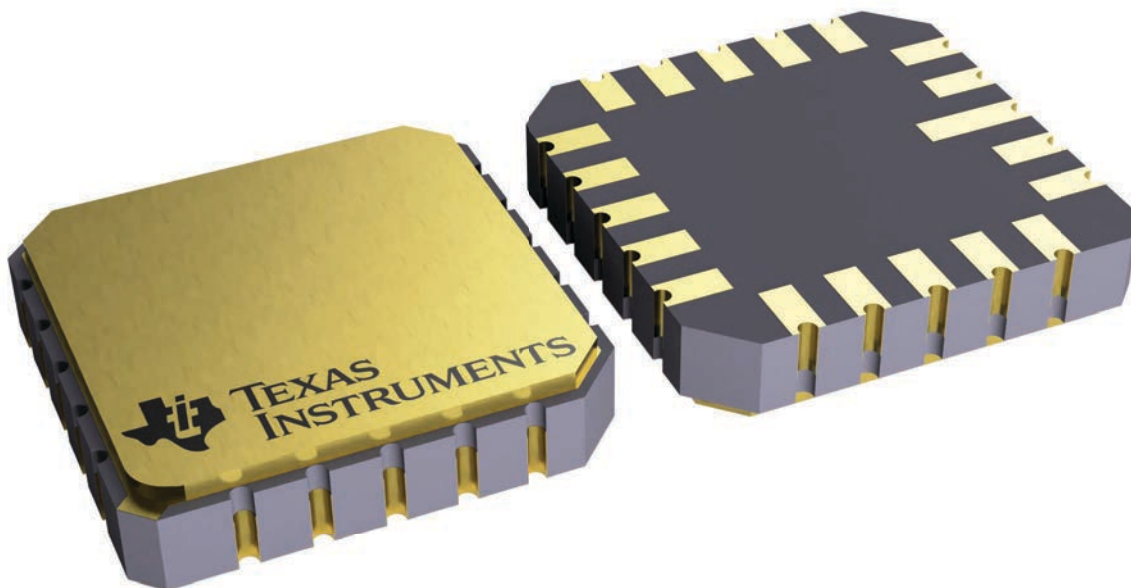
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

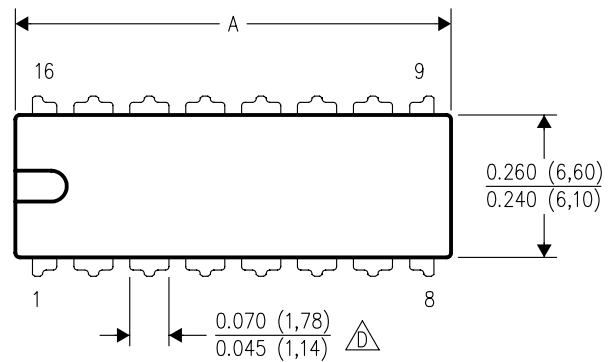


4229370VA\

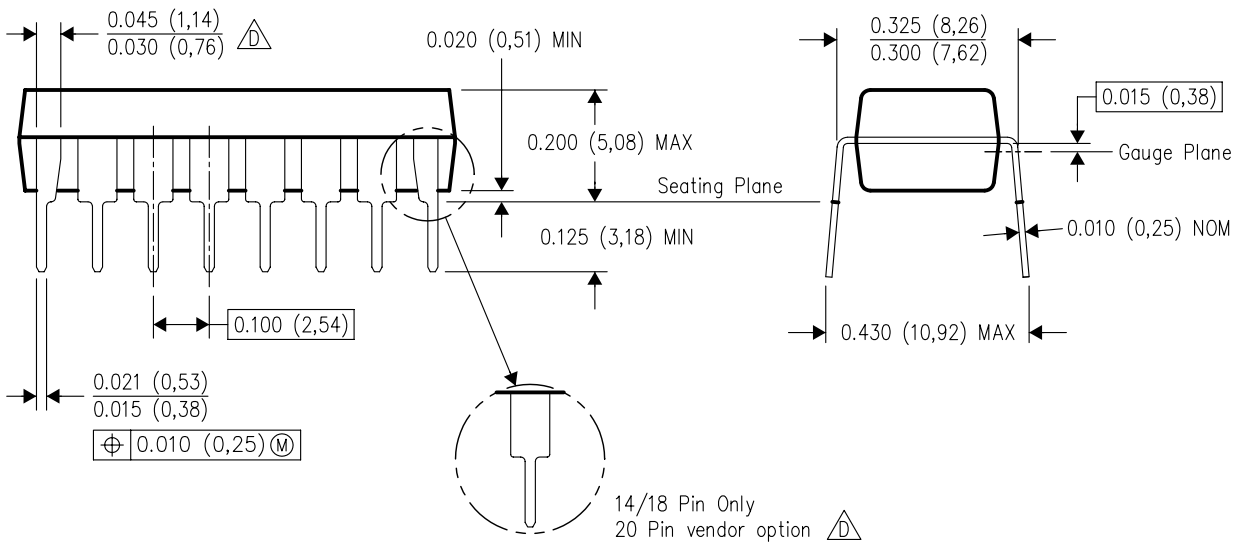
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

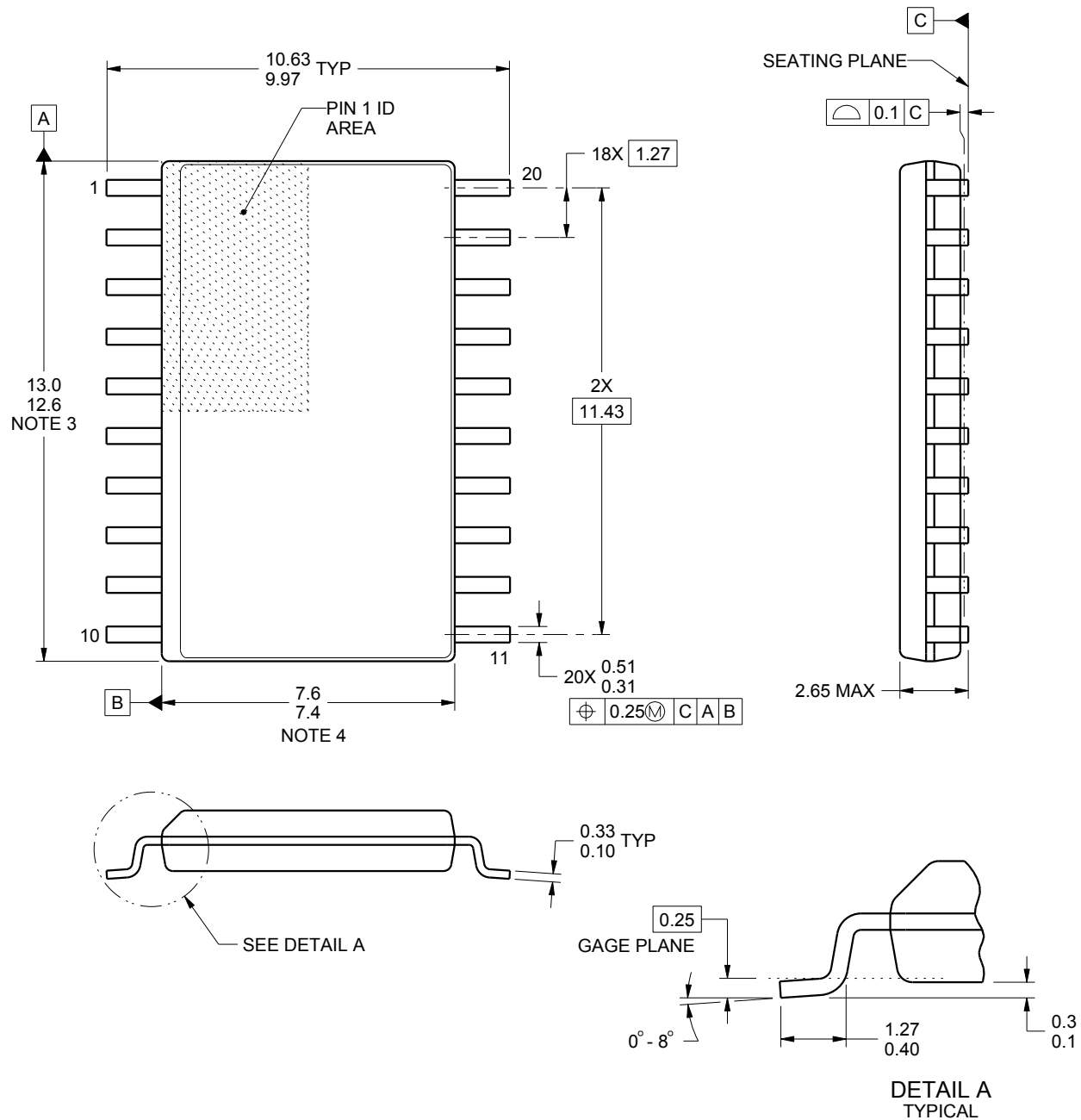
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW0020A

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

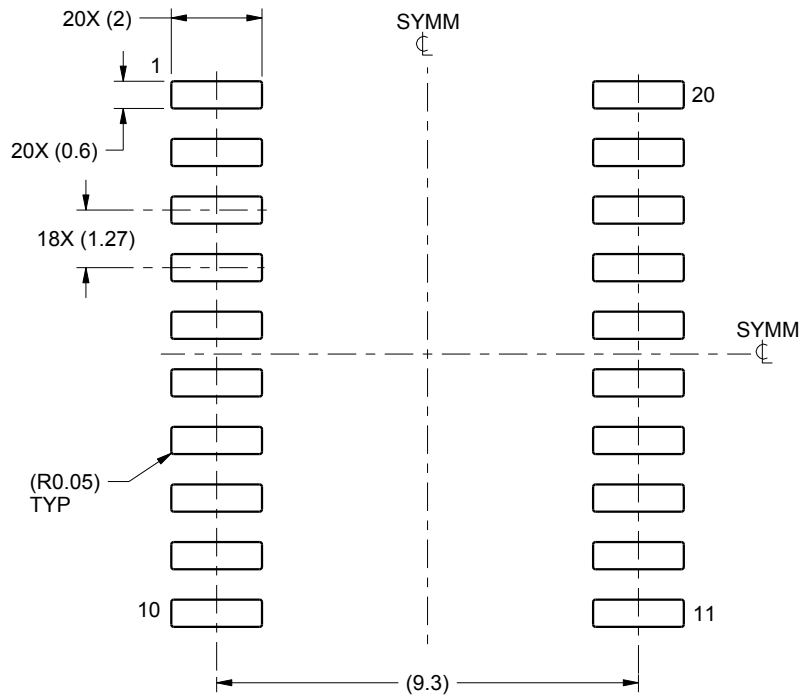
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

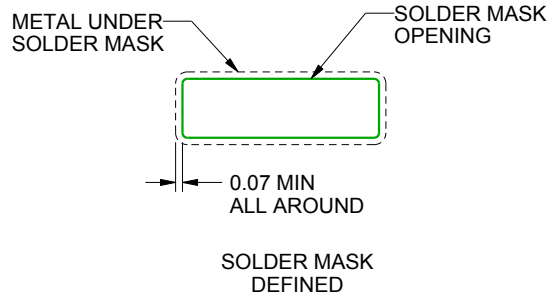
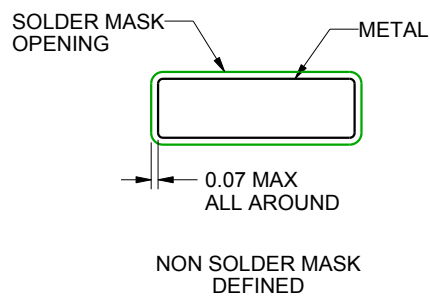
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

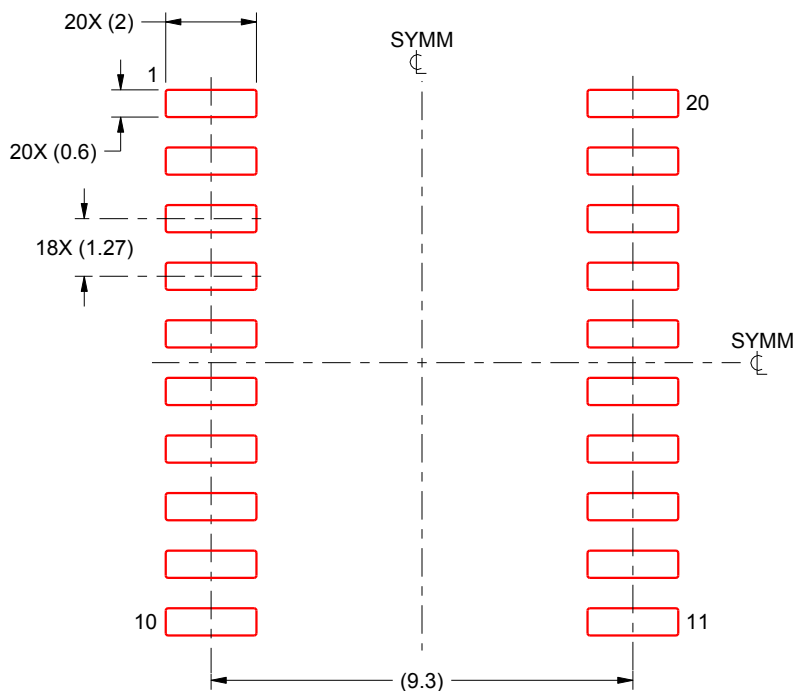
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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