

## 256 Kb (256K x 1) Static RAM

### Features

- Fast access time: 12 ns
- Wide voltage range: 5.0V  $\pm$  10% (4.5V to 5.5V)
- CMOS for optimum speed and power
- TTL compatible inputs and outputs
- Available in 24-lead DIP and 24-lead SOJ

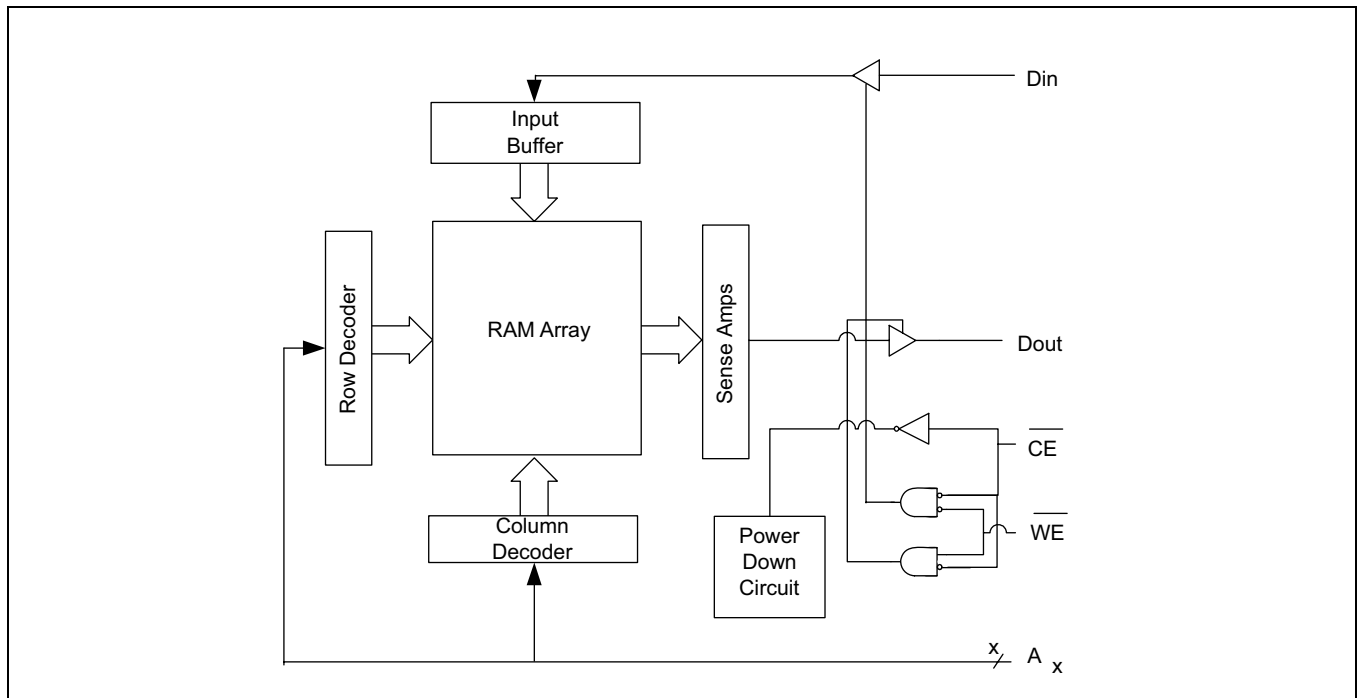
### General Description <sup>[1]</sup>

The CY7C197BN is a high performance CMOS Asynchronous SRAM organized as 256K  $\times$  1 bits that supports an asynchronous memory interface. The device features an automatic power down feature that significantly reduces power consumption when deselected.

See the "Truth Table" on page 7 for a complete description of Read and Write modes.

The CY7C197BN is available in 24-lead DIP and 24-lead SOJ package(s).

### Logic Block Diagram



### Product Portfolio

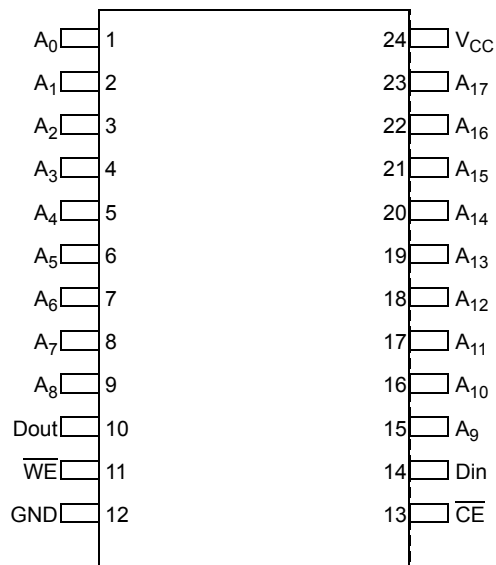
|                              | -12 | -15 | -25 | Unit |
|------------------------------|-----|-----|-----|------|
| Maximum Access Time          | 12  | 15  | 25  | ns   |
| Maximum Operating Current    | 150 | 150 | 95  | mA   |
| Maximum CMOS Standby Current | 10  | 10  | 10  | mA   |

#### Notes

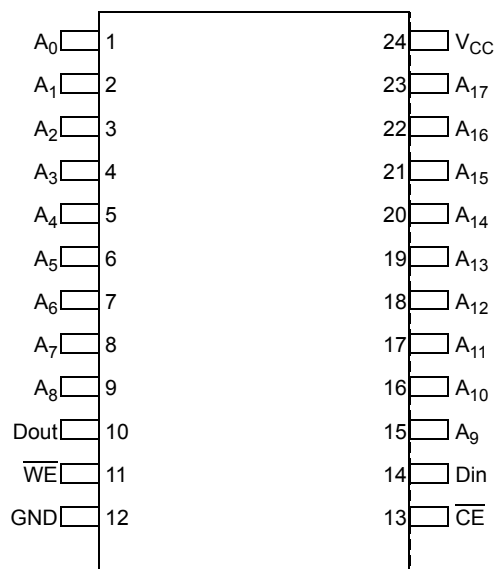
1. For best practice recommendations, refer to the Cypress application note [System Design Guidelines](http://www.cypress.com) on [www.cypress.com](http://www.cypress.com).

## Pin Layout and Specification

### 24-lead DIP (6.6 × 31.8 × 3.5 mm)



### 24-lead SOJ (8 × 15 × 3.5 mm)



## Pin Description

| Pin             | Type    | Description      | DIP                                                           | SOJ                                                           |
|-----------------|---------|------------------|---------------------------------------------------------------|---------------------------------------------------------------|
| A <sub>x</sub>  | Input   | Address Inputs   | 1, 2, 3, 4, 5, 6, 7, 8, 9, 15, 16, 17, 18, 19, 20, 21, 22, 23 | 1, 2, 3, 4, 5, 6, 7, 8, 9, 15, 16, 17, 18, 19, 20, 21, 22, 23 |
| $\overline{CE}$ | Control | Chip Enable      | 13                                                            | 13                                                            |
| Din             | Input   | Data Input Pins  | 14                                                            | 14                                                            |
| Dout            | Output  | Data Output Pins | 10                                                            | 10                                                            |
| V <sub>CC</sub> | Supply  | Power (5.0V)     | 24                                                            | 24                                                            |
| $\overline{WE}$ | Control | Write Enable     | 11                                                            | 11                                                            |

## Maximum Ratings

Exceeding the maximum rating may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with  
Power Applied ..... -55°C to +125°C

Supply Voltage on  $V_{CC}$  to Relative GND ..... -0.5V to +7.0V

DC Voltage Applied to Outputs  
in High Z State<sup>[2]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

DC Input Voltage<sup>[2]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... 2001V  
(per MIL-STD-883, Method 3015)

Latch Up Current ..... >200 mA

## Operating Range

| Range      | Ambient Temperature <sup>[3]</sup> | $V_{CC}$       |
|------------|------------------------------------|----------------|
| Commercial | 0°C to 70°C                        | 5.0V $\pm$ 10% |

## DC Electrical Characteristics<sup>[2]</sup>

| Parameter | Description                                 | Condition                                                                                                                      | 12 and 15 ns |                | 25 ns |                | Unit          |
|-----------|---------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------|--------------|----------------|-------|----------------|---------------|
|           |                                             |                                                                                                                                | Min          | Max            | Min   | Max            |               |
| $V_{IH}$  | Input HIGH Voltage                          |                                                                                                                                | 2.2          | $V_{CC} + 0.3$ | 2.2   | $V_{CC} + 0.3$ | V             |
| $V_{IL}$  | Input LOW Voltage                           |                                                                                                                                | -0.3         | 0.8            | -0.3  | 0.8            | V             |
| $V_{OH}$  | Output HIGH Voltage                         | $V_{CC} = \text{Min}$ , $I_{OH} = -4.0 \text{ mA}$                                                                             | 2.4          | —              | 2.4   | —              | V             |
| $V_{OL}$  | Output LOW Voltage                          | $V_{CC} = \text{Min}$ , $I_{OL} = 8.0 \text{ mA}$                                                                              | —            | 0.4            | —     | 0.4            | V             |
| $I_{OZ}$  | Output Leakage Current                      | $GND \leq V_i \leq V_{CC}$ , Output Disabled                                                                                   | -5           | +5             | -5    | +5             | $\mu\text{A}$ |
| $I_{IX}$  | Input Leakage Current                       | $GND \leq V_i \leq V_{CC}$                                                                                                     | -5           | +5             | -5    | +5             | $\mu\text{A}$ |
| $I_{CC}$  | $V_{CC}$ Operating Supply Current           | $V_{CC} = \text{Max}$ , $I_{OUT} = 0 \text{ mA}$ ,<br>$f = F_{MAX} = 1/t_{RC}$                                                 | —            | 150            | —     | 95             | mA            |
| $I_{SB1}$ | Automatic CE Power Down Current TTL Inputs  | $V_{CC} = \text{Max}$ ,<br>$\overline{CE} \geq V_{IH}$ , $V_{IN} \geq V_{IH}$ or<br>$V_{IN} \leq V_{IL}$ , $f = F_{MAX}$       | —            | 30             | —     | 30             | mA            |
| $I_{SB2}$ | Automatic CE Power Down Current CMOS Inputs | $V_{CC} = \text{Max}$ ,<br>$\overline{CE} \geq V_{CC} - 0.3V$ ,<br>$V_{IN} \geq V_{CC} - 0.3V$ or<br>$V_{IN} < 0.3V$ , $f = 0$ | —            | 10             | —     | 10             | mA            |

## Capacitance<sup>[4]</sup>

| Parameter | Description        | Conditions                                                          | Max (ALL – PACKAGES) | Unit |
|-----------|--------------------|---------------------------------------------------------------------|----------------------|------|
| $C_{IN}$  | Input Capacitance  | $T_A = 25^\circ\text{C}$ , $f = 1 \text{ MHz}$ ,<br>$V_{CC} = 5.0V$ | 8                    | pF   |
| $C_{OUT}$ | Output Capacitance |                                                                     | 10                   |      |

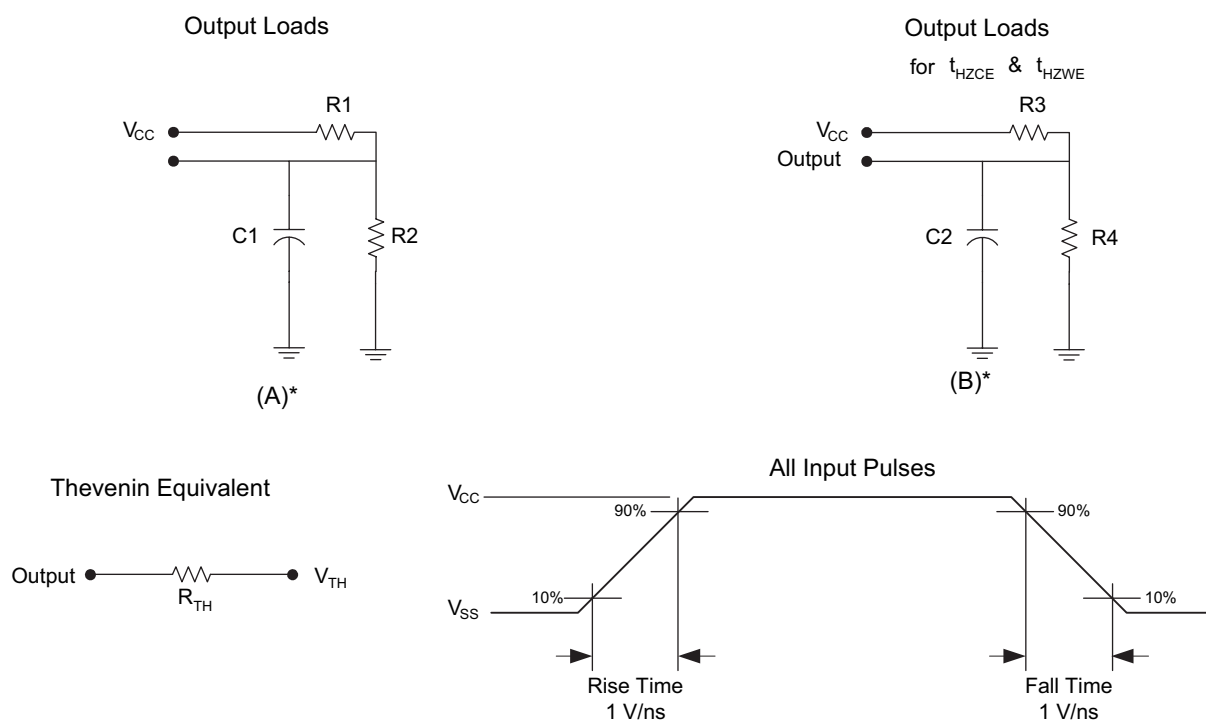
## Thermal Resistance<sup>[4]</sup>

| Parameter     | Description                              | Conditions                                                                      | 24 DIP | 24 SOJ | Unit               |
|---------------|------------------------------------------|---------------------------------------------------------------------------------|--------|--------|--------------------|
| $\theta_{JA}$ | Thermal Resistance (Junction to Ambient) | Still Air, soldered on a 3 x 4.5 square inches, two-layer printed circuit board | 75.69  | 84.15  | $^\circ\text{C/W}$ |
| $\theta_{JC}$ | Thermal Resistance (Junction to Case)    |                                                                                 | 33.80  | 37.56  |                    |

### Notes

- $V_{IL}(\text{min}) = -2.0V$  for pulse durations of less than 20 ns.
- $T_A$  is the "instant on" case temperature
- Tested initially and after any design or process change that may affect these parameters

## AC Test Loads<sup>[5]</sup>



\* including scope and jig capacitance

## AC Test Conditions

| Parameter | Description       | Nom. | Unit     |
|-----------|-------------------|------|----------|
| C1        | Capacitor 1       | 30   | pF       |
| C2        | Capacitor 2       | 5    |          |
| R1        | Resistor 1        | 480  | $\Omega$ |
| R2        | Resistor 2        | 255  |          |
| R3        | Resistor 3        | 480  |          |
| R4        | Resistor 4        | 255  |          |
| $R_{TH}$  | Resistor Thevenin | 167  | V        |
| $V_{TH}$  | Voltage Thevenin  | 1.73 |          |

### Note

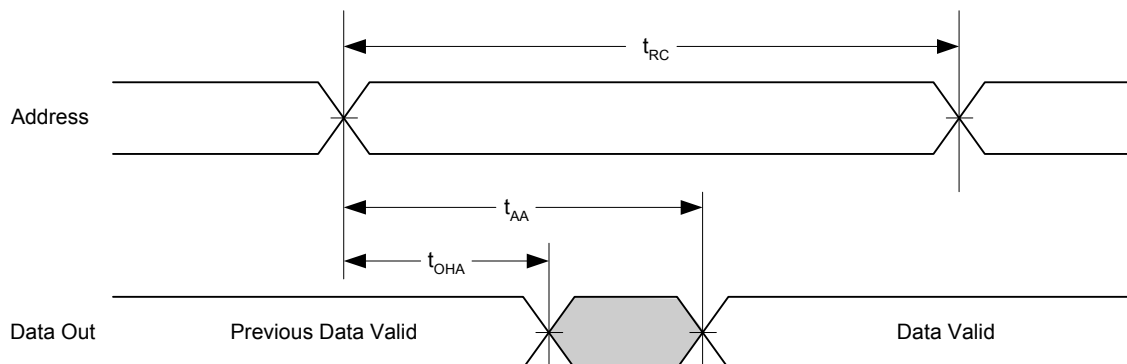
5. Test Conditions assume a transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V

## AC Electrical Characteristics<sup>[4, 6, 7, 8]</sup>

| Parameter  | Description                   | 12 ns |     | 15 ns |     | 25 ns |     | Unit |
|------------|-------------------------------|-------|-----|-------|-----|-------|-----|------|
|            |                               | Min   | Max | Min   | Max | Min   | Max |      |
| $t_{RC}$   | Read Cycle Time               | 12    | –   | 15    | –   | 25    | –   | ns   |
| $t_{AA}$   | Address to Data Valid         | –     | 12  | –     | 15  | –     | 25  | ns   |
| $t_{OHA}$  | Data Hold from Address Change | 3     | –   | 3     | –   | 3     | –   | ns   |
| $t_{ACE}$  | $\overline{CE}$ to Data Valid | –     | 12  | –     | 15  | –     | 25  | ns   |
| $t_{LZCE}$ | $\overline{CE}$ to Low Z      | 3     | –   | 3     | –   | 3     | –   | ns   |
| $t_{HZCE}$ | $\overline{CE}$ to High Z     | –     | 5   | –     | 5   | –     | 11  | ns   |
| $t_{PU}$   | $\overline{CE}$ to Power-up   | 0     | –   | 0     | –   | 0     | –   | ns   |
| $t_{PD}$   | $\overline{CE}$ to Power-down | –     | 12  | –     | 15  | –     | 20  | ns   |
| $t_{WC}$   | Write Cycle Time              | 12    | –   | 15    | –   | 25    | –   | ns   |
| $t_{SCE}$  | $\overline{CE}$ to Write End  | 9     | –   | 9     | –   | 20    | –   | ns   |
| $t_{AW}$   | Address Set-up to Write End   | 9     | –   | 10    | –   | 20    | –   | ns   |
| $t_{HA}$   | Address Hold from Write End   | 0     | –   | 0     | –   | 0     | –   | ns   |
| $t_{SA}$   | Address Set-up to Write Start | 0     | –   | 0     | –   | 0     | –   | ns   |
| $t_{PWE}$  | $\overline{WE}$ Pulse Width   | 8     | –   | 9     | –   | 20    | –   | ns   |
| $t_{SD}$   | Data Set-Up to Write End      | 8     | –   | 9     | –   | 15    | –   | ns   |
| $t_{HD}$   | Data Hold from Write End      | 0     | –   | 0     | –   | 0     | –   | ns   |
| $t_{HZWE}$ | $\overline{WE}$ LOW to High Z | –     | 7   | –     | 7   | –     | 11  | ns   |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to Low Z | 2     | –   | 2     | –   | 3     | –   | ns   |

## Timing Waveforms

### Read Cycle No. 1<sup>[9, 10]</sup>

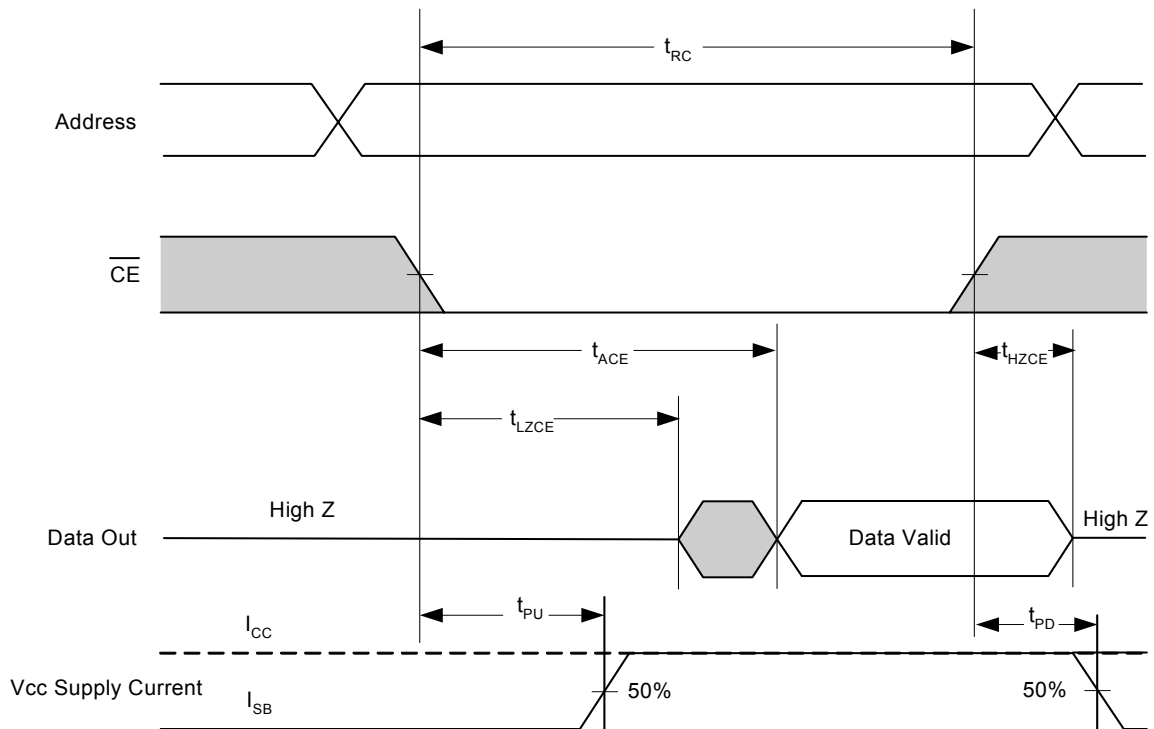


### Notes

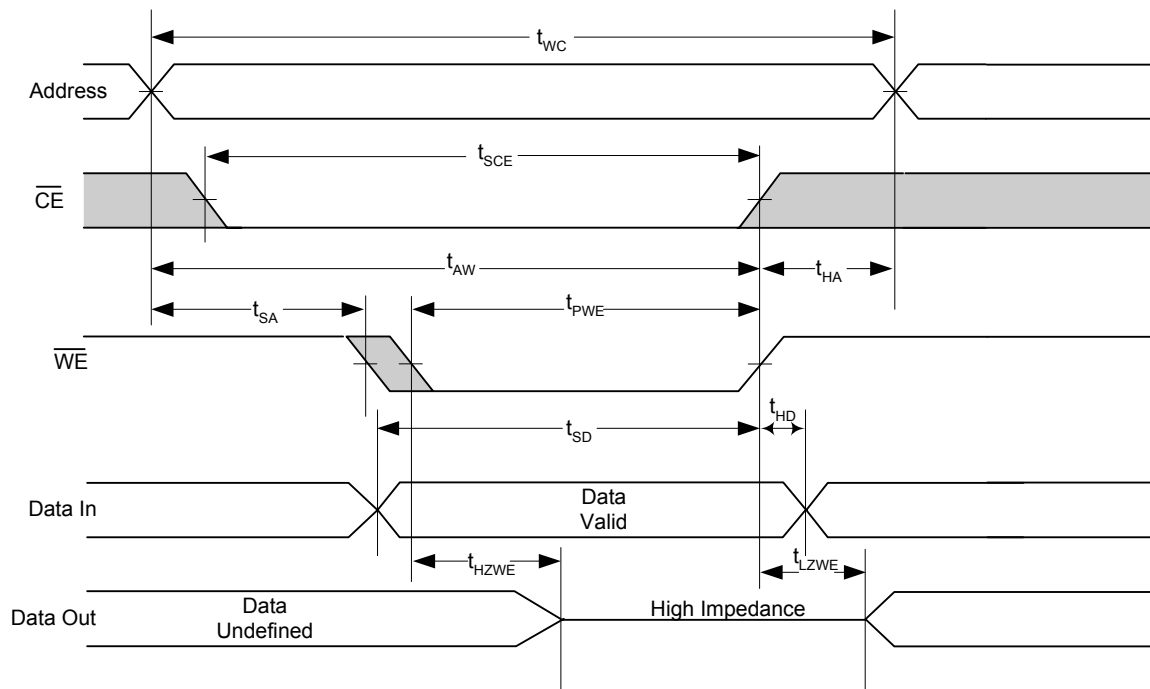
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- The internal Write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW.  $\overline{CE}$  and  $\overline{WE}$  must be LOW to initiate a write, and the transition of any of these signals can terminate the Write. The input data setup and hold timing should be referenced to the leading edge of the signal that terminates the write.
- $t_{HZCE}$ ,  $t_{HZWE}$  are specified as in part (b) of the "AC Test Loads<sup>[5]</sup>" on page 4. Transitions are measured  $\pm 200$  mV from steady state voltage.
- Device is continuously selected.  $\overline{CE} = V_{IL}$ .
- $\overline{WE}$  is HIGH for Read Cycle.

## Timing Waveforms (continued)

### Read Cycle No. 2<sup>[4, 11, 12]</sup>



### Write Cycle No. 1 ( $\overline{\text{WE}}$ Controlled)<sup>[4, 13]</sup>

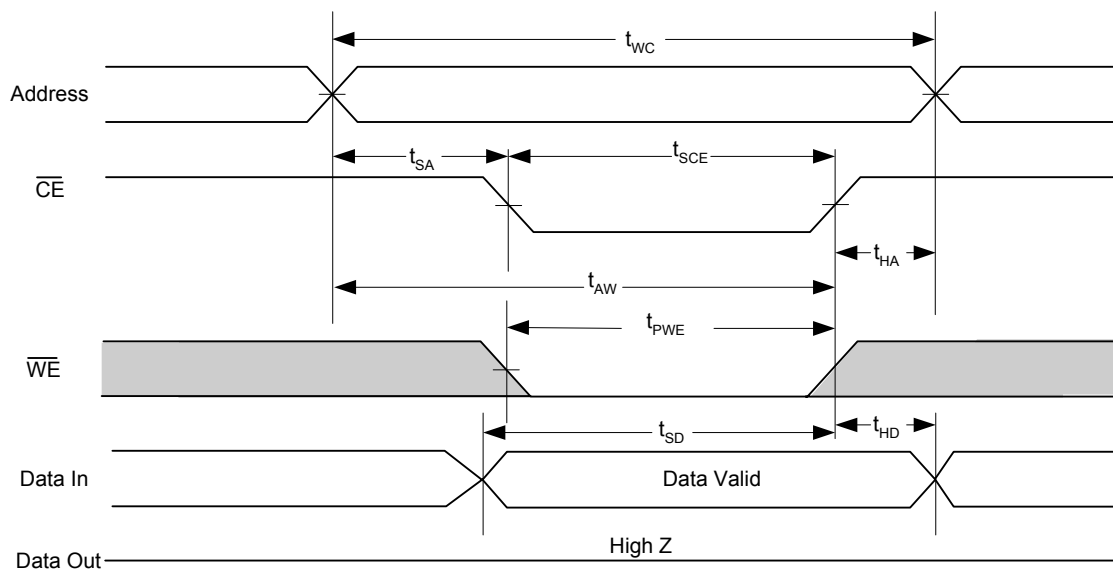


#### Notes

11.  $\overline{\text{WE}}$  is HIGH in read cycle.
12. Address valid prior to or coincident with  $\overline{\text{CE}}$  transition LOW.
13. The minimum write cycle time is the sum of  $t_{\text{HZWE}}$  and  $t_{\text{SD}}$ .

## Timing Waveforms (continued)

### Write Cycle No. 2 ( $\overline{\text{CE}}$ Controlled)<sup>[14, 15]</sup>



## Truth Table

| $\overline{\text{CE}}$ | $\overline{\text{WE}}$ | I/Ox     | Mode                | Power                |
|------------------------|------------------------|----------|---------------------|----------------------|
| H                      | X                      | High Z   | Deselect/Power-Down | Standby ( $I_{SB}$ ) |
| L                      | H                      | Data Out | Read                | Active ( $I_{CC}$ )  |
| L                      | L                      | Data In  | Write               | Active ( $I_{CC}$ )  |

## Ordering Information

| Speed (ns) | Ordering Code  | Package Diagram | Package Type                      | Operating Range |
|------------|----------------|-----------------|-----------------------------------|-----------------|
| 12         | CY7C197BN-12VC | 51-85030        | 24-lead SOJ (8 x 15 x 3.5 mm)     | Commercial      |
| 15         | CY7C197BN-15VC | 51-85030        | 24-lead SOJ (8 x 15 x 3.5 mm)     | Commercial      |
| 25         | CY7C197BN-25PC | 51-85013        | 24-lead DIP (6.6 x 31.8 x 3.5 mm) | Commercial      |

Please contact local sales representative regarding availability of these parts.

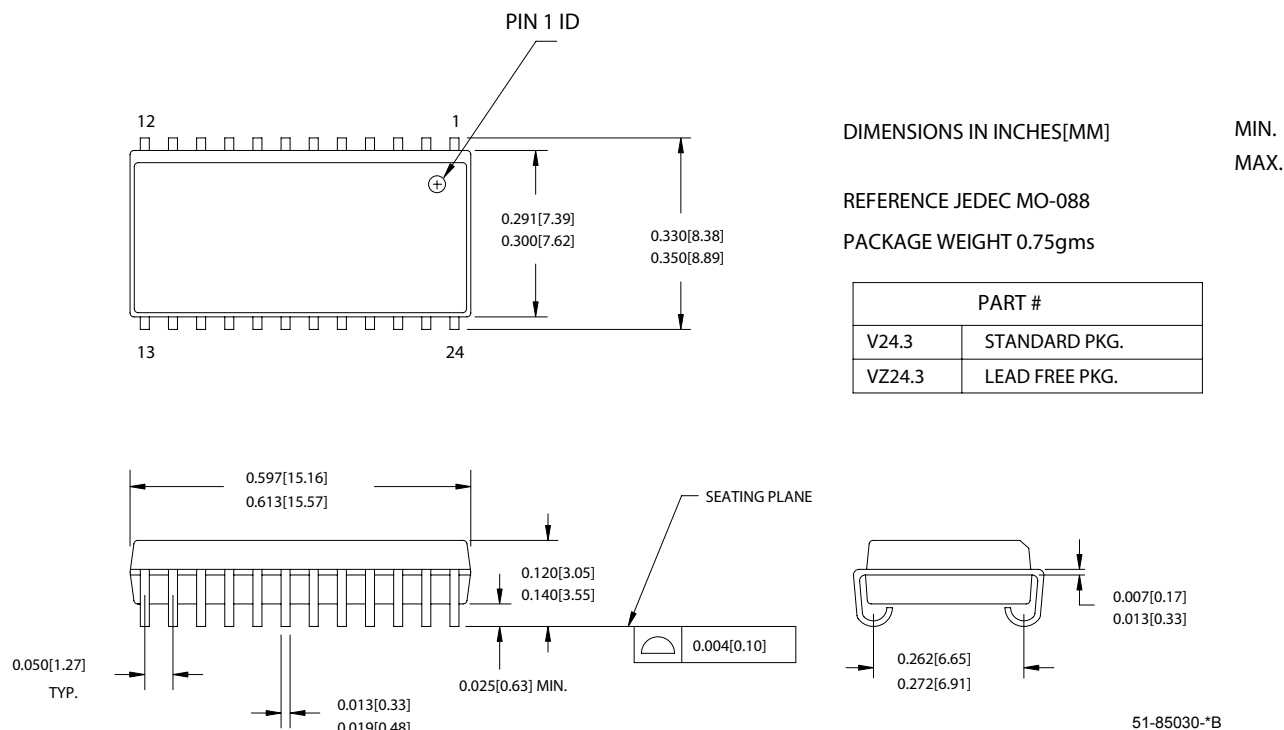
### Notes

14. This cycle is  $\overline{\text{CE}}$  controlled.

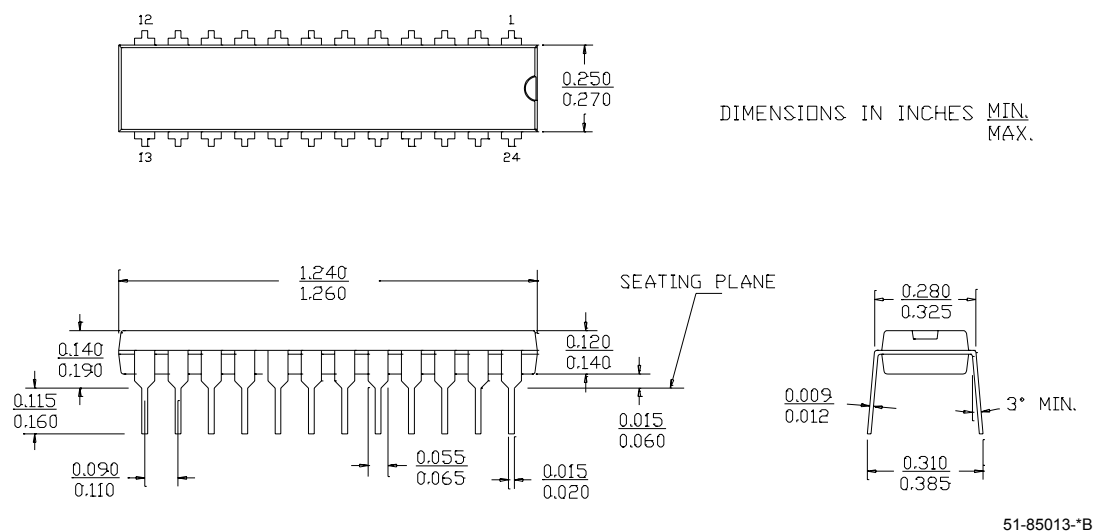
15. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high impedance state.

## Package Diagrams

**Figure 1. 24-lead (300-mil) SOJ (51-85030)**



**Figure 2. 24-lead DIP (6.6 x 31.8 x 3.5 mm) (51-85013)**



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## Document History Page

| Document Title: CY7C197BN 256 Kb (256K x 1) Static RAM<br>Document Number: 001-06447 |         |            |                 |                       |
|--------------------------------------------------------------------------------------|---------|------------|-----------------|-----------------------|
| REV.                                                                                 | ECN No. | Issue Date | Orig. of Change | Description of Change |
| **                                                                                   | 901742  | See ECN    | NXR             | New Data Sheet        |