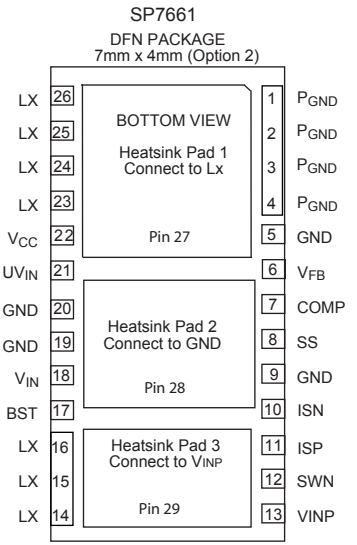
SP7661

Wide Input Voltage Range 3A, 600kHz, Buck Regulator

PowerBlox™

FEATURES

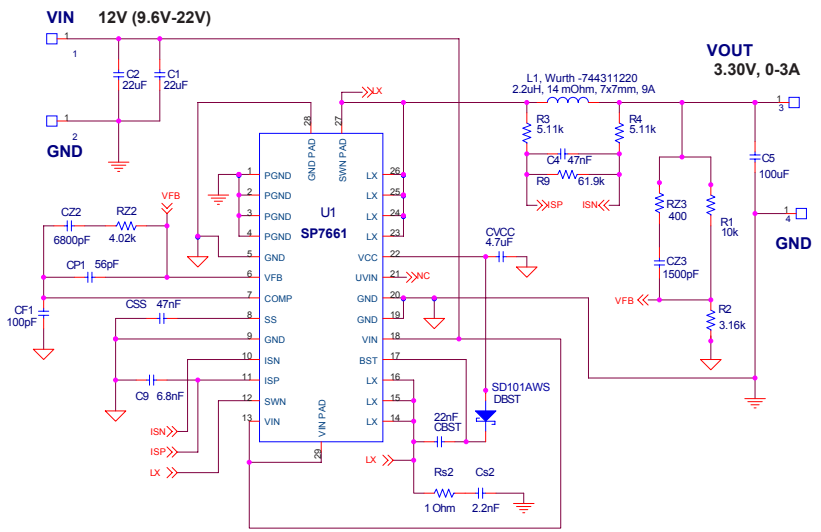
- 4.75V to 22V Input Voltage Range using Single Supply
- 3V to 22V Input Voltage Range using Dual Supply
- ±1% 0.8V Reference
- 3A Output Capability
- Current Limiting using Inductor DCR
- Built in Low $R_{DS(ON)}$ Power Switches
- 600kHz Fixed Frequency Operation
- Over Temperature Protection
- Short Circuit Protection with Auto-Restart
- Wide BW Amp Allows Type II or III Compensation
- Programmable Soft Start
- Fast Transient Response
- High Efficiency: Greater than **93%** Possible
- Nonsynchronous Start-Up into a Pre-Charged Output
- Available in RoHS Compliant, Lead Free Packaging: Small 7mm x 4mm DFN
- U.S. Patent #6,922,041



DESCRIPTION

The SP7661 is a synchronous step-down switching regulator optimized for high efficiency. The part is designed for use with a single 4.75V to 22V single supply or 3V to 22V input if an external Vcc is provided. The SP7661 provides a fully integrated buck regulator solution using a fixed 600kHz frequency, PWM voltage mode architecture. Protection features include UVLO, thermal shutdown, output current limit and short circuit protection. The SP7661 is available in the space saving DFN package.

TYPICAL APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{CC} 7V
V_{IN} 25V
BST..... 30V
LX-BST..... -0.3V to 7V
LX..... -1V to 30V
All other pins..... -0.3V to V_{CC} + 0.3V

Storage Temperature..... -65°C to 150°C
Power Dissipation..... Internally Limited via OTP
Lead Temperature (Soldering, 10 sec)..... 300°C
ESD Rating..... 2kV HBM
Thermal Resistance θ_{JC} ..... 5°C/W

ELECTRICAL SPECIFICATIONS

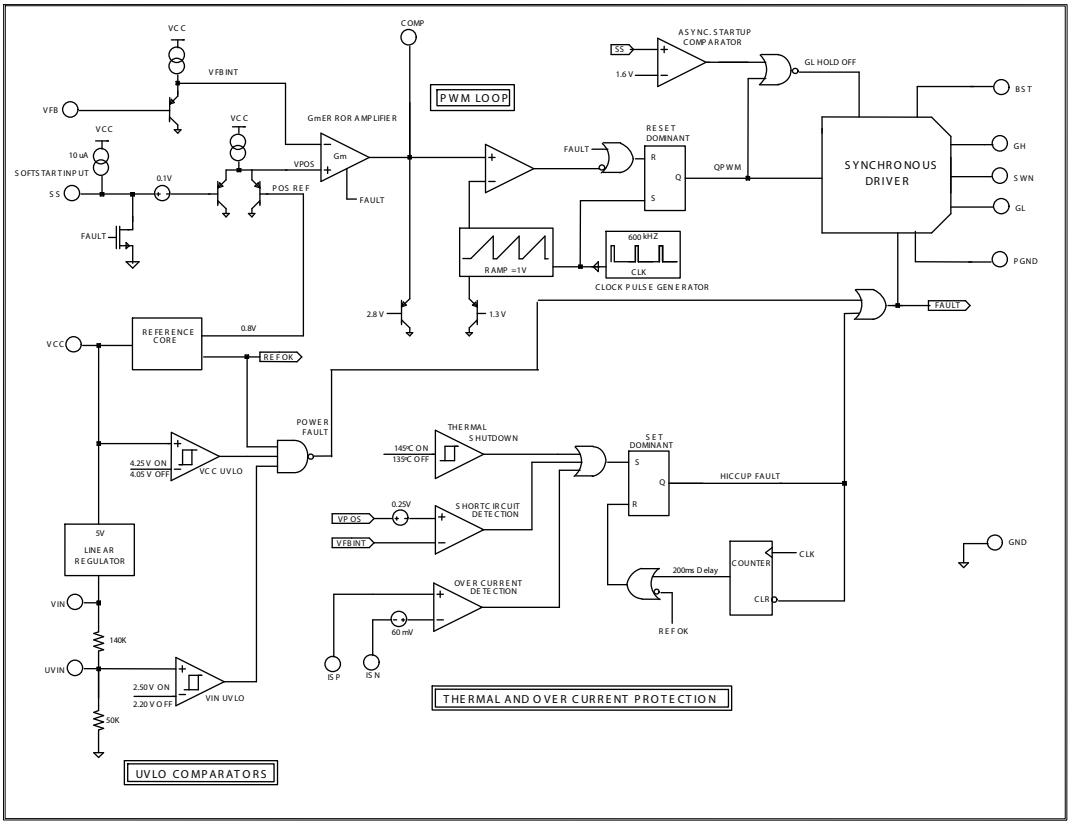
Specifications are for T_{AMB} = T_J = 25°C, and those denoted by ♦ apply over the full operating range, -40°C< Tj< 125°C. Unless otherwise specified: 4.5V < Vcc < 5.5V, 3V < V_{IN} < 22V, BST = LX + 5V, UVIN = 3V, CVCC = 1µF, C_{COMP} = 0.1µF, Css = 50nF.

PARAMETER	MIN	TYP	MAX	UNITS	♦	CONDITIONS
QUIESCENT CURRENT						
V_{IN} Supply Current (No switching)		1.5	3.0	mA	♦	V_{FB}= 0.9V
V_{IN} Supply Current (switching)		8	14	mA		
BST Supply Current (No switching)		0.2	0.4	mA	♦	V_{FB}= 0.9V
BST Supply Current (switching)		3	6	mA		
PROTECTION: UVLO						
Vcc UVLO Start Threshold	4.00	4.25	4.50	V	♦	
Vcc UVLO Hysteresis	100	200	300	mV	♦	
UVIN Start Threshold	2.30	2.50	2.65	V	♦	
UVIN Hysteresis	200	300	400	mV	♦	
UVIN Input Current			1.0	µA	♦	UVIN=3.0V
ERROR AMPLIFIER REFERENCE						
Error Amplifier Reference	0.792	0.800	0.808	V		2X Gain Config., Measure V_{FB}; Vcc=5V
Error Amplifier Reference Over Line	0.784	0.800	0.816	V	♦	
COMP Sink Current	70	150	230	µA	♦	V_{FB}=0.9V, COMP=0.9V
COMP Source Current	-230	-150	-70	µA	♦	V_{FB}=0.9V, COMP=0.9V
V_{FB} Input Bias Current		50	200	nA	♦	V_{FB}=0.8V
COMP Clamp	3.2	3.5	3.8	V		V_{FB}=0.7V, T_A=25°C
COMP Clamp Temp. Coefficient		-2.0		mV/°C		
VCC LINEAR REGULATOR						
VCC Output Voltage	4.7	5.0	5.3	V	♦	V_{IN} = 6 to 23V, I_{LOAD} = 0mA to 30mA
	4.51	4.73			♦	V_{IN} = 5V, 20mA
Dropout Voltage	250	500	750	mV	♦	Vin-Vout = Dropout voltage when Vcc regulated drops by 2%. IVCC = 30 mA.

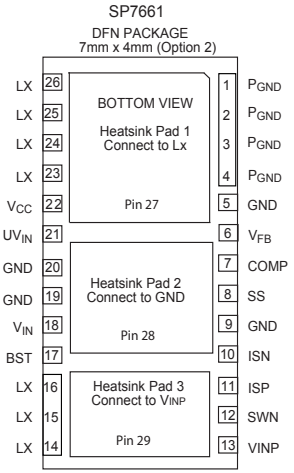
ELECTRICAL SPECIFICATIONS

Specifications are for T_{AMB} = T_J = 25°C, and those denoted by ♦ apply over the full operating range, -40°C< Tj< 125°C. Unless otherwise specified: 4.5V < Vcc < 5.5V, 3V < V_{IN} < 22V, BST = LX + 5V, UVIN = 3V, CVCC = 1µF, C_{COMP} = 0.1µF, Css = 50nF.

PARAMETER	MIN	TYP	MAX	UNITS	♦	CONDITIONS
CONTROL LOOP: PWM COMPARATOR, RAMP & LOOP DELAY PATH						
Ramp Amplitude	0.80	1.00	1.20	V	♦	
RAMP Offset	1.7	2.0	2.3	V	♦	
Ramp offset Temperature Coefficient		-2		mV/°C		
GH Minimum Pulse Width		150	180	ns	♦	
Maximum Controllable Duty Ratio	92	97		%	♦	
Maximum Duty Ratio	100			%	♦	Valid for 20 cycles
Internal Oscillator Ratio	510	600	690	kHz	♦	
TIMERS: SOFTSTART						
SS Charge Current:	-16	-10	-4.0	µA	♦	
SS Discharge Current:	1.0	2.0	3.0	mA	♦	Fault Present, SS=0.2V
PROTECTION: SHORT CIRCUIT, OVERCURRENT & THERMAL						
Short Circuit Threshold Voltage	0.2	0.25	0.3	V	♦	
Hiccup Timeout	90	110	130	ms	♦	V_{FB}=0.5V
Overcurrent Threshold Voltage	54	60	66	mV		Measured ISP - ISN
ISP, ISN Common Mode Range	0		3.6	V		
Thermal Shutdown Temperature	135	145	155	°C		Guaranteed by design
Thermal Recovery Temperature		135		°C		
Thermal Hysteresis		10		°C		
OUTPUT: POWER STAGE						
High Side Switch R_{DSON}		35	75	mΩ		V_{GS}=4.5V; I_{DRAIN}=4.1A; T_{AMB}=25°C
Synchronous Low Side Switch R_{DSON}		35	75	mΩ		V_{GS}=4.5V; I_{DRAIN}=4.1A; T_{AMB}=25°C
Maximum Output Current	3			A	♦	



Note: The SP7661 uses the Sipex PWM controller SP6136



Pin #	Pin Name	Description
1-4	PGND	Ground connection for the synchronous rectifier.
5, 9, 19, 20	GND	Ground Pin. The control circuitry of the IC and lower power driver are referenced to this pin. Return separately from other ground traces to the (-) terminal of C_{OUT}.
6	VFB	Feedback Voltage and Short Circuit Detection pin. It is the inverting input of the Error Amplifier and serves as the output voltage feedback point for the Buck Converter. The output voltage is sensed and can be adjusted through an external resistor divider. Whenever VFB drops 0.25V below the positive reference, a short circuit fault is detected and the IC enters hiccup mode.
7	COMP	Output of the Error Amplifier. It is internally connected to the inverting input of the PWM comparator. An optimal filter combination is chosen and connected to this pin and either ground or VFB to stabilize the voltage mode loop.
8	SS	Soft Start. Connect an external capacitor between SS and GND to set the soft start rate based on the 10µA source current. The SS pin is held low via a 1mA (min) current during all fault conditions.
10	ISN	Current sense negative input. Rail-to-rail input for overcurrent detection.
11	ISP	Current sense positive input. Rail-to-rail input for overcurrent detection.
12	SWN	Lower supply rail for the GH high-side gate driver. Connect this pin to the switching node as close as possible to pins 23- 27. Do not connect this pin to pins 14 – 16.
13	VINP	Input connection to the high side N-channel MOSFET.
14-16, 23-26	LX	Connect an inductor between this pin and V_{OUT}.
17	BST	High side driver supply pin. Connect BST to the external boost diode and capacitor as shown in the Typical Application Circuit on page 1. The high side driver is connected between BST pin and SWN pin.
18	VIN	V_{IN} connection for internal LDO and PWM Controller.
21	UVIN	UVLO input for V_{IN} voltage. Connect a resistor divider between V_{IN} and UVIN to set minimum operating voltage. Use resistor values below 20kΩ to override internal resistor divider.
22	VCC	Output of internal regulator. May be exterinally biased if Vin < 5V.

General Overview

The SP7661 is a fixed frequency, voltage mode, synchronous PWM regulator optimized for high efficiency. The part has been specifically designed for single supply operation from a 5V to 22V input.

The heart of the SP7661 is a wide bandwidth transconductance amplifier designed to accommodate Type II and Type III compensation schemes. A precision 0.8V reference, present on the positive terminal of the error amplifier, permits the programming of the output voltage down to 0.8V via the VFB pin. The output of the error amplifier, COMP, is compared to a 1.1V peak-to-peak ramp, which is responsible for trailing edge PWM control. This voltage ramp and PWM control logic are governed by the internal oscillator that accurately sets the PWM frequency to 600kHz.

The SP7661 contains two unique control features that are very powerful in distributed applications. First, nonsynchronous driver control is enabled during startup, to prohibit the low side switch from pulling down the output until the high side switch has attempted to turn on. Second, a 100% duty cycle timeout ensures that the low side switch is periodically enhanced during extended periods at 100% duty cycle. This guarantees the synchronized refreshing of the BST capacitor during very large duty ratios.

The SP7661 also contains a number of valuable protection features. Programmable V_{IN} UVLO allows the user to set the exact value at which the conversion voltage can safely begin down-conversion, and an internal V_{CC} UVLO which ensures that the controller itself has enough voltage to properly operate. Other protection features include thermal shutdown and short-circuit detection. In the event that either a thermal, short-circuit, or UVLO fault is detected, the SP7661 is forced into an idle state where the output drivers are held off for a finite period before a restart is attempted.

Soft Start

"Soft Start" is achieved when a power converter ramps up the output voltage while controlling the magnitude of the input supply source current. In a modern step down converter, ramping up the positive terminal of the error amplifier controls soft start. As a result, excess source current can be defined as the current required to charge the output capacitor.

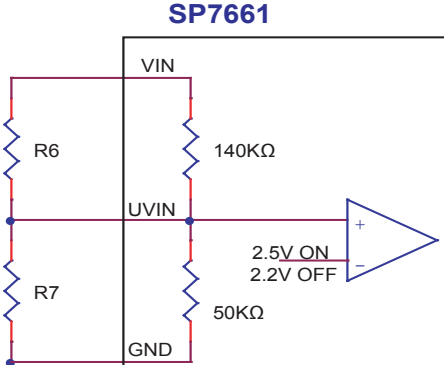
$$I_{VIN} = C_{OUT} \bullet (\Delta V_{OUT} / \Delta T_{SOFT\text{-}START})$$

The SP7661 provides the user with the option to program the soft start rate by tying a capacitor from the SS pin to GND. The selection of this capacitor is based on the 10µA pull up current present at the SS pin and the 0.8V reference voltage. Therefore, the excess source can be redefined as:

$$I_{VIN} = C_{OUT} \bullet [\Delta V_{OUT} \bullet 10\mu A / (C_{SS} \bullet 0.8V)]$$

Under Voltage Lock Out (UVLO)

The SP7661 has two separate UVLO comparators to monitor the bias (Vcc) and Input (V_{IN}) voltages independently. The Vcc UVLO is internally set to 4.25V. The V_{IN} UVLO is programmable through UVIN pin. When UVIN pin is greater than 2.5V the SP7661 is permitted to start up pending the removal of all other faults. A pair of internal resistors is connected to UVIN as shown in the figure below.



Internal and external bias of UVIN

Therefore without external biasing the VIN start threshold is 9.5V. A small capacitor may be required between UVIN and GND to filter out noise. For applications with VIN of 5V or 3.3V, connect UVIN directly to VIN. To program the VIN start threshold, use a pair of external resistors as shown. If external resistors are an order of magnitude smaller than internal resistors, then the VIN start threshold is given by:

$$V_{IN}(start) = 2.5 \bullet (R6+R7)/R7$$

For example, if it is required to have a VIN start threshold of 7V, then let R7 = 5KΩ and using the VIN start threshold equation we get R6 = 9.09KΩ.

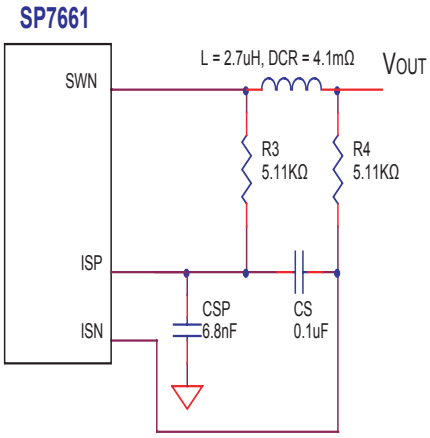
Thermal and Short-Circuit Protection

Because the SP7661 is designed to drive large output current, there is a chance that the power converter will become too hot. Therefore, an internal thermal shutdown (145°C) has been included to prevent the IC from malfunctioning at extreme temperatures.

A short-circuit detection comparator has also been included in the SP7661 to protect against an accidental short at the output of the power converter. This comparator constantly monitors the positive and negative terminals of the error amplifier, and if the VFB pin falls more than 250mV (typical) below the positive reference, a short-circuit fault is set. Because the SS pin overrides the internal 0.8V reference during soft start, the SP7661 is capable of detecting short-circuit faults throughout the duration of soft start as well as in regular operation.

Over-Current Protection

The Over-current protection feature can only be used on output voltages ≤ 3.3 volts. It is limited by the common mode rating of the op-amp used to sense the voltage across the inductor. Over-current is detected by monitoring a differential voltage across the output inductor as shown in the next figure.



Over-current detection circuit

Inputs to an over-current detection comparator, set to trigger at 60 mV nominal, are connected to the inductor as shown. Since the average voltage sensed by the comparator is equal to the product of inductor current and inductor DC resistance (DCR), then IMAX = 60mV / DCR. Solving this equation for the specific inductor in circuit 1, IMAX = 14.6A. When IMAX is reached, a 220 ms time-out is initiated, during which top and bottom drivers are turned off. Following the time-out, a restart is attempted. If the fault condition persists, then the time-out is repeated (referred to as hiccup).

Increasing the Current Limit

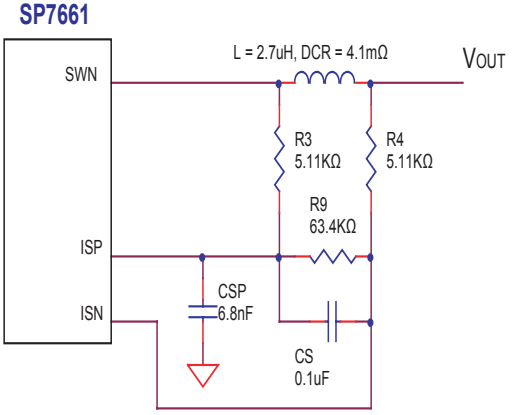
If it is desired to set IMAX > {60mV / DCR} (in this case larger than 14.6A), then a resistor R9 should be added as shown in the next figure. R9 forms a resistor divider and reduces the voltage seen by the comparator.

$$\text{Since: } \frac{60mV}{R9} = \frac{(I_{MAX} \bullet DCR)}{\{R3 + R4 + R9\}}$$

Solving for R9 we get:

$$R9 = \frac{[60mV \bullet (R3 + R4)]}{[(I_{MAX} \bullet DCR) - 60mV]}$$

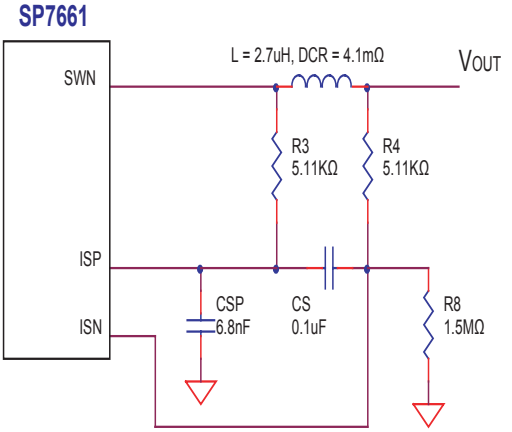
As an example: if desired I_{MAX} is 17A, then R9 = 63.4KΩ.



Over-current detection circuit for Imax > 60mV / DCR

$$R8 = R4 \bullet \frac{[V_{OUT} - 60mV + (I_{MAX} \bullet DCR)]}{60mV - (I_{MAX} \bullet DCR)}$$

As an example: for I_{MAX} of 4A and V_{OUT} of 3.3V, calculated R8 is 381kΩ.



Over-current detection circuit for I_{MAX} < {60mV / DCR}

Decreasing the Current Limit

If it is required to set I_{MAX} < {60mV / DCR, a resistor is added as shown in the following figure. R8 increases the net voltage detected by the current-sense comparator. Voltage at the positive and negative terminal of comparator is given by:

$VSP = V_{OUT} + (I_{MAX} \bullet DCR)$

$VSN = V_{OUT} \bullet \{R8 / (R4 + R8)\}$

Since the comparator is triggered at 60mV:
VSP-VSN = 60 mV

Combining the above equations and solving for R8:

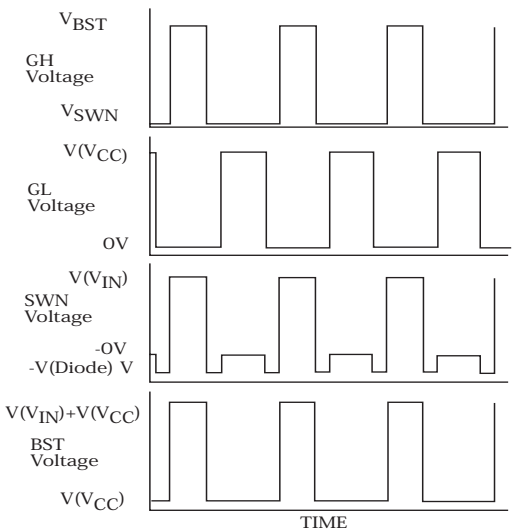
Handling of Faults

Upon the detection of power (UVLO), thermal, or short-circuit faults, the SP7661 is forced into an idle state where the SS and COMP pins are pulled low and both switches are held off. In the event of UVLO fault, the SP7661 remains in this idle state until the UVLO fault is removed. Upon the detection of a thermal or short-circuit fault, an internal 100ms timer is activated. In the event of a short-circuit fault, a restart is attempted immediately after the 100ms timeout expires. Whereas, when a thermal fault is detected the 100ms delay continuously recycles and a restart cannot be attempted until the thermal fault is removed and the timer expires.

Error Amplifier and Voltage Loop

The heart of the SP7661 voltage error loop is a high performance, wide bandwidth transconductance amplifier. Because of the amplifier's current limited (+/-150µA) transconductance, there are many ways to compensate the voltage loop or to control the COMP pin externally. If a simple, single-pole, single-zero response is desired, then compensation can be as simple as an RC circuit to Ground. If a more complex compensation is required, then the amplifier has enough bandwidth (45° at 4 MHz), and enough gain (60dB) to run Type III compensation schemes with adequate gain and phase margins at crossover frequencies greater than 50kHz.

The common mode output of the error amplifier is 0.9V to 2.2V. Therefore, the PWM voltage ramp has been set between 1.1V and 2.2V to ensure proper 0% to 100% duty cycle capability. The voltage loop also includes two other very important features. One is a nonsynchronous startup mode. Basically, the synchronous rectifier cannot turn on unless the high side switch has attempted to turn on or the SS pin has exceeded 1.7V. This feature prevents the controller from "dragging down" the output voltage during startup or in fault modes.



The second feature is a 100% duty cycle timeout that ensures synchronized refreshing of the BST capacitor at very high duty ratios. In the event that the high side NFET is on for 20 continuous clock cycles, a reset is given to the PWM flip flop half way through the 21st cycle. This forces GL to rise for the cycle, in turn refreshing the BST capacitor. The boost capacitor is used to generate a high voltage drive supply for the high side switch, which is Vcc above V_{IN}.

Power MOSFETs

The SP7661 contains a pair of integrated low resistance N-channel switches designed to drive up to 3A of output current. Care should be taken to de-rate the output current based on the thermal conditions in the system such as ambient temperature, airflow and heat sinking. Maximum output current could be limited by thermal limitations of a particular application by taking advantage of the integrated-over-temperature protective scheme employed in the SP7661. The SP7661 incorporates a built-in overtemperature protection to prevent internal overheating.

Setting Output Voltages

The SP7661 can be set to different output voltages. The relationship in the following formula is based on a voltage divider from the output to the feedback pin V_{FB}, which is set to an internal reference voltage of 0.80V. Standard 1% metal film resistors of surface mount size 0603 are recommended.

$$V_{OUT} = 0.80V \left[R1 / R2 + 1 \right] \Rightarrow$$

$$R2 = R1 / \left[\left(V_{OUT} / 0.80V \right) - 1 \right]$$

Where R1 = 10KΩ and for V_{OUT} = 0.80V setting, simply remove R2 from the board. Furthermore, one could select the value of the R1 and R2 combination to meet the exact output voltage setting by restricting the R1 resistance range such that 10KΩ < R1 < 100KΩ for overall system loop stability.

Inductor Selection

There are many factors to consider in selecting the inductor including core material, inductance vs. frequency, current handling capability, efficiency, size and EMI. In a typical SP7661 circuit, the inductor is chosen primarily for value, saturation current and DC resistance. Increasing the inductor value will decrease output voltage ripple, but degrade transient response. Low inductor values provide the smallest size, but cause large ripple currents, poor efficiency and require more output capacitance to smooth out the larger ripple current. The inductor must be able to handle the peak current at the switching frequency without saturating, and the copper resistance in the winding should be kept as low as possible to minimize resistive power loss. A good compromise between size, loss and cost is to set the inductor ripple current to be within 20% to 40% of the maximum output current.

The switching frequency and the inductor operating point determine the inductor value as follows:

$$L = \frac{V_{OUT} \bullet (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \bullet f_S \bullet K_R \bullet I_{OUT(MAX)}}$$

where:

f_S = switching frequency

K_R = ratio of the AC inductor ripple current to the maximum output current

The peak-to-peak inductor ripple current is:

$$I_{PP} = \frac{V_{OUT} \bullet (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \bullet f_S \bullet L}$$

Once the required inductor value is selected, the proper selection of core material is based on peak inductor current and efficiency requirements. The core must be large enough not to saturate at the peak inductor current

$$I_{PEAK} = I_{OUT(MAX)} + \frac{I_{PP}}{2}$$

and provide low core loss at the high switching frequency. Low cost powdered-iron cores have a gradual saturation characteristic but can introduce considerable AC core loss, especially when the inductor value is relatively low and the ripple current is high. Ferrite materials, although more expensive, have an abrupt saturation characteristic with the inductance dropping sharply when the peak design current is exceeded. Nevertheless, they are preferred at high switching frequencies because they present very low core loss while the designer is only required to prevent saturation. In general, ferrite or molypermalloy materials are a better choice for all but the most cost sensitive applications.

Optimizing Efficiency

The power dissipated in the inductor is equal to the sum of the core and copper losses. To minimize copper losses, the winding resistance needs to be minimized, but this usually comes at the expense of a larger inductor. Core losses have a more significant contribution at low output current where the copper losses are at a minimum, and can typically be neglected at higher output currents where the copper losses dominate. Core loss information is usually available from the magnetics vendor. Proper inductor selection can affect the resulting power supply efficiency by more than 15%!

The copper loss in the inductor can be calculated using the following equation:

$$P_{L(Cu)} = I^2_{L(RMS)} \bullet R_{WINDING}$$

where $I_{L(RMS)}$ is the RMS inductor current that can be calculated as follows:

$$I_{L(RMS)} = I_{OUT(MAX)} \bullet \sqrt{1 + \frac{1}{3}\left(\frac{I_{PP}}{I_{OUT(MAX)}}\right)^2}$$

Output Capacitor Selection

The required ESR (Equivalent Series Resistance) and capacitance drive the selection of the type and quantity of the output capacitors. The ESR must be small enough that both the resistive voltage deviation due to a step change in the load current and the output ripple voltage do not exceed the tolerance limits expected on the output voltage. During an output load transient, the output capacitor must supply all the additional current demanded by the load until the SP7661 adjusts the inductor current to the new value.

In order to maintain V_{OUT},the capacitance must be large enough so that the output voltage is held up while the inductor current ramps to the value corresponding to the new load current. Additionally, the ESR in the output capacitor causes a step in the output voltage equal to the current. Because of the fast transient response and inherent 100% to 0% duty cycle capability provided by the SP7661 when exposed to output load transients, the output capacitor is typically chosen for ESR, not for capacitance value.

The ESR of the output capacitor, combined with the inductor ripple current, is typically the main contributor to output voltage ripple. The maximum allowable ESR required to maintain a specified output voltage ripple can be calculated by:

$$R_{ESR} \leq \frac{\Delta V_{OUT}}{I_{PK-PK}}$$

where:

ΔV_{OUT} = Peak-to-Peak Output Voltage Ripple

I_{PK-PK} = Peak-to-Peak Inductor Ripple Current

The total output ripple is a combination of the ESR and the output capacitance value and can be calculated as follows:

$$\Delta V_{OUT} = \sqrt{\left(\frac{I_{PP} \bullet (1 - D)}{f_S \bullet C_{OUT}}\right)^2 + (I_{PP} \bullet R_{ESR})^2}$$

f_S = Switching Frequency

D = Duty Cycle

C_{OUT} = Output Capacitance Value

Input Capacitor Selection

The input capacitor should be selected for ripple current rating, capacitance and voltage rating. The input capacitor must meet the ripple current requirement imposed by the switching current. In continuous conduction mode, the source current of the high-side MOSFET is approximately a square wave of duty cycle V_{OUT}/V_{IN}. More accurately, the current wave form is trapezoidal, given a finite turn-on and turn-off, switch transition slope. Most of this current is supplied by the input bypass capacitors. The RMS current handling capability of the input capacitors is determined at maximum output current and under the assumption that the peak-to-peak inductor ripple current is low, it is given by:

$$I_{CIN(RMS)} = I_{OUT(MAX)} \bullet \sqrt{D(1 - D)}$$

The worst case occurs when the duty cycle D is 50% and gives an RMS current value equal to $I_{OUT}/2$. Select input capacitors with adequate ripple current rating to ensure reliable operation.

The power dissipated in the input capacitor is:

$$P_{CIN} = I^2_{CIN(RMS)} \bullet R_{ESR(CIN)}$$

This can become a significant part of power losses in a converter and hurt the overall energy transfer efficiency. The input voltage ripple primarily depends on the input

capacitor ESR and capacitance. Ignoring the inductor ripple current, the input voltage ripple can be determined by:

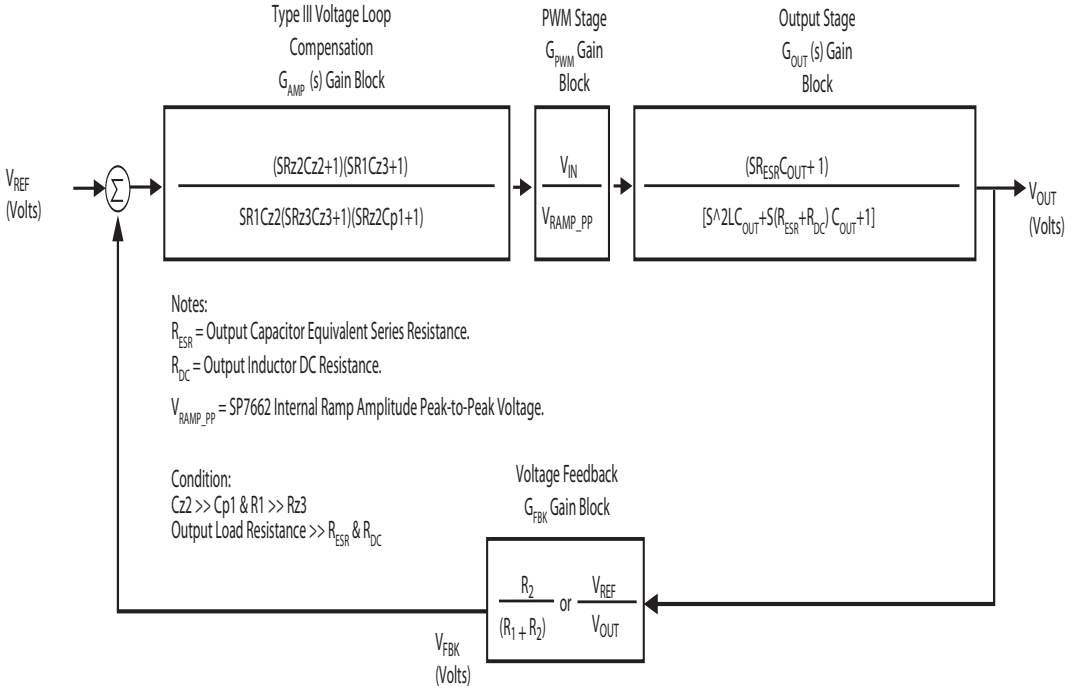
$$\Delta V_{IN} = I_{OUT(MAX)} \bullet R_{ESR(CIN)} + \frac{I_{OUT(MAX)} \bullet V_{OUT} \bullet (V_{IN} - V_{OUT})}{V^2_{IN} \bullet f_S \bullet C_{IN}}$$

The capacitor type suitable for the output capacitors can also be used for the input capacitors. However, exercise extra caution when tantalum capacitors are used. Tantalum capacitors are known for catastrophic failure when exposed to surge current, and input capacitors are prone to such surge current when power supplies are connected “live” to low impedance power sources. Although tantalum capacitors have been successfully employed at the input, it is generally not recommended.

Loop Compensation Design

The open loop gain of the whole system can be divided into the gain of the error amplifier, PWM modulator, buck converter output stage, and feedback resistor divider. In order to cross over at the desired frequency cut-off (FCO), the gain of the error amplifier must compensate for the attenuation caused by the rest of the loop at this frequency. The goal of loop compensation is to manipulate loop frequency response such that its crossover gain at 0db, results in a slope of -20db/decade.

The first step of compensation design is to pick the loop crossover frequency. High crossover frequency is desirable for fast transient response, but often jeopardizes the power supply stability. Crossover frequency should be higher than the ESR zero but less than 1/5 of the switching frequency or



SP7661 Voltage Mode Control Loop with Loop Dynamic

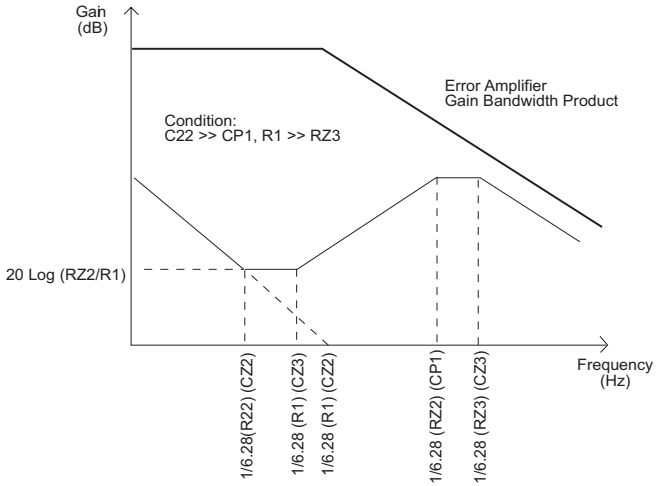
120kHz. The ESR zero is contributed by the ESR associated with the output capacitors and can be determined by:

$$f_{Z(ESR)} = \frac{1}{2\pi \cdot C_{OUT} \cdot R_{ESR}}$$

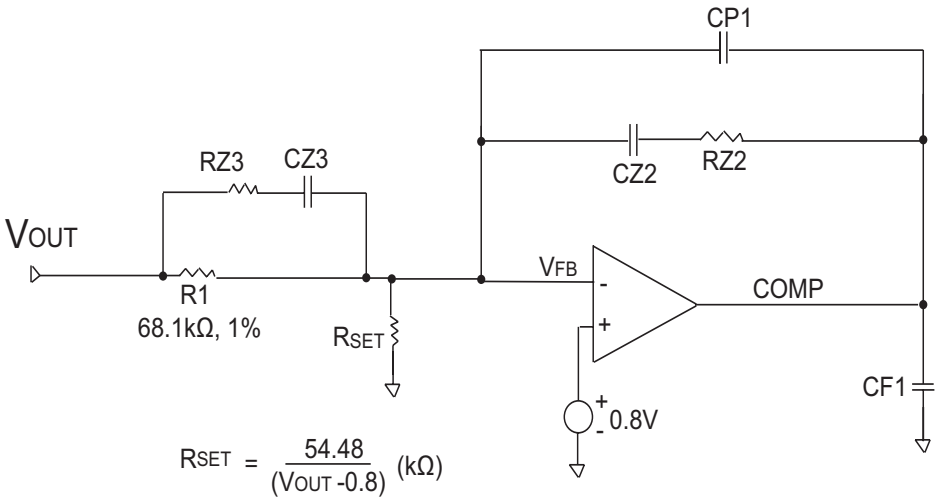
The next step is to calculate the complex conjugate poles contributed by the LC output filter,

$$f_{P(LC)} = \frac{1}{2\pi \cdot \sqrt{L \cdot C_{OUT}}}$$

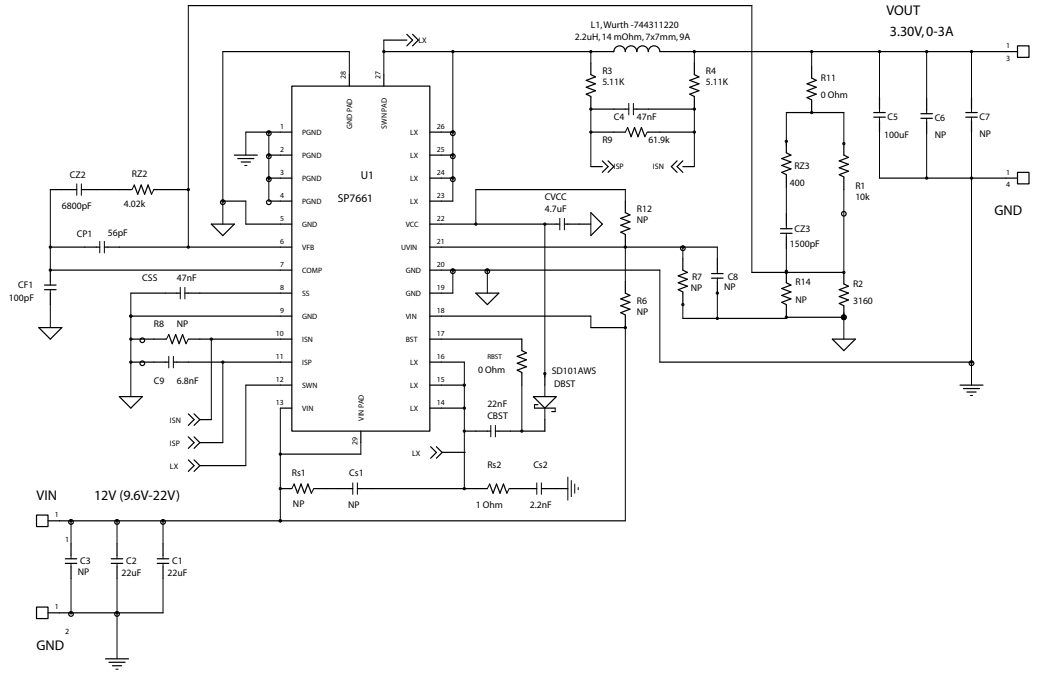
When the output capacitors are of a Ceramic Type, the SP7661 Evaluation Board requires a Type III compensation circuit to give a phase boost of 180° in order to counteract the effects of an underdamped resonance of the output filter at the double pole frequency.



Bode Plot of Type III Error Amplifier Compensation.

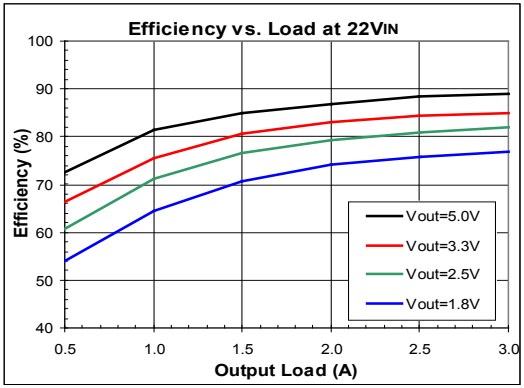


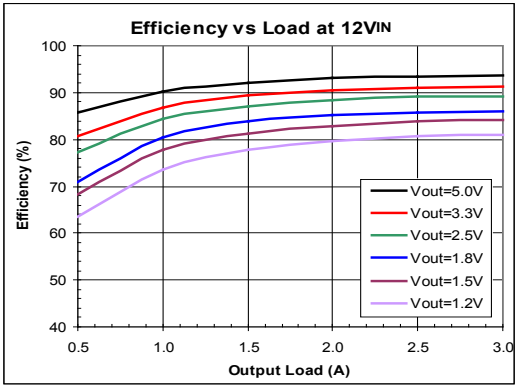
Type III Error Amplifier Compensation Circuit

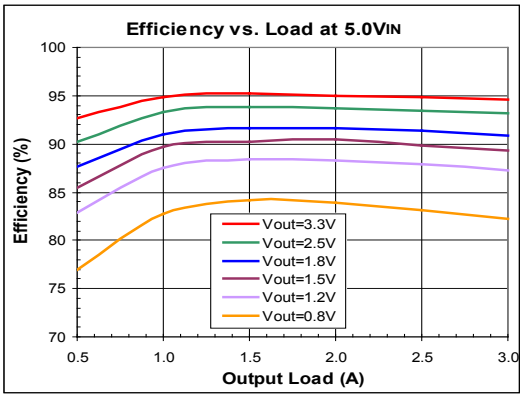


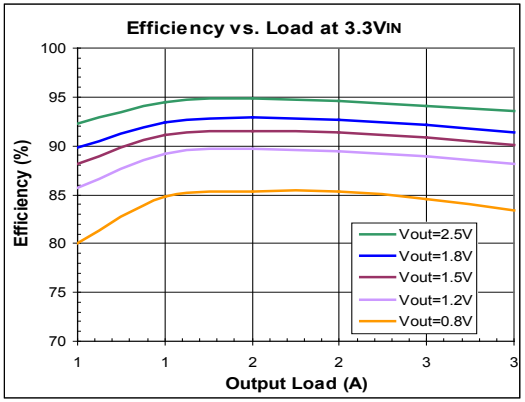
Evaluation Board Schematic

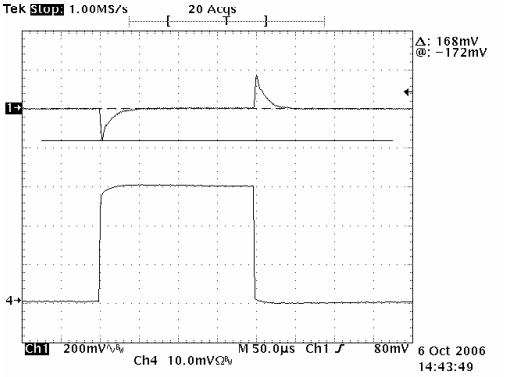
Parts shown for 9.6V-22V input, 3.3V Output



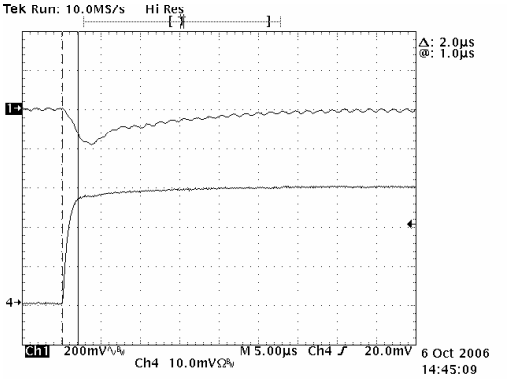




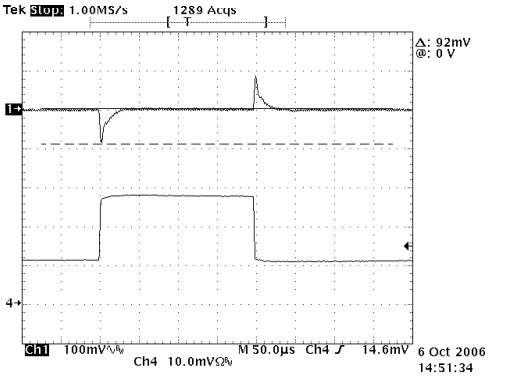




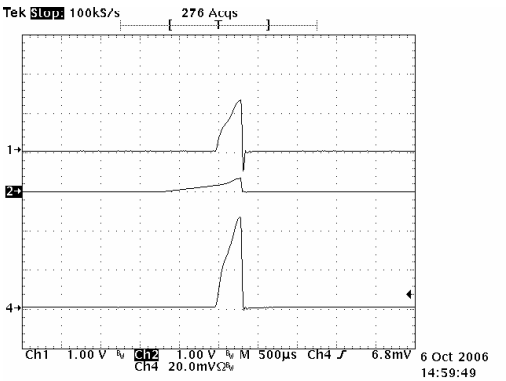
Transient Response:
CH1: VOUT. CH4: IOUT 1A/div.



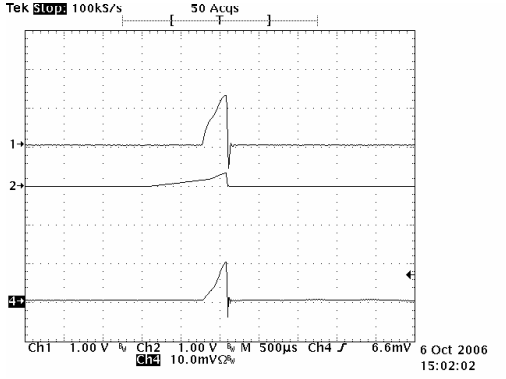
Transient Response: CH1: VOUT. CH4: IOUT 1A/div. Zoom showing ~1.5A/us Irate



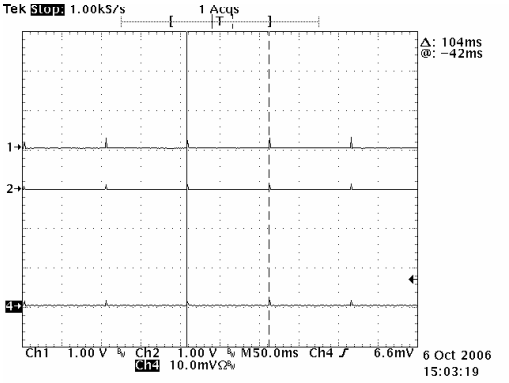
Transient Response:
CH1: VOUT. CH4: IOUT 1A/div.



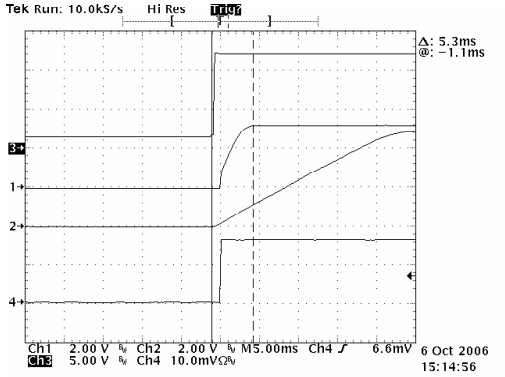
Short Circuit Protection: CH1:VOUT.
CH2:Sstart. CH4:IOUT(10A/div).



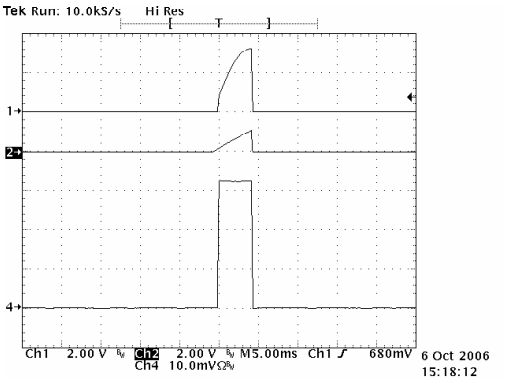
Short Circuit Protection: CH1:VOUT. CH2:
Sstart. CH4:Input Current (5A/div).



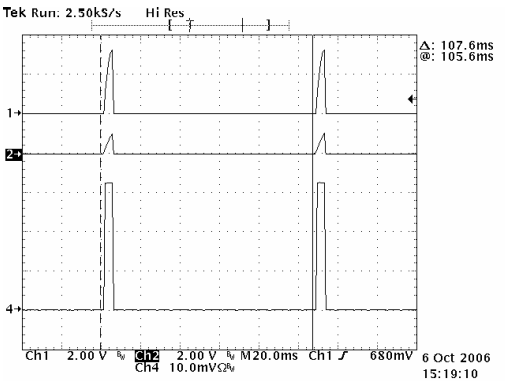
Short Circuit Protection: CH1:VOUT.
CH2:Sstart. CH4: Input Current (5A/div).
104ms restart rate shown.



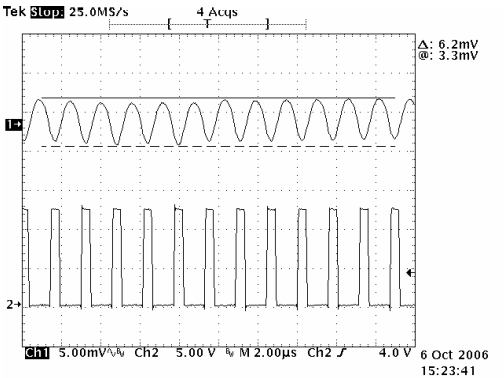
Start-up in to 3A Load: CH1:VOUT. CH2:SS. CH3:VIN. CH4: Iout (2A/div).



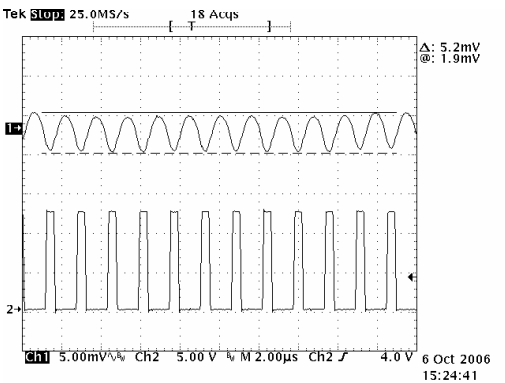
Current Limit: CH1: VOUT. CH2:SoftStart. CH4 IOUT (2A/div). Current is reaching approximtely 6A before a shutdown & restart



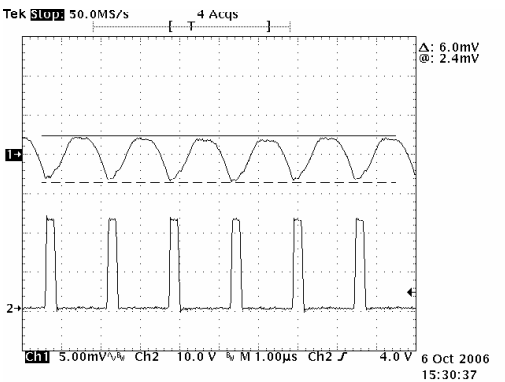
Current Limit: CH1: VOUT. CH2:SoftStart. CH4 IOUT (2A/div).
OCP Repeat rate is 107ms



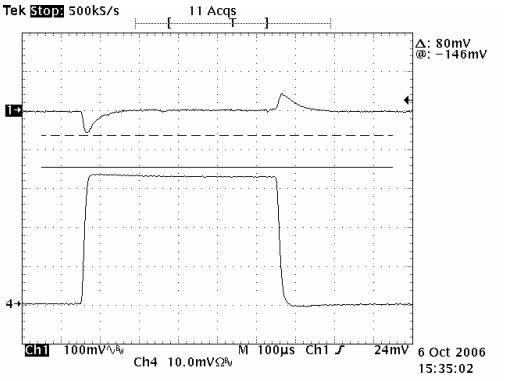
12Vin Output Ripple: CH1:VOUT. CH2: Switch Node taken at 3A Out.



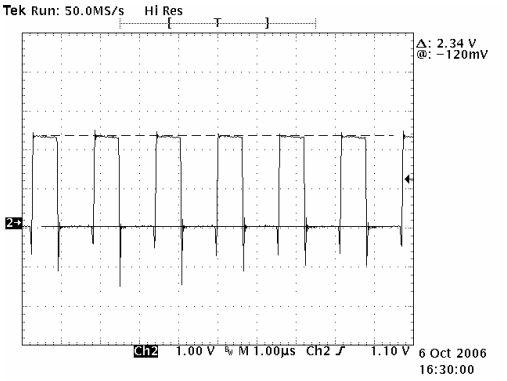
12Vin Output Ripple: CH1: VOUT. CH2: Switch Node taken at 0A Out.



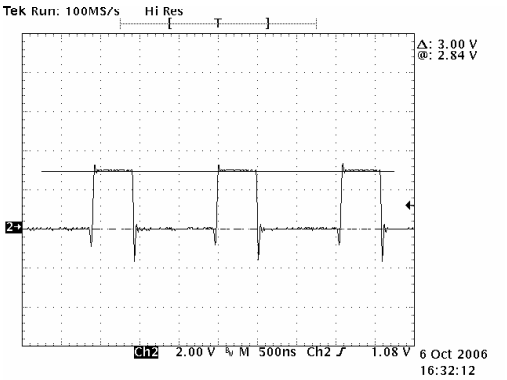
22Vin Output Ripple: CH1: VOUT. CH2: Switch Node taken at 0A out.



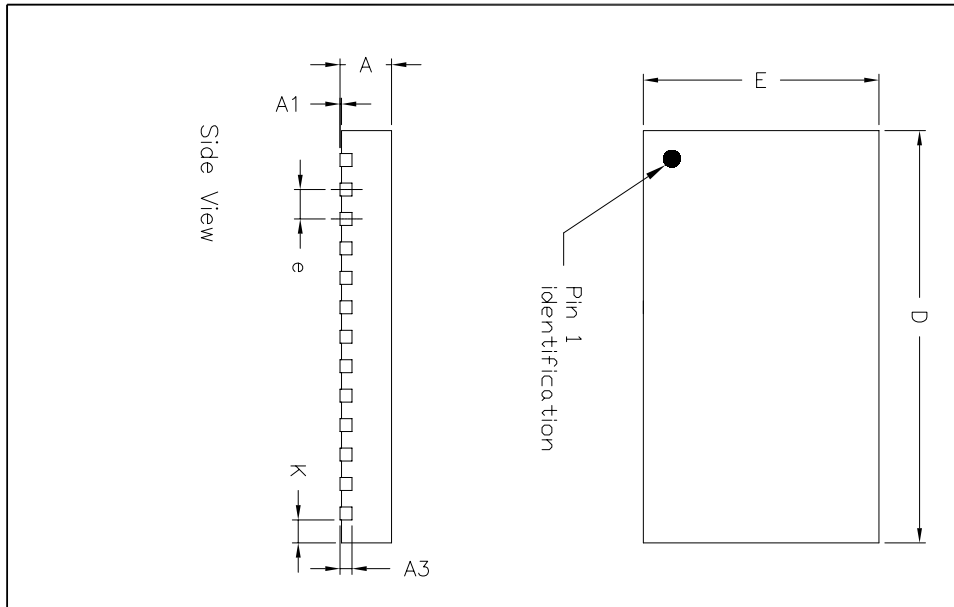
22Vin Transient Response
CH1: V_{OUT}. CH4: I_{OUT} (1A/div).



Operation from exernal bias:
CH2: Switchnode @ 2.34V_{IN}.



Operation from exernal bias:
CH2: Switchnode @ 3V_{IN}, I_{OUT} = 3A.



REVISION HISTORY			
REV.	DESCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	05/02/06	JL
B	REVISE DISTANCE BETWEEN EXPOSED PADS	06/29/06	JL

26LD 7 X 4 MM DFN -- (OPTION 2)*

SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0.00	—	0.05	0.000	—	0.002
A3	0.18	0.20	0.23	0.007	0.008	0.009
b	0.17	0.22	0.27	0.007	0.009	0.011
D	6.95	7.00	7.05	0.274	0.276	0.278
D1	2.55	2.60	2.65	0.100	0.102	0.104
D2	1.85	1.90	1.95	0.073	0.075	0.077
D3	1.45	1.50	1.55	0.057	0.059	0.061
e	0.50 BSC			0.020 BSC		
E	3.95	4.00	4.05	0.156	0.157	0.159
E2	2.75	2.80	2.85	0.108	0.110	0.112
J	0.17	0.22	0.25	0.007	0.009	0.010
J1	0.23	0.28	0.33	0.009	0.011	0.013
K	0.34	0.39	0.44	0.013	0.015	0.017
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.16 BSC			0.006 BSC		
N	26			26		

* Refer to product datasheet for POD option being used

SIPEX CORPORATION

26LD 7X4 DFN PACKAGE OUTLINE

Packaging Approval:		Drawing No:	26LD 7X4 DFN
By: JL	Date: 06/29/06	Revision: B	Sheet: 2 OF 3

Part Number	Junction Temperature	Package
SP7661ER/TR	-40°C to +125°C	26 Pin 7 X 4 DFN (Option 2)
SP7661ER-L/TR	-40°C to +125°C	(Lead Free) 26 Pin 7 X 4 DFN (Option 2)

/TR = Tape and Reel
Pack quantity is 3,000 26 pin DFN.

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