

MC14503B

Hex Non-Inverting 3-State Buffer

The MC14503B is a hex non-inverting buffer with 3-state outputs, and a high current source and sink capability. The 3-state outputs make it useful in common bussing applications. Two disable controls are provided. A high level on the Disable A input causes the outputs of buffers 1 through 4 to go into a high impedance state and a high level on the Disable B input causes the outputs of buffers 5 and 6 to go into a high impedance state.

Features

- 3-State Outputs
- TTL Compatible – Will Drive One TTL Load Over Full Temperature Range
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Two Disable Controls for Added Versatility
- Pin for Pin Replacement for MM80C97 and 340097
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- This Device is Pb-Free and is RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 1)

Parameter	Symbol	Value	Unit
DC Supply Voltage Range	V_{DD}	-0.5 to +18.0	V
Input or Output Voltage Range (DC or Transient)	V_{in} , V_{out}	-0.5 to V_{DD} + 0.5	V
Input Current (DC or Transient) per Pin	I_{in}	± 10	mA
Output Current (DC or Transient) per Pin	I_{out}	± 25	mA
Power Dissipation, per Package (Note 2)	P_D	500	mW
Ambient Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range		-65 to +150	°C
Lead Temperature (8-Second Soldering)		260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Maximum Ratings are those values beyond which damage to the device may occur.

2. Temperature Derating:

"D/DW" Package: -7.0 mW/°C From 65°C To 125°C

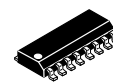
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



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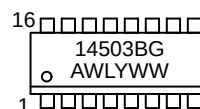


1
SOIC-16
D SUFFIX
CASE 751B

PIN ASSIGNMENT

DIS A	1	16	V_{DD}
IN 1	2	15	DIS B
OUT 1	3	14	IN 6
IN 2	4	13	OUT 6
OUT 2	5	12	IN 5
IN 3	6	11	OUT 5
OUT 3	7	10	IN 4
V_{SS}	8	9	OUT 4

MARKING DIAGRAM



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb-Free Package

TRUTH TABLE

In_n	Appropriate Disable Input	Out_n
0	0	0
1	0	1
X	1	High Impedance

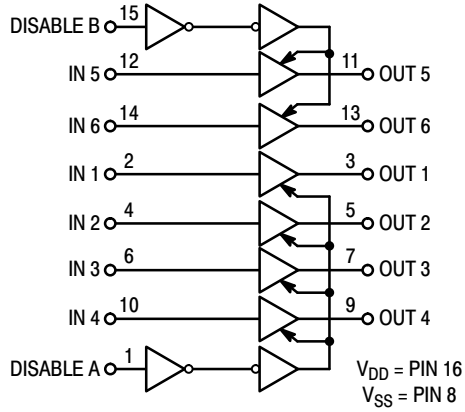
X = Don't Care

ORDERING INFORMATION

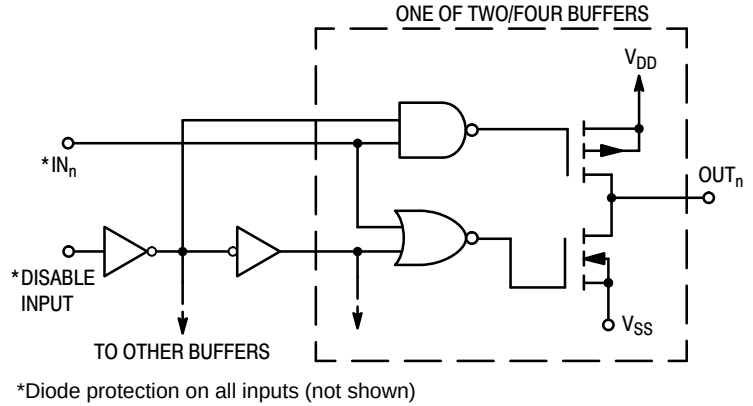
See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

MC14503B

LOGIC DIAGRAM



CIRCUIT DIAGRAM



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	– 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (Note 3)	Max	Min	Max	
Output Voltage V _{in} = 0 "0" Level	V _{OL}	5.0 10 15	– – –	0.05 0.05 0.05	– – –	0 0 0	0.05 0.05 0.05	– – –	0.05 0.05 0.05	Vdc
V _{in} = V _{DD} "1" Level	V _{OH}	5.0 10 15	4.95 9.95 14.95	– – –	4.95 9.95 14.95	5.0 10 15	– – –	4.95 9.95 14.95	– – –	Vdc
Input Voltage (V _O = 3.6 or 1.4 Vdc) (V _O = 7.2 or 2.8 Vdc) (V _O = 11.5 or 3.5 Vdc) "0" Level	V _{IL}	5.0 10 15	– – –	1.5 3.0 4.0	– – –	2.25 4.50 6.75	1.5 3.0 4.0	– – –	1.5 3.0 4.0	Vdc
(V _O = 1.4 or 3.6 Vdc) (V _O = 2.8 or 7.2 Vdc) (V _O = 3.5 or 11.5 Vdc) "1" Level	V _{IH}	5.0 10 15	3.5 7.0 11	– – –	3.5 7.0 11	2.75 5.50 8.25	– – –	3.5 7.0 11	– – –	Vdc
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) Source	I _{OH}	4.5 5.0 5.0 10 15	–4.3 –5.8 –1.2 –3.1 –8.2	– – – – –	–3.6 –4.8 –1.02 –2.6 –6.8	–5.0 –6.1 –1.4 –3.7 –14.1	– – – – –	–2.5 –3.0 –0.7 –1.8 –4.8	– – – – –	mAdc
(V _{OL} = 0.4 Vdc) (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc) Sink	I _{OL}	4.5 5.0 10 15	2.2 2.6 6.5 19.2	– – – –	1.8 2.1 5.5 16.1	2.1 2.3 6.2 25	– – – –	1.2 1.3 3.8 11.2	– – – –	mAdc
Input Current	I _{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Capacitance, (V _{in} = 0)	C _{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current, (Per Package)	I _Q	5.0 10 15	– – –	1.0 2.0 4.0	– – –	0.002 0.004 0.006	1.0 2.0 4.0	– – –	30 60 120	μAdc
Total Supply Current (Note 4, 5) (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs) (All outputs switching, 50% Duty Cycle)	I _T	5.0 10 15	I _T = (2.5 μA/kHz) f + I _{DD} I _T = (6.0 μA/kHz) f + I _{DD} I _T = (10 μA/kHz) f + I _{DD}							μAdc
3–State Output Leakage Current	I _{TL}	15	–	±0.1	–	±0.0001	±0.1	–	±3.0	μAdc

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

4. The formulas given are for the typical characteristics only at 25°C.

5. To calculate total supply current at loads other than 50 pF: I_T(C_L) = I_T(50 pF) + (C_L – 50) Vfk where: I_T is in μA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.006.

MC14503B

SWITCHING CHARACTERISTICS (Note 6) ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V_{DD} V_{CC}	All Types		Unit
			Typ (Note 7)	Max	
Output Rise Time $t_{TLH} = (0.5 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH} = (0.3 \text{ ns/pF}) C_L + 8.0 \text{ ns}$ $t_{TLH} = (0.2 \text{ ns/pF}) C_L + 8.0 \text{ ns}$	t_{TLH}	5.0 10 15	45 23 18	90 45 35	ns
Output Fall Time $t_{THL} = (0.5 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{THL} = (0.3 \text{ ns/pF}) C_L + 8.0 \text{ ns}$ $t_{THL} = (0.2 \text{ ns/pF}) C_L + 8.0 \text{ ns}$	t_{THL}	5.0 10 15	45 23 18	90 45 35	ns
Turn-Off Delay Time, all Outputs $t_{PLH} = (0.3 \text{ ns/pF}) C_L + 60 \text{ ns}$ $t_{PLH} = (0.15 \text{ ns/pF}) C_L + 27 \text{ ns}$ $t_{PLH} = (0.1 \text{ ns/pF}) C_L + 20 \text{ ns}$	t_{PLH}	5.0 10 15	75 35 25	150 70 50	ns
Turn-On Delay Time, all Outputs $t_{PHL} = (0.3 \text{ ns/pF}) C_L + 60 \text{ ns}$ $t_{PHL} = (0.15 \text{ ns/pF}) C_L + 27 \text{ ns}$ $t_{PHL} = (0.1 \text{ ns/pF}) C_L + 20 \text{ ns}$	t_{PHL}	5.0 10 15	75 35 25	150 70 50	ns
3-State Propagation Delay Time Output "1" to High Impedance Output "0" to High Impedance High Impedance to "1" Level High Impedance to "0" Level	t_{PHZ}	5.0 10 15	75 40 35	150 80 70	ns
	t_{PLZ}	5.0 10 15	80 40 35	160 80 70	ns
	t_{PZH}	5.0 10 15	65 25 20	130 50 40	ns
	t_{PZL}	5.0 10 15	100 35 25	200 70 50	ns

6. The formulas given are for the typical characteristics only at 25°C .

7. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

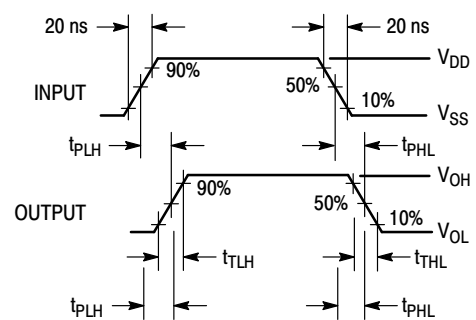
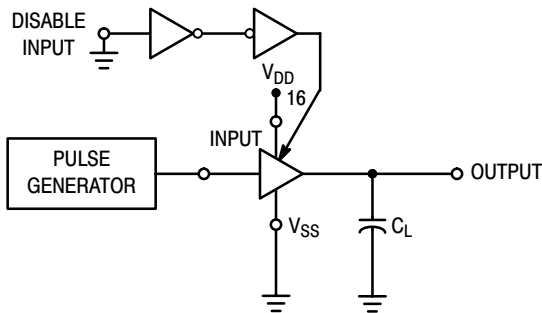


Figure 1. Switching Time Test Circuit and Waveforms
(t_{TLH} , t_{THL} , t_{PHL} , and t_{PLH})

MC14503B

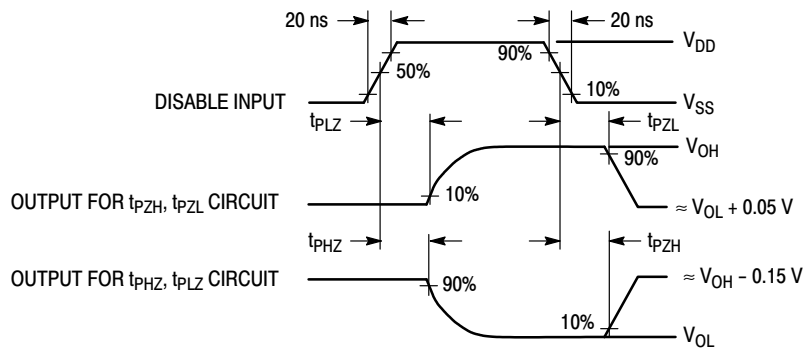
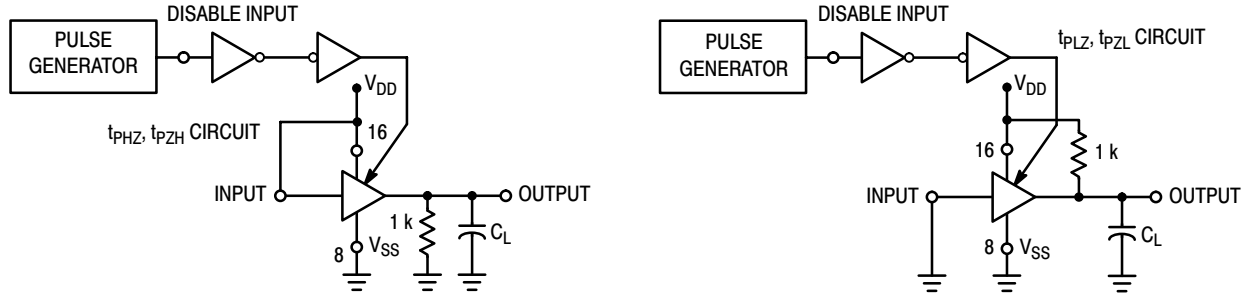


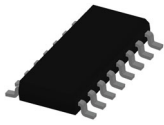
Figure 2. 3-State AC Test Circuit and Waveforms
(t_{PLZ} , t_{PHZ} , t_{PZH} , t_{PZL})

ORDERING INFORMATION

Device	Package	Shipping [†]
MC14503BDG	SOIC-16 (Pb-Free)	48 / Rail
MC14503BDR2G	SOIC-16 (Pb-Free)	2500 / Tape & Reel
NLV14503BDR2G*	SOIC-16 (Pb-Free)	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

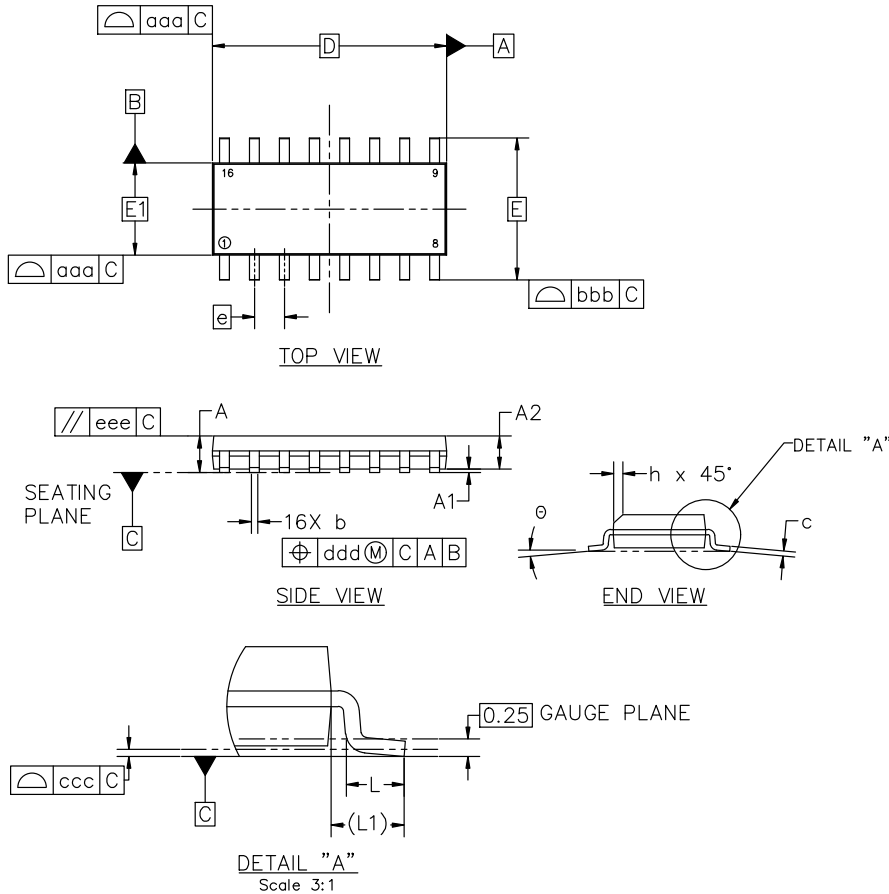
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.


SOIC-16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

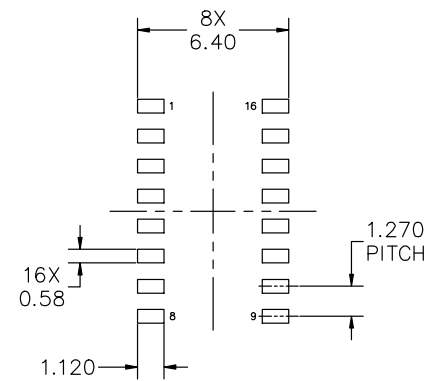
DATE 18 OCT 2024

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.25	1.37	1.50
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	---	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
θ	0°	---	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D

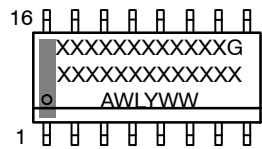
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SOIC-16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

GENERIC
MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1: PIN 1. COLLECTOR 2. BASE 3. EMITTER 4. NO CONNECTION 5. EMITTER 6. BASE 7. COLLECTOR 8. COLLECTOR 9. BASE 10. EMITTER 11. NO CONNECTION 12. EMITTER 13. BASE 14. COLLECTOR 15. EMITTER 16. COLLECTOR	STYLE 2: PIN 1. CATHODE 2. ANODE 3. NO CONNECTION 4. CATHODE 5. CATHODE 6. NO CONNECTION 7. ANODE 8. CATHODE 9. CATHODE 10. ANODE 11. NO CONNECTION 12. CATHODE 13. CATHODE 14. NO CONNECTION 15. ANODE 16. CATHODE	STYLE 3: PIN 1. COLLECTOR, DYE #1 2. BASE, #1 3. EMITTER, #1 4. COLLECTOR, #1 5. COLLECTOR, #2 6. BASE, #2 7. EMITTER, #2 8. COLLECTOR, #2 9. COLLECTOR, #3 10. BASE, #3 11. EMITTER, #3 12. COLLECTOR, #3 13. COLLECTOR, #4 14. BASE, #4 15. EMITTER, #4 16. COLLECTOR, #4	STYLE 4: PIN 1. COLLECTOR, DYE #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. COLLECTOR, #3 6. COLLECTOR, #3 7. COLLECTOR, #4 8. COLLECTOR, #4 9. BASE, #4 10. EMITTER, #4 11. BASE, #3 12. EMITTER, #3 13. BASE, #2 14. EMITTER, #2 15. BASE, #1 16. EMITTER, #1
STYLE 5: PIN 1. DRAIN, DYE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. DRAIN, #3 6. DRAIN, #3 7. DRAIN, #4 8. DRAIN, #4 9. GATE, #4 10. SOURCE, #4 11. GATE, #3 12. SOURCE, #3 13. GATE, #2 14. SOURCE, #2 15. GATE, #1 16. SOURCE, #1	STYLE 6: PIN 1. CATHODE 2. CATHODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE 7. CATHODE 8. CATHODE 9. ANODE 10. ANODE 11. ANODE 12. ANODE 13. ANODE 14. ANODE 15. ANODE 16. ANODE	STYLE 7: PIN 1. SOURCE N-CH 2. COMMON DRAIN (OUTPUT) 3. COMMON DRAIN (OUTPUT) 4. GATE P-CH 5. COMMON DRAIN (OUTPUT) 6. COMMON DRAIN (OUTPUT) 7. COMMON DRAIN (OUTPUT) 8. SOURCE P-CH 9. SOURCE P-CH 10. COMMON DRAIN (OUTPUT) 11. COMMON DRAIN (OUTPUT) 12. COMMON DRAIN (OUTPUT) 13. GATE N-CH 14. COMMON DRAIN (OUTPUT) 15. COMMON DRAIN (OUTPUT) 16. SOURCE N-CH	

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