EMIF06-AUD01F2

6-line EMI filter and ESD protection for audio interface

Features

- 4-line EMI filter and ESD protection for internal and external (headset) microphone
- 2-line EMI filter and ESD protection for headset speaker

Benefits

- EMI (I/O) low-pass filter
- High efficiency EMI filter
- Very low PCB space consumption: 4.6 mm^2
- Very thin package: 0.65 mm
- High efficiency in ESD suppression
- High reliability offered by monolithic integration
- High reduction of parasitic elements through integration and wafer level packaging

Complies with following standards

- IEC 61000-4-2 level 4 external pins
  – 15 kV (air discharge)
  – 8 kV (contact discharge)
- IEC 61000-4-2 level 1 internal pins
  – 2 kV (air discharge)
  – 2 kV (contact discharge)

Applications

ESD protection and EMI/RFI filtering for the audio bottom connector interface, where EMI filtering in ESD sensitive equipment is required:

- Mobile phones and communication systems
- Wireless modules

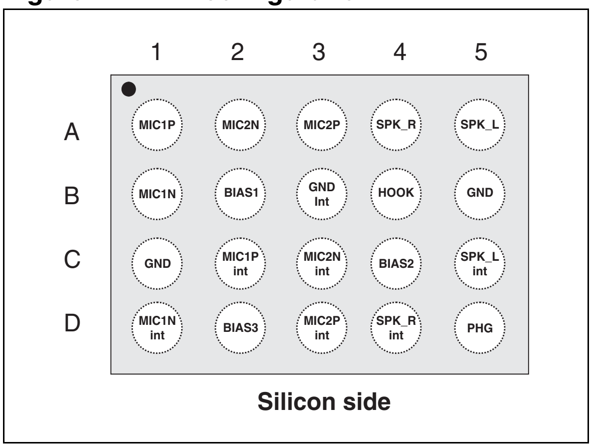
Flip chip package, 20 bumps

Description

The EMIF06-AUD01F2 is a highly integrated device designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interference. The flip chip packaging means the package size is equal to the die size.

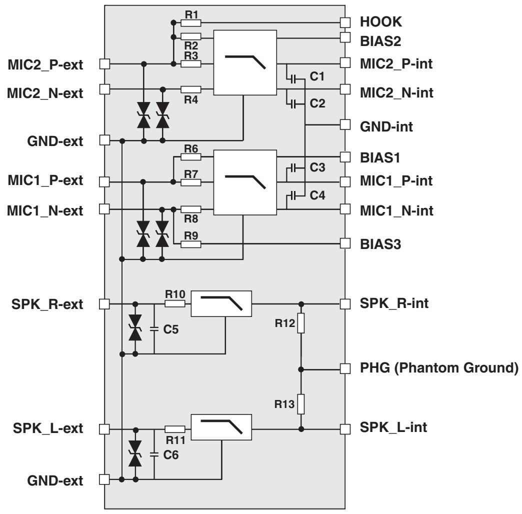
This filter includes ESD protection circuitry, which prevents damage to the application when it is subjected to ESD surges up to 15 kV.

Figure 1. Pin configuration



1 Characteristics

Figure 2. Circuit schematic



C1 to C4 = 1.3 nF typical

Table 1. Absolute ratings (limiting values)

Symbol	Parameter	Test conditions	Min	Max	Unit
V_{pp}	IEC61000-4-2 air discharge on external lines IEC61000-4-2 contact discharge on external lines IEC61000-4-2 air discharge on internal lines IEC61000-4-2 contact discharge on internal lines			15 15 2 2	kV
P_{SPK}	Continuous power dissipation per channel SPK_L, SPK_R	T_{amb} = 85 °C		180	mW
I_{SPK}	Continuous current per channel SPK_L, SPK_R	T_{amb} = 85 °C		135	mA
P_{total}	Total continuous power dissipation	T_{amb} = 85 °C		285	mW
T_{op}	Operating temperature range		-40	+85	°C
T_{stg}	Storage temperature range		-40	+125	°C
T_j	Junction temperature			+125	°C

Table 2. Electrical characteristics - definitions (T_{amb} = 25 °C)

Symbol	Parameters
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
R_d	Dynamic impedance
I_{PP}	Peak pulse current
C_{line}	Input capacitance per line

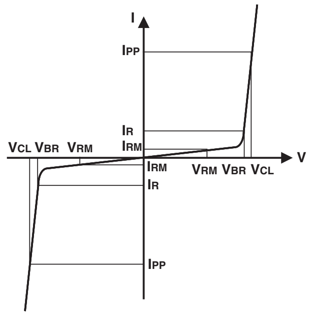


Table 3. Electrical characteristics - values (T_{amb} = -40 °C to + 85 °C unless otherwise specified)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{BR}	Diode reverse breakdown voltage	I_R = 1 mA T_{amb} = 25 °C	14.0			V
I_{RM}	Leakage current through clamping diodes	V_R = 3 V DC per line T_{amb} = 25 °C			0.5	µA
C1-C4[1]	Capacitance on MIC lines	V = 0 V, F = 1 MHz, V_{OSC} = 30 mV T_{amb} = 25 °C		1.3		nF
C5-C6[1]	Channel Capacitance SPK_L, SPK_R			60		pF
R1[2]	Hook Pull up resistance			47		kΩ
R2[2]	External Microphone Pull up resistance			2.2		kΩ
R3,R4, R7, R8[2]	Microphone Serial Resistance			100		Ω
R6, R9[2]	Internal Microphone Pull up and Pull down resistance			1		kΩ
R10, R11[3]	SPK Serial Resistance			10		Ω
R12, R13[2]	SPK PHG Resistance			15		kΩ
MICx channel THD	Distortion	V_{dc} = 0 - 2.4 V, [4] F = 20 Hz - 20 kHz, R_{gen} = 600 Ω, V_{out} = 1.5 V_{PP} R_{load} = 200 kΩ, T_{amb} = 25 °C Balanced (or differential mode)			-75	dB(A)

1. Capacitor tolerance ±30%
2. Resistor tolerances ±10%
3. Resistor tolerances ±20%
4. See *Figure 20* and *Figure 21*

1.1 RF filtering

The low signal level on the analog inputs and the pulsed transmitter in the phone are a combination that requires efficient RF-filtering. **RF-rectification must be avoided.** Therefore, the stop band attenuation is optimized for the frequency bands 800-2480 MHz.

Table 4. Stop band performance 800 - 2480 MHz

Channel	Test conditions	Attenuation			
		Min	Typ	Max	Unit
MIC1_x to MIC1_x-int	R_{source} = 50 Ω, R_{load} = 1 kΩ	25			dB
MIC2_x to MIC2_x-int	R_{source} = 50 Ω, R_{load} = 1 kΩ	25			dB
MIC1_P to BIAS1	R_{source} = 50 Ω, R_{load} = 1 kΩ	25			dB
MIC2_P to BIAS2	R_{source} = 50 Ω, R_{load} = 1 kΩ	25			dB
SPK_x to SPK_x-int	R_{source} = 50 Ω, R_{load} = 1 kΩ	25			dB

Table 5. Stop band performance 10 - 800 MHz

Channel	Test conditions	Attenuation			
		Min	Typ	Max	Unit
MIC1_x to MIC1_x-int	R_{source} = 50 Ω, R_{load} = 1 kΩ	20			dB
MIC2_x to MIC2_x-int	R_{source} = 50 Ω, R_{load} = 1 kΩ	20			dB
MIC1_P to BIAS1	R_{source} = 50 Ω, R_{load} = 1 kΩ	20			dB
MIC2_P to BIAS2	R_{source} = 50 Ω, R_{load} = 1 kΩ	20			dB

1.2 Attenuation characteristics

Figure 3. S21 attenuation measurement MIC1_P and MIC1_N lines (50 Ω / 50 Ω)

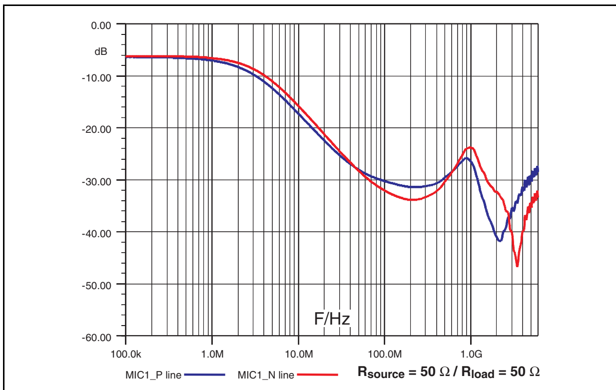


Figure 4. S21 attenuation measurement MIC1_P and MIC1_N lines (50 Ω / 1 KΩ simulation)

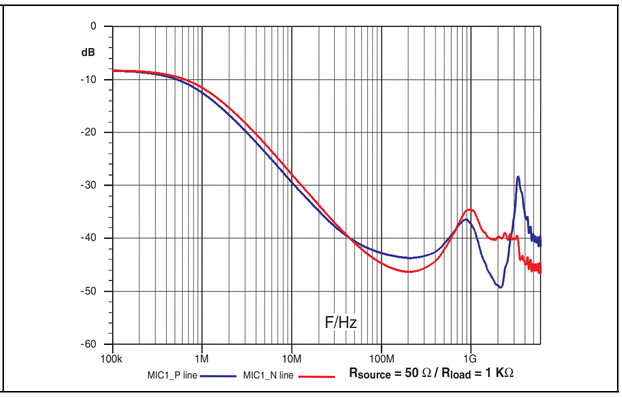


Figure 5. S21 attenuation measurement MIC2_P and MIC2_N lines (50 Ω / 50 Ω)

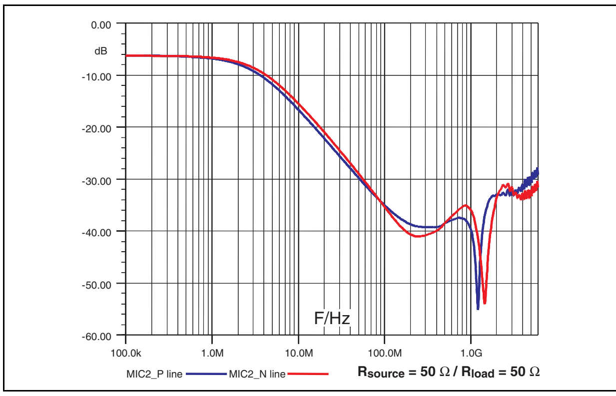


Figure 6. S21 attenuation measurement MIC2_P and MIC2_N lines (50 Ω / 1 KΩ simulation)

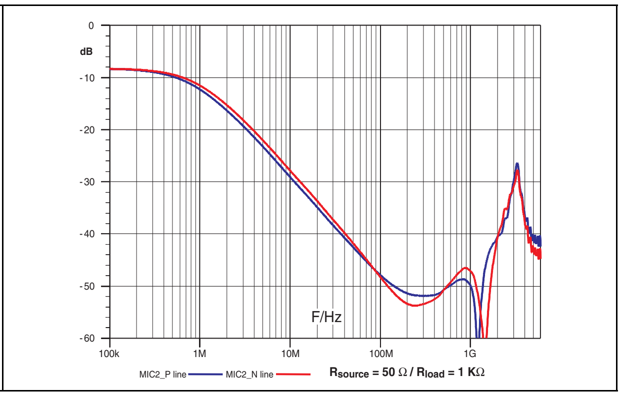


Figure 7. S21 attenuation measurement SPK_L and SPK_R lines (50 Ω / 50 Ω)

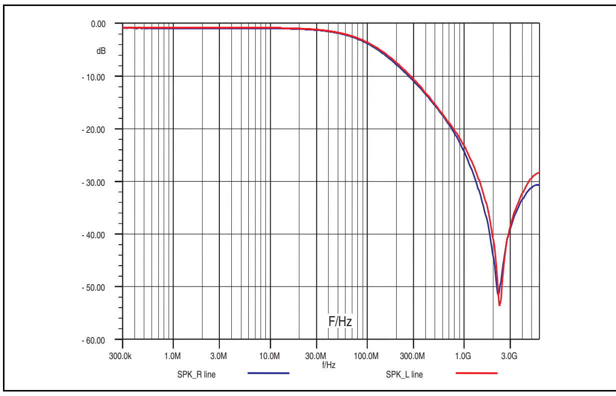


Figure 8. S21 attenuation measurement SPK_L and SPK_R lines (50 Ω / 1 KΩ simulation)

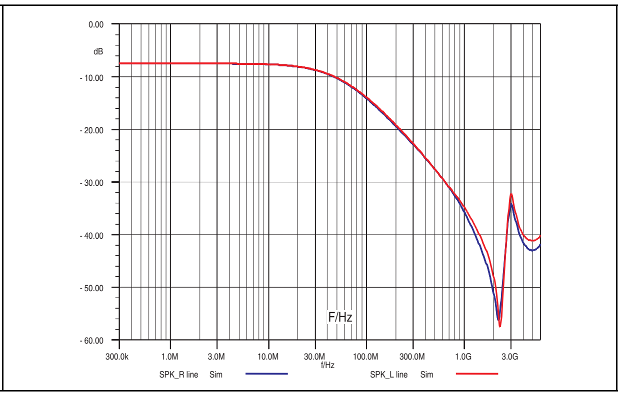


Figure 9. S21 attenuation measurement MIC1_P and BIAS1 lines (50 Ω / 50 Ω)

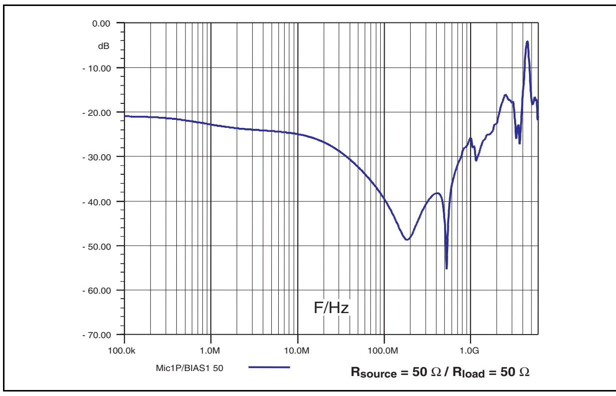


Figure 10. S21 attenuation measurement MIC1_P and BIAS1 lines (50 Ω / 1 KΩ simulation)

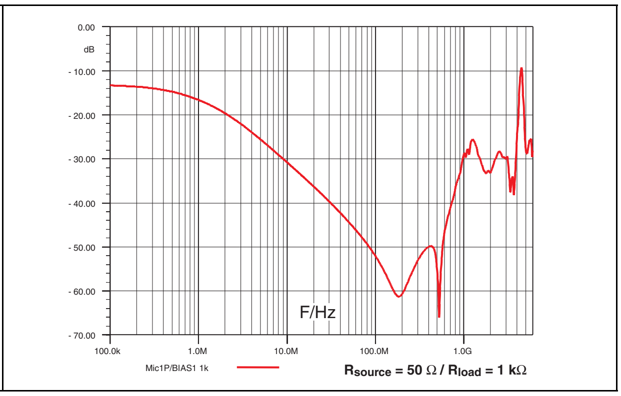


Figure 11. S21 attenuation measurement MIC2_P and BIAS2 lines (50 Ω / 50 Ω)

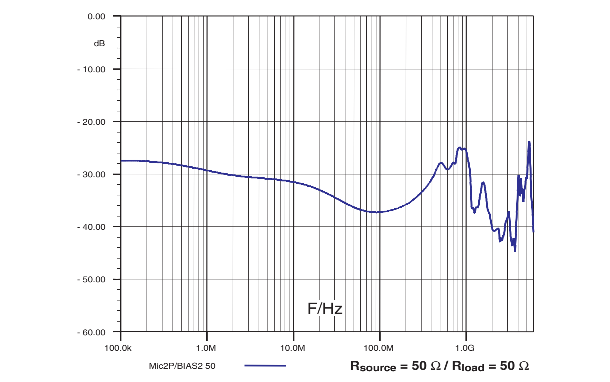
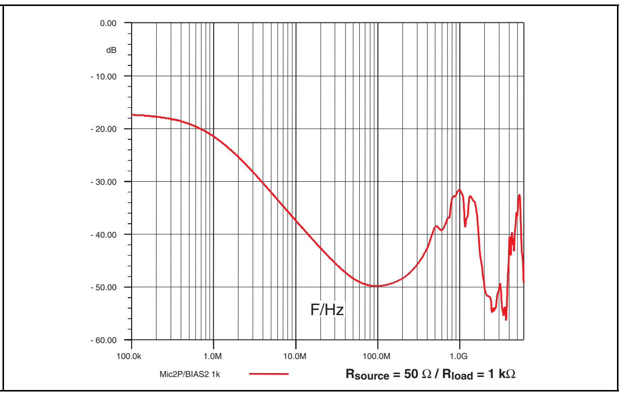


Figure 12. S21 attenuation measurement MIC2_P and BIAS2 lines (50 Ω / 1 KΩ simulation)



1.3 ESD characteristics

Figure 13. ESD response to IEC 61000-4-2 (+15 kV air discharge) on input V_{in} and output V_{out} Mic1 line

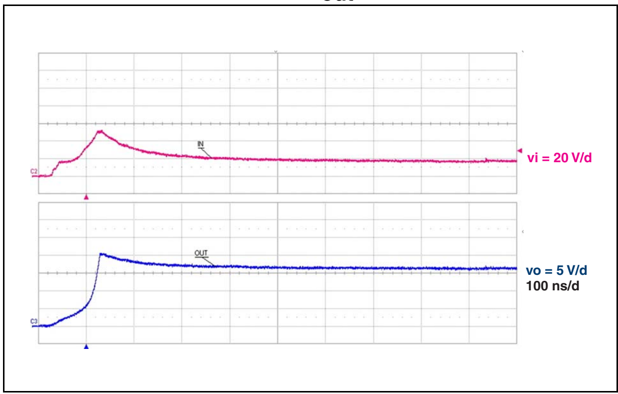


Figure 14. ESD response to IEC 61000-4-2 (-15 kV air discharge) on input V_{in} and output V_{out} Mic1 line

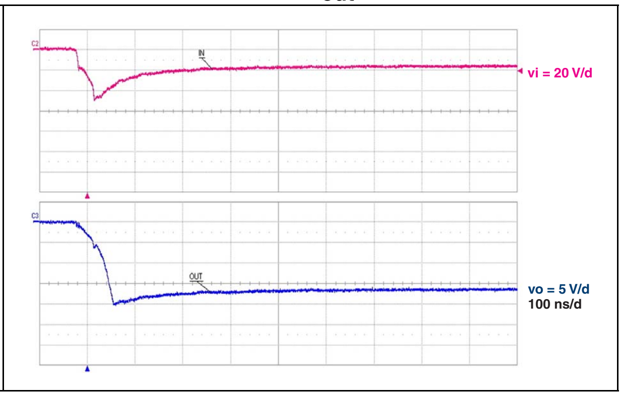


Figure 15. ESD response to IEC 61000-4-2 (+15 kV air discharge) on input V_{in} and output V_{out} Mic2 line

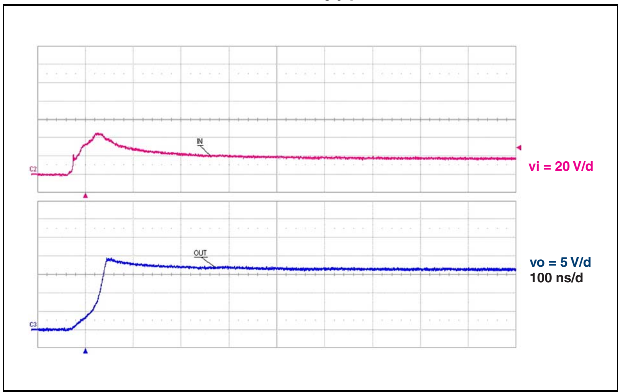
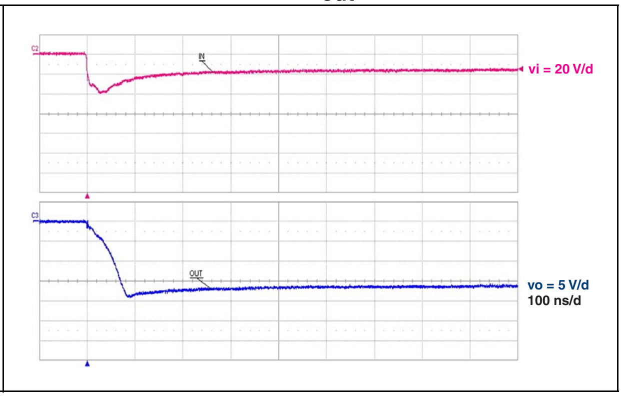


Figure 16. ESD response to IEC 61000-4-2 (-15 kV air discharge) on input V_{in} and output V_{out} Mic2 line



1.4 Filter characteristics

Figure 17. Analog crosstalk MIC2_P and MIC1_N lines (50 Ω / 50 Ω)

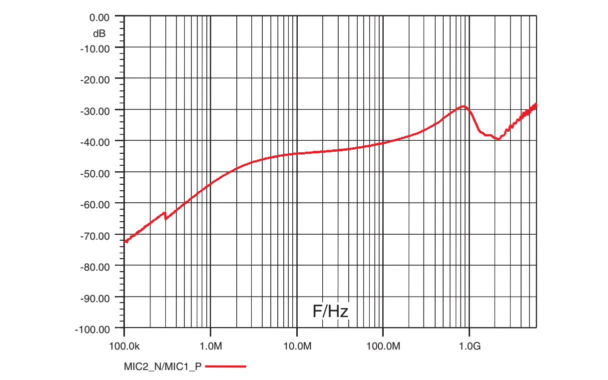
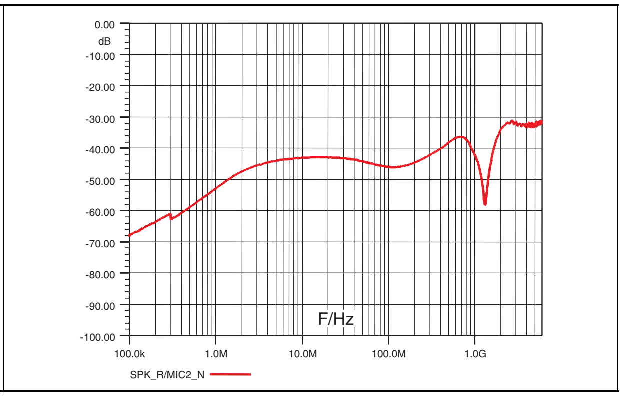


Figure 18. Analog crosstalk SPK_R and MIC2_N lines (50 Ω / 50 Ω)



1.5 Total harmonic distortion characteristics

Figure 19. Total harmonic distortion and noise with only cables and environmental circuit versus frequency, V_{BIAS} = 0 V

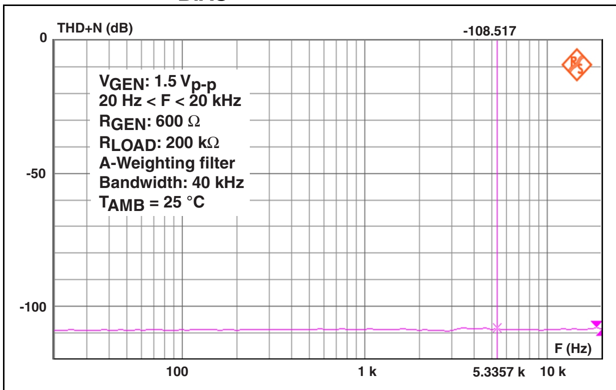


Figure 20. Variation of total harmonic distortion and noise in microphone lines versus frequency, balanced (or differential) mode, V_{BIAS} = 0 V

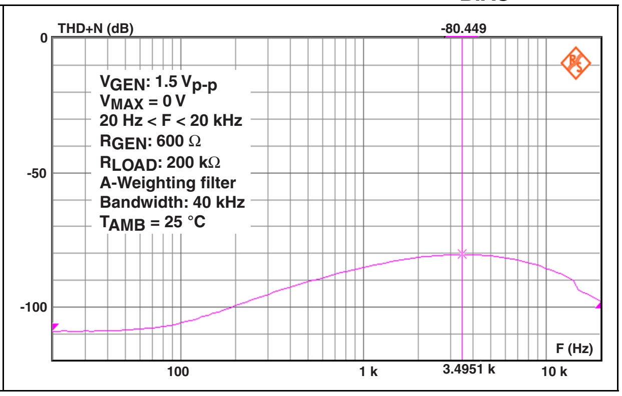


Figure 21. Variation of total harmonic distortion and noise in microphone lines versus frequency, balanced (or differential) mode, V_{BIAS} = 2.4 V

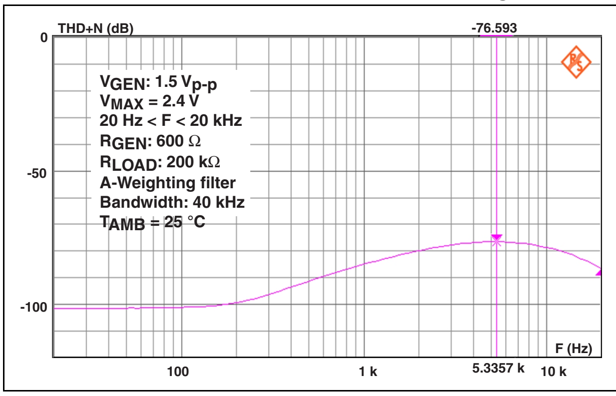


Figure 22. Variation of total harmonic distortion and noise in microphone lines versus frequency, unbalanced (or single-ended) mode

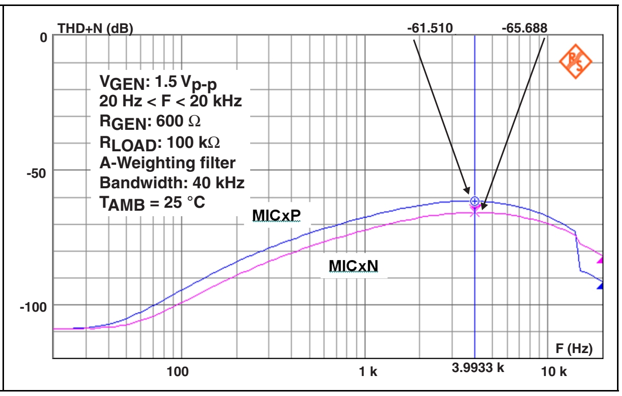


Figure 23. Test setup for measurement of distortion on MIC channels

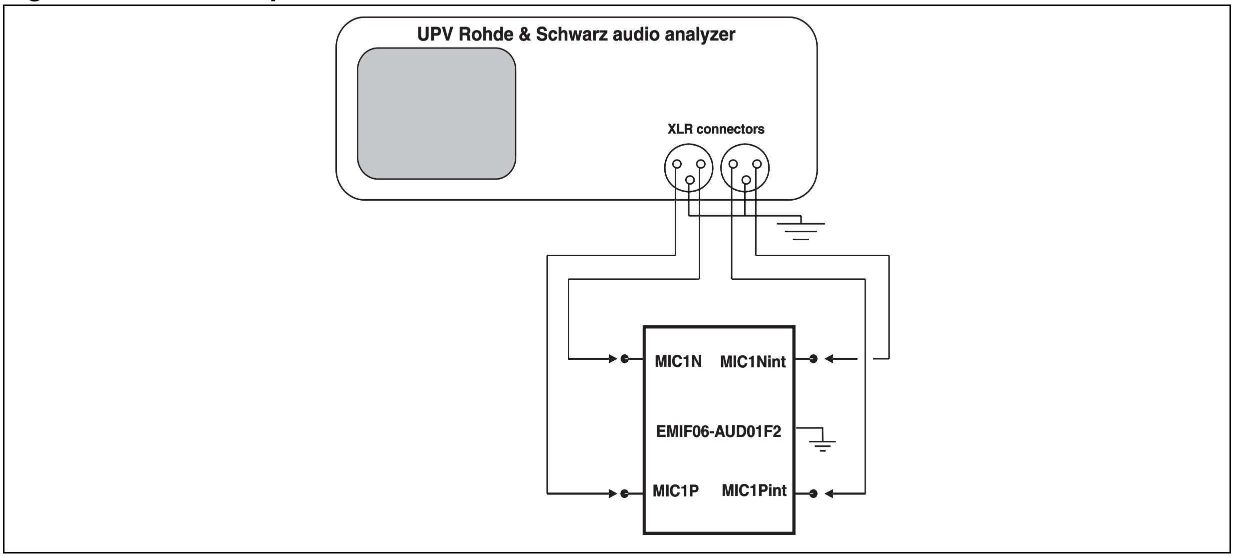
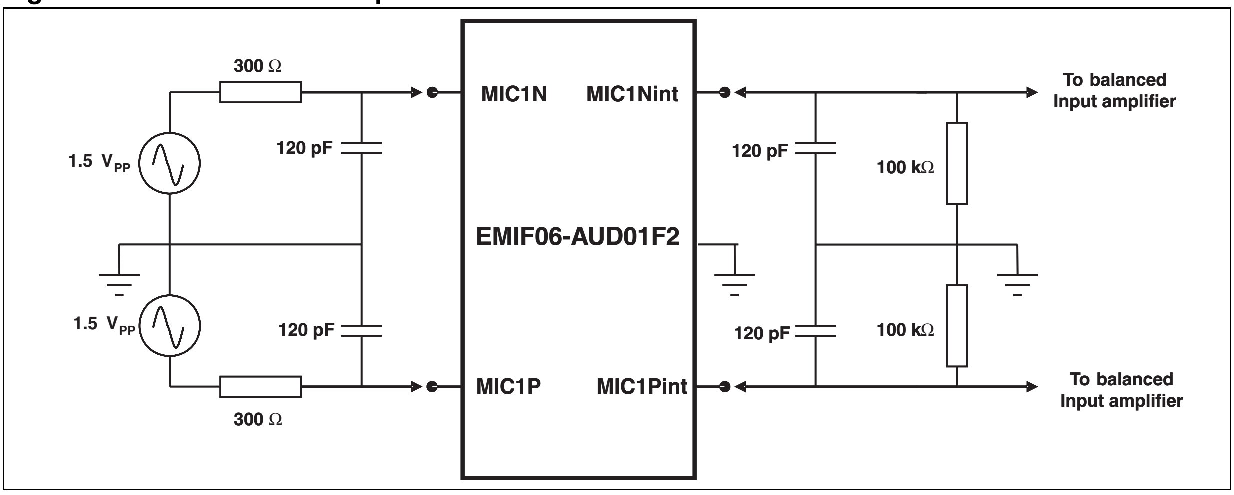


Figure 24. Internal UPV setup schematic



2 Application schematics

Figure 25. Basic configuration scheme

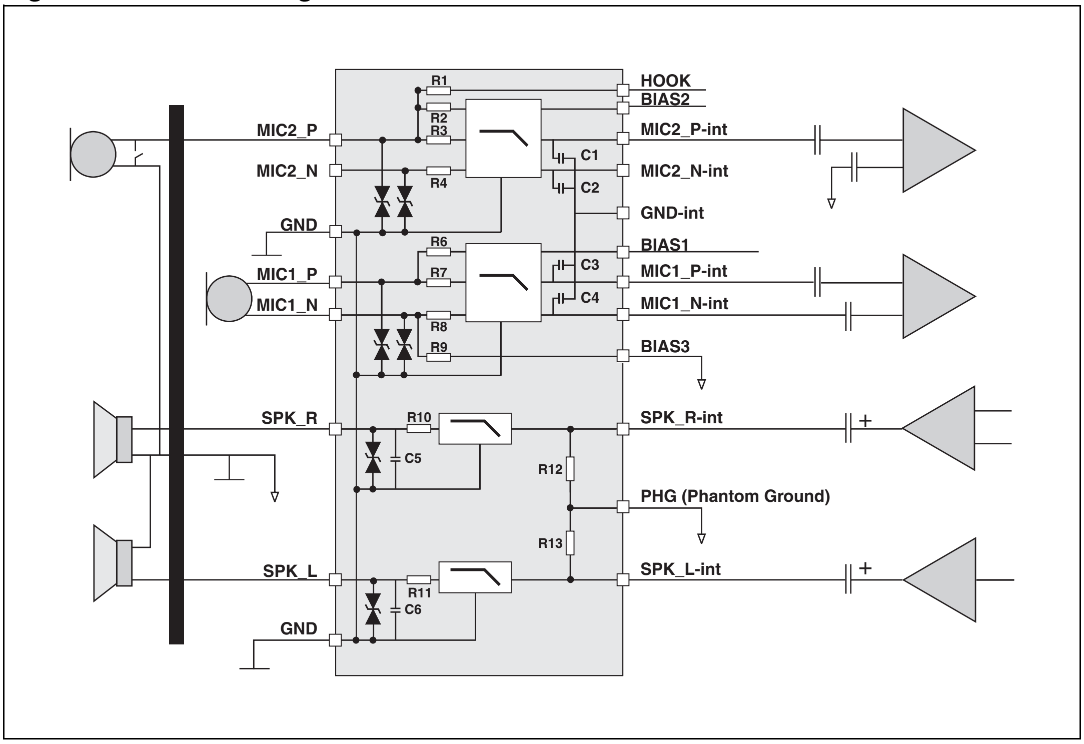


Figure 26. Stereo line in

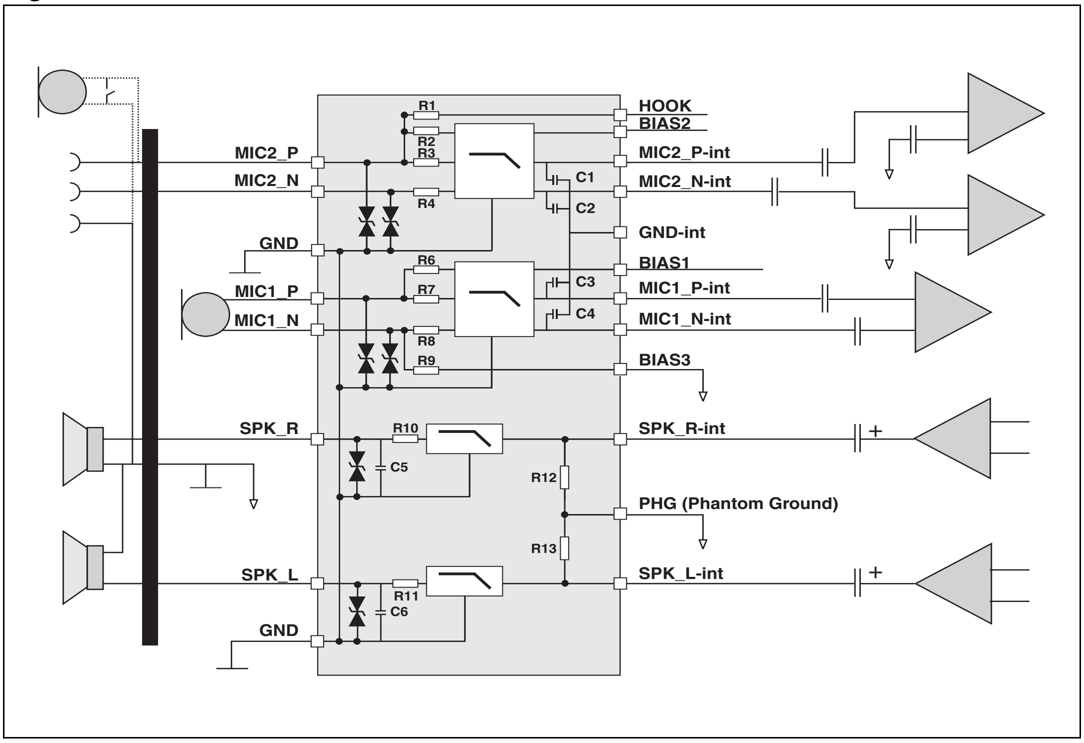


Figure 27. Stereo microphone / line in

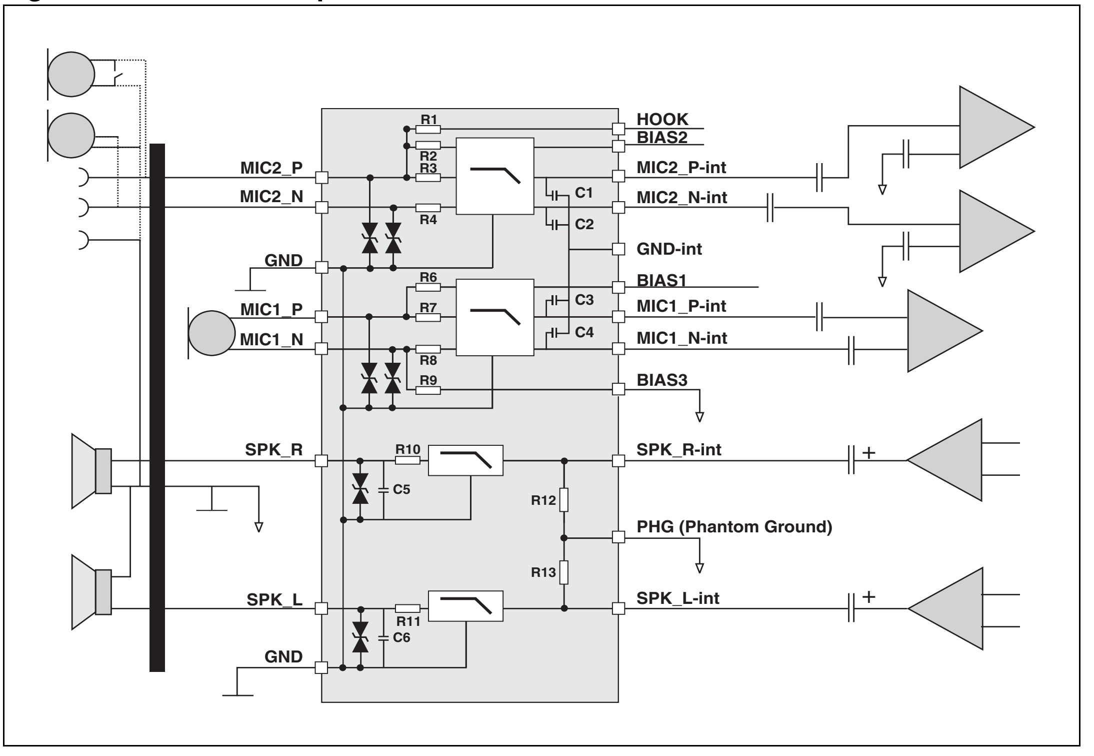
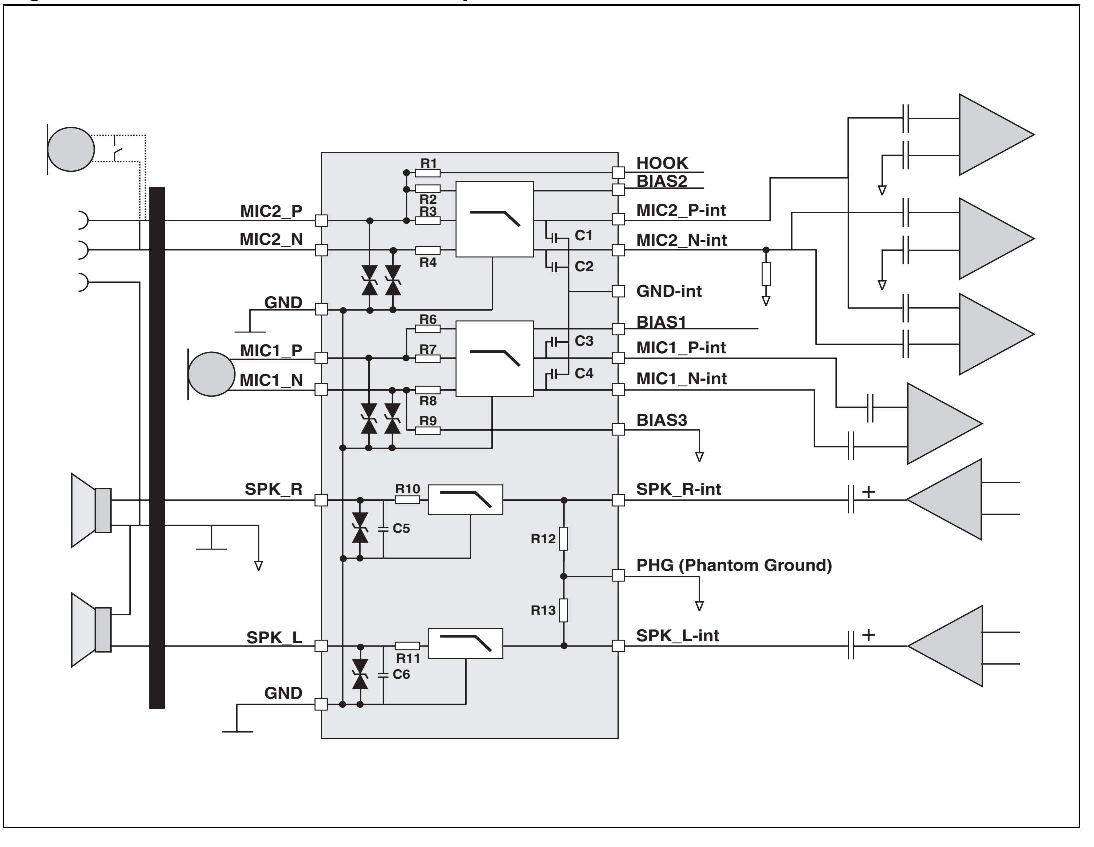
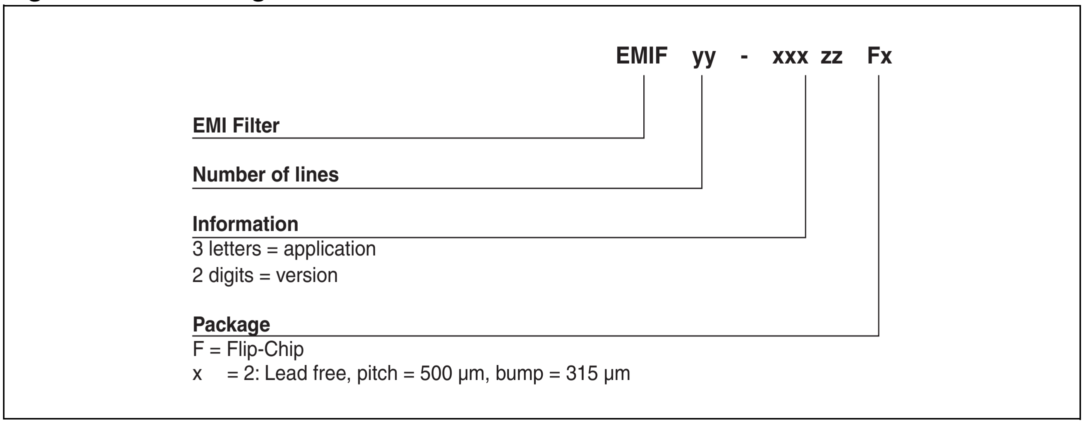


Figure 28. External balanced microphone / stereo line in



3 Ordering information scheme

Figure 29. Ordering information scheme



4 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at *www.st.com*.

Figure 30. Flip chip dimensions

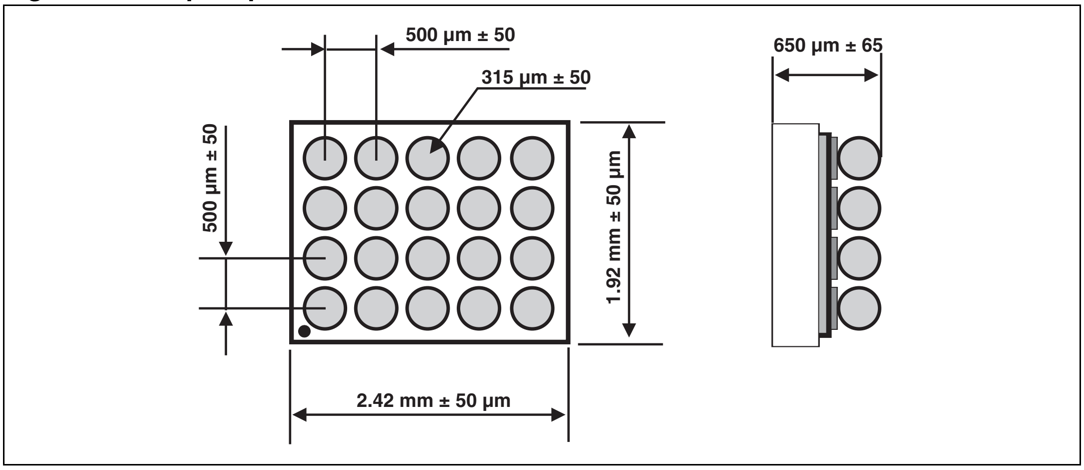


Figure 31. Marking

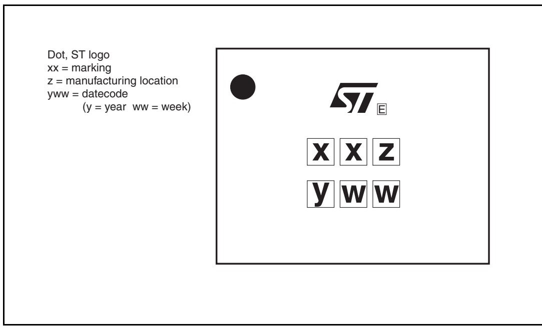


Figure 32. Footprint recommendation

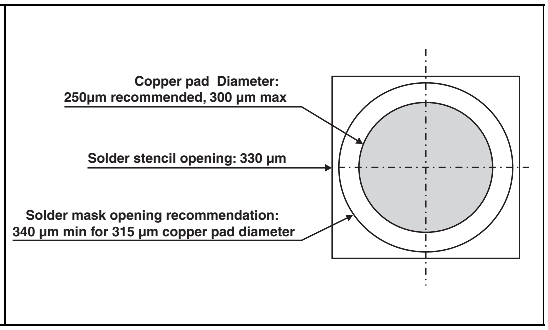
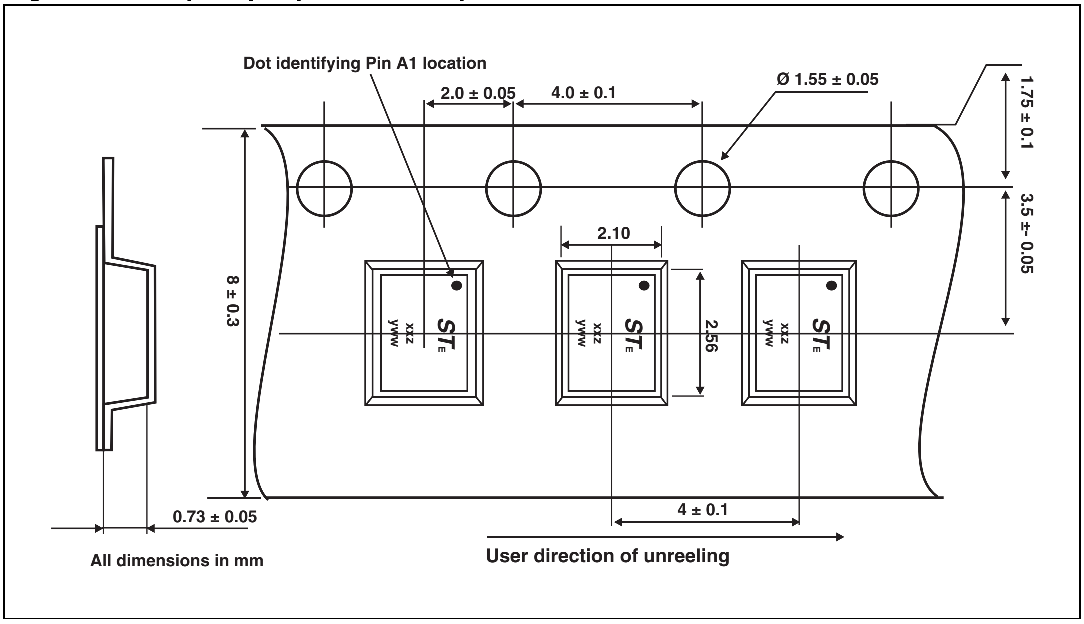


Figure 33. Flip chip tape and reel specification



Note: More packing information is available in the application notes:

AN1235: “Flip chip: Package description and recommendations for use”

AN1751: "EMI Filters: Recommendations and measurements"

5 Ordering information

Table 6. Ordering information

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
EMIF06-AUD01F2	HP	Flip chip	6.45 mg	5000	7” Tape and reel

6 Revision history

Table 7. Document revision history

Date	Revision	Changes
18-Feb-2008	1	First issue