

**FOUR-CHANNEL PCM CODEC**

The  $\mu$ PD9611 incorporates 4-channel A-law/ $\mu$ -law PCM CODECs compliant with ITU-T Recommendation G.711/G.714 and is suitable for applications such as PBX analog subscriber line circuits.

Its gain setting circuit allows transmit/receive gain to be set for 4 channels independently by externally inputting digital signals.

**FEATURES**

- Single-chip CMOS monolithic LSI
- ITU-T Recommendation G.711/G.714 compliant
- Four-channel PCM CODECs integrated on a single chip
- Compatible with A-law and  $\mu$ -law
- Digital gain setting for each channel
  - Transmit : +7.5 to -8.0 dB (0.5 dB step)
  - Receive : 0 to -15.5 dB (0.5 dB step)
- Data transfer system: Transmit/receive synchronization
- Data rate: 2048 kHz
- +5 V single power supply
- Power down function for each channel
- Low power consumption

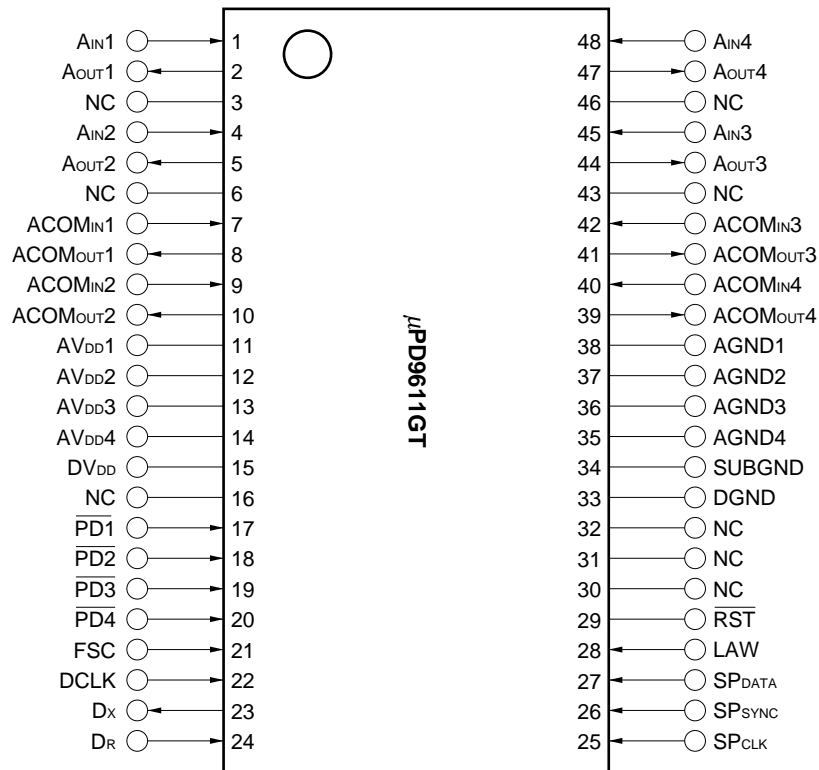
**ORDERING INFORMATION**

Part Number	Package
$\mu$ PD9611GT	48-pin shrink SOP (375 mil)

The information in this document is subject to change without notice.

## PIN CONFIGURATION (Top View)

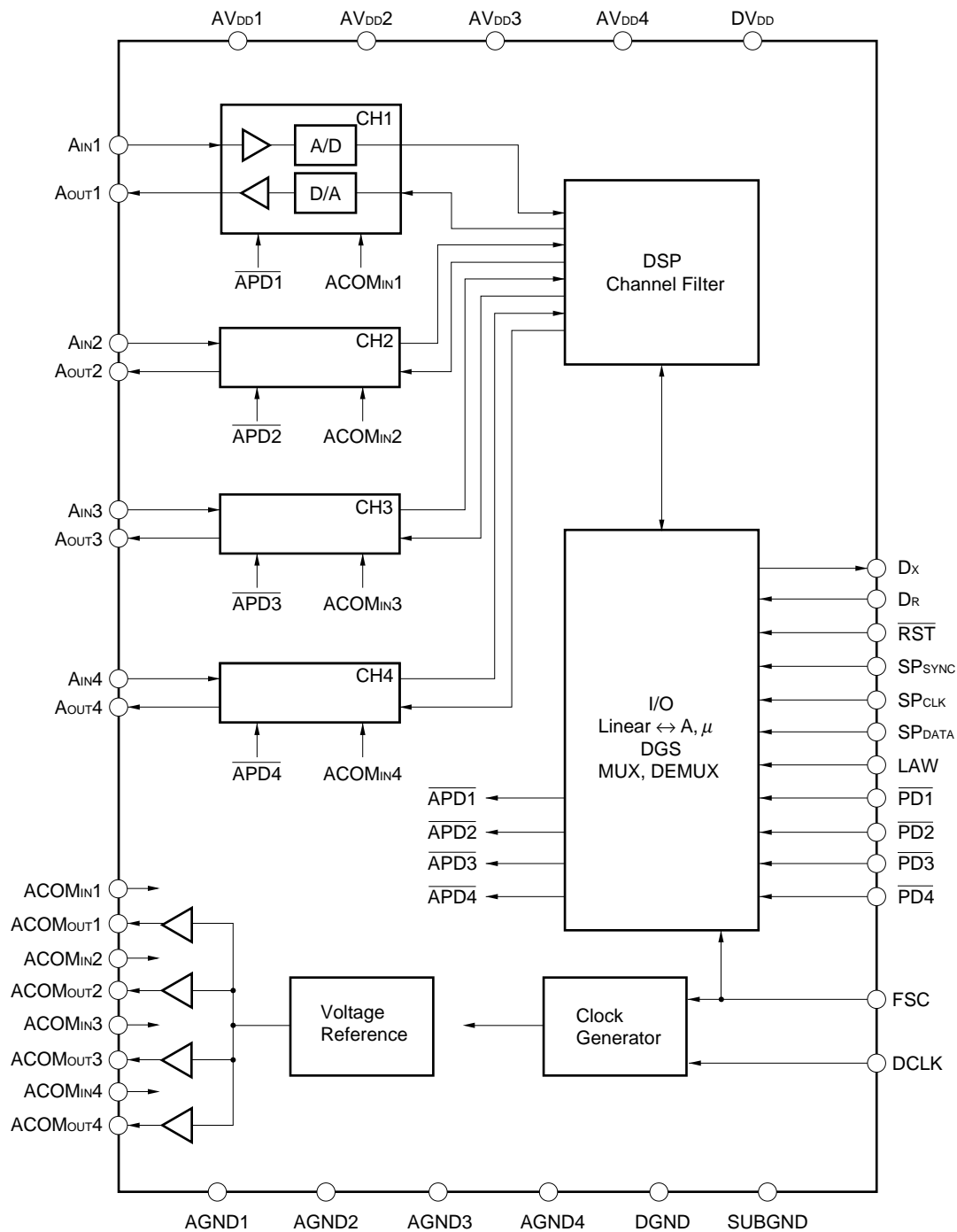
48-pin shrink SOP (375 mil)



ACOM<sub>IN1</sub>-ACOM<sub>IN4</sub> : Analog common voltage in  
 ACOM<sub>OUT1</sub>-ACOM<sub>OUT4</sub> : Analog common voltage out  
 AGND1-AGND4 : Analog ground  
 A<sub>IN1</sub>-A<sub>IN4</sub> : Analog signal in  
 A<sub>OUT1</sub>-A<sub>OUT4</sub> : Analog signal out  
 AV<sub>DD1</sub>-AV<sub>DD4</sub> : Analog power supply  
 DCLK : Data clock in  
 DGND : Digital ground  
 D<sub>R</sub> : Receive PCM data in  
 DV<sub>DD</sub> : Digital power supply

D<sub>X</sub> : Transmit PCM data out  
 FSC : Frame synchronous clock in  
 LAW : A-law/ $\mu$ -law control in  
 NC : No connection  
 PD1-PD4 : Power down control  
 RST : Reset in  
 SP<sub>CLK</sub> : Serial port data clock in  
 SP<sub>DATA</sub> : Serial port data in  
 SP<sub>SYNC</sub> : Serial port synchronous clock in  
 SUBGND : Sub ground

# BLOCK DIAGRAM



## 1. PIN DESCRIPTION

Pin No.	Symbol	I/O	Name and Function
1	A <sub>IN1</sub>	I	Transmit analog input pin for channel 1 When not used, connect to ACOM <sub>OUT1</sub> pin.
2	A <sub>OUT1</sub>	O	Receive analog output pin for channel 1
3	NC	–	Leave this pin open.
4	A <sub>IN2</sub>	I	Receive analog input pin for channel 2 When not used, connect to ACOM <sub>OUT1</sub> pin.
5	A <sub>OUT2</sub>	O	Transmit analog output pin for channel 2
6	NC	–	Leave this pin open.
7	ACOM <sub>IN1</sub>	I	Signal reference voltage input for channel 1
8	ACOM <sub>OUT1</sub>	O	Signal reference voltage output for channel 1
9	ACOM <sub>IN2</sub>	I	Signal reference voltage input for channel 2
10	ACOM <sub>OUT2</sub>	O	Signal reference voltage output for channel 2
11	AV <sub>DD1</sub>	–	Analog power supply pin for channel 1 +5 $\pm$ 0.25 V
12	AV <sub>DD2</sub>	–	Analog power supply pin for channel 2 +5 $\pm$ 0.25 V
13	AV <sub>DD3</sub>	–	Analog power supply pin for channel 3 +5 $\pm$ 0.25 V
14	AV <sub>DD4</sub>	–	Analog power supply pin for channel 4 +5 $\pm$ 0.25 V
15	DV <sub>DD</sub>	–	Digital power supply pin +5 $\pm$ 0.25 V
16	NC	–	Leave this pin open.
17	$\overline{\text{PD1}}$	I	Power-down control input pin for channel 1 Channel 1 enters power-down mode when this signal is low level. The output of Dx pin for channel 1 becomes high-impedance and A <sub>OUT1</sub> becomes signal reference voltage in the power-down mode.
18	$\overline{\text{PD2}}$	I	Power-down control input pin for channel 2 Channel 2 enters power-down mode when this signal is low level. The output of Dx pin for channel 2 becomes high-impedance and A <sub>OUT2</sub> becomes signal reference voltage in the power-down mode.
19	$\overline{\text{PD3}}$	I	Power-down control input pin for channel 3 Channel 3 enters power-down mode when this signal is low level. The output of Dx pin for channel 3 becomes high-impedance and A <sub>OUT3</sub> becomes signal reference voltage in the power-down mode.
20	$\overline{\text{PD4}}$	I	Power-down control input pin for channel 4 Channel 4 enters power-down mode when this signal is low level. The output of Dx pin for channel 4 becomes high-impedance and A <sub>OUT4</sub> becomes signal reference voltage in the power-down mode.
21	FSC	I	Frame synchronous clock input pin (8 kHz)
22	DCLK	I	Data clock input pin (2048 kHz)
23	D <sub>X</sub>	O	Transmit PCM data output pin This pin outputs PCM data for channel 1 to 4 in synchronization with rising edges of DCLK after rising edges of FSC. It becomes high-impedance for other timings.
24	D <sub>R</sub>	I	Receive PCM data input pin This pin inputs PCM data for channel 1 to 4 in synchronization with falling edges of DCLK after rising edges of FSC.
25	SP <sub>CLK</sub>	I	Setting data clock input pin
26	SP <sub>SYNC</sub>	I	Setting synchronous clock input pin
27	SP <sub>DATA</sub>	I	Setting data input pin

Pin No.	Symbol	I/O	Name and Function
28	LAW	I	A-law/ $\mu$ -law select pin in common to four channels L: A-law, H: $\mu$ -law
29	$\overline{\text{RST}}$	–	Reset input, power-on reset pin H: normal operation L: internal registers are in the default status.
30-32	NC	–	Leave this pin open.
33	DGND	–	Digital ground pin
34	SUBGND	–	Substrate ground pin
35	AGND4	–	Analog ground pin for channel 4
36	AGND3	–	Analog ground pin for channel 3
37	AGND2	–	Analog ground pin for channel 2
38	AGND1	–	Analog ground pin for channel 1
39	ACOM <sub>OUT4</sub>	O	Signal reference voltage output for channel 4
40	ACOM <sub>IN4</sub>	I	Signal reference voltage input for channel 4
41	ACOM <sub>OUT3</sub>	O	Signal reference voltage output for channel 3
42	ACOM <sub>IN3</sub>	I	Signal reference voltage input for channel 3
43	NC	–	Leave this pin open.
44	A <sub>OUT3</sub>	O	Receive analog output pin for channel 3
45	A <sub>IN3</sub>	I	Transmit analog input pin for channel 3 When not used, connect to ACOM <sub>OUT1</sub> pin.
46	NC	–	Leave this pin open.
47	A <sub>OUT4</sub>	O	Receive analog output pin for channel 4
48	A <sub>IN4</sub>	I	Transmit analog input pin for channel 4 When not used, connect to ACOM <sub>OUT1</sub> pin.

## 2. CAUTIONS ON USE

### (1) Absolute maximum ratings

Application of voltage or current in excess of the absolute maximum ratings to the  $\mu$ PD9611 may result in damage due to latch up, etc. Be especially cautious about power supply noise, etc.

### (2) Wiring pattern

The design of the ground pattern is extremely important for operating the  $\mu$ PD9611 with high precision. Connect the analog ground pins (AGND1 to AGND4), digital ground pin (DGND) and substrate ground pin (SUBGND) close to the IC pins, and connect to a wide analog ground line on the board.

### (3) Addition of bypass capacitors for power supply pins

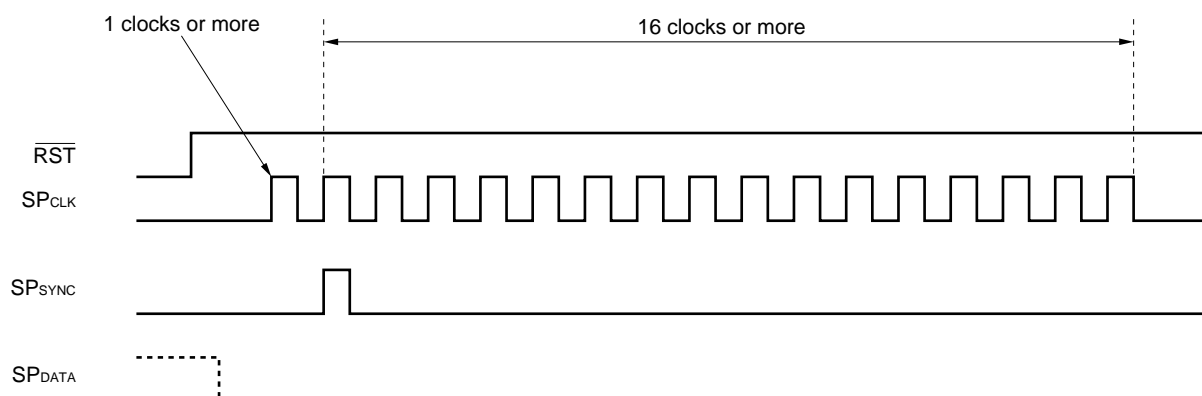
Because the  $\mu$ PD9611 uses many internal high-frequency operational amplifiers, high power supply impedance can cause instability (such as oscillation) in these internal operational amplifiers. To suppress such instability and eliminate power supply noise, connect all power supply pins (AV<sub>DD</sub>1 to AV<sub>DD</sub>4, DV<sub>DD</sub>) close to the IC pins, and put bypass capacitors ( $C_{VDD}$  = approximately 0.1  $\mu$ F) having superior high-frequency characteristics very close to the pins.

### (4) Addition of bypass capacitors for ACOM pins

The  $\mu$ PD9611 incorporates reference voltages for signal sources. Superposing of noise on these reference voltages may have adverse effects on transmission characteristics, etc. Therefore, connect the ACOM<sub>OUT</sub> pin and ACOM<sub>IN</sub> pin close to the IC pins, and put bypass capacitors ( $C_{ACOM}$  = approximately 0.1  $\mu$ F) having superior high-frequency characteristics very close to the pins.

### (5) Control or SP<sub>DATA</sub> pin on reset

When inputting the setting data from the SP<sub>DATA</sub> pin after the  $\mu$ PD9611 is reset, first input the following patterns to reset to 0 the counter used to fetch data from the SP<sub>DATA</sub> pin.



After the  $\overline{RST}$  pin has been set to the high level, input 1 clock or more to the SP<sub>CLK</sub> pin, set the SP<sub>SYNC</sub> pin to the high level and input 16 clocks more to the SP<sub>CLK</sub> pin.

During this operation, the SP<sub>DATA</sub> pin is held at the low level. Afterwards, input the setting data.

### 3. GENERAL OPERATION

#### (1) PCM data transfer

In the transmit section, if FSC pin is set to the high level in synchronization with the rising edge ( $\uparrow$ ) of the data clock applied to the DCLK pin, the D<sub>x</sub> pin becomes active and sign bit data (MSB) of channel 1 is output. The following data of 7 bits is clocked out in synchronization with the rising edge ( $\uparrow$ ) of each data clock. Sign bit data (MSB) of channel 2 is output in synchronization with the rising edge ( $\uparrow$ ) of the 9th data clock. In the same manner, each data up to channel 4 is output and the rising edge ( $\uparrow$ ) of the 33rd data clock then sets the D<sub>x</sub> pin to high-impedance state.

Similarly, in the receive section, if the FSC pin is set to the high level in synchronization with the rising edge ( $\uparrow$ ) of the data clock applied to the DCLK pin, data of D<sub>R</sub> pin is latched by the falling edges ( $\downarrow$ ) of the data clock and consecutively clocked in.

#### (2) Power down control

The  $\mu$ PD9611 has the following two methods for power down control and is able to control power-down independently for each channel.

- Sets pins  $\overline{\text{PD1}}$  to  $\overline{\text{PD4}}$  to high or low level.
- Inputs 8-bit setting data from SP<sub>DATA</sub> pin (see **(5) Control of SP<sub>DATA</sub> pin**).

Internal data is the logical sum of  $\overline{\text{PD1}}$  to  $\overline{\text{PD4}}$  pin state and 8-bit setting data input.

If the internal data is 0, the channel enters the power-down state. If the internal data is 1, the channel enters the power-up state. In the power down state, PCM data in the channel goes to high-impedance state and analog output becomes the signal reference voltage level.

8-Bit Setting Data (Channel 1)	$\overline{\text{PD1}}$ Pin	Internal Data
0	0	0
1	0	1
0	1	1
1	1	1

**Remarks** 1. 0: Power down, 1: Power up  
2. The settings are the same for channel 2 to channel 4.

### (3) A-law/μ-law control

The μPD9611 has the following two methods for A-law/μ-law control.

- Sets LAW pin to high or low level.
- Inputs 8-bit setting data from SP<sub>DATA</sub> pin (see **(5) Control of SP<sub>DATA</sub> pin**).

Internal data is the logical sum of LAW pin state and 8-bit setting data input.

If the internal data is 0, the μPD9611 enters A-law mode. If the internal data is 1, the μPD9611 enters μ-law mode.

8-Bit Setting Data	LAW Pin	Internal Data
0	0	0
1	0	1
0	1	1
1	1	1

**Remark** 0: A-law, 1: μ-law

### (4) Gain Setting control for transmit/receive

The μPD9611 can control gain settings independently for the transmit/receive by inputting 8-bit setting data (see **(5) Control of SP<sub>DATA</sub> pin**) from the SP<sub>DATA</sub> pin for four channels. Gain can be set from +7.5 to −8.0 dB for the transmit and +0.0 dB to −15.5 dB for the receive in 0.5 dB steps.

8-bit setting data input from SP<sub>DATA</sub> pin specifies the channel set in the first 8 bits, and performs selection of transmit/receive and gain setting in the second 8 bits.



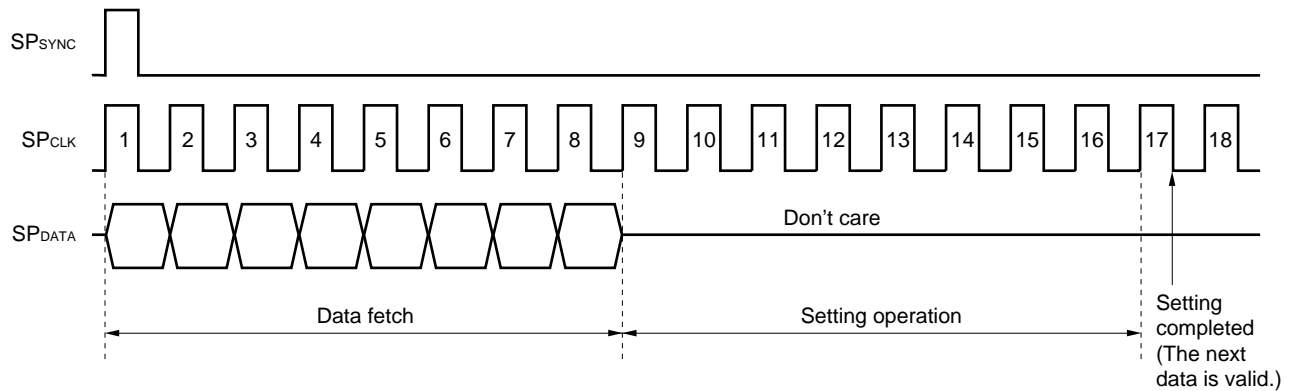
**(5) Control of SP<sub>DATA</sub> pin**

If SP<sub>SYNC</sub> pin is set to the high level in synchronization with the rising edge ( $\uparrow$ ) of the data clock applied to the SP<sub>CLK</sub> pin, data of the SP<sub>DATA</sub> pin is latched by the falling edge ( $\downarrow$ ) of the data clock and consecutively fetched in.

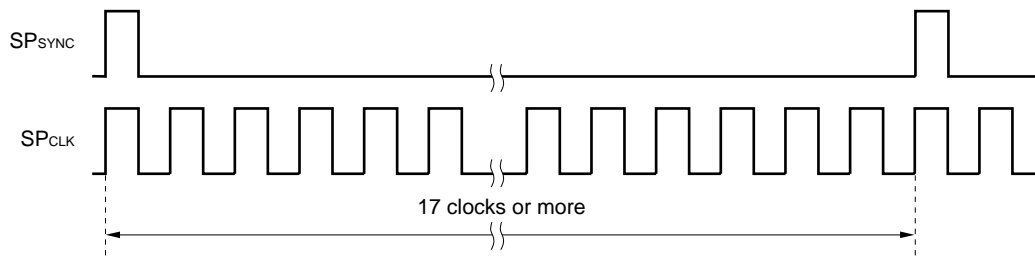
After the 8-bit data has been fetched, the setting operation is performed according to the data.

This setting operation is performed during the 8 clocks after fetching the data and the next data is valid at the 17th clock.

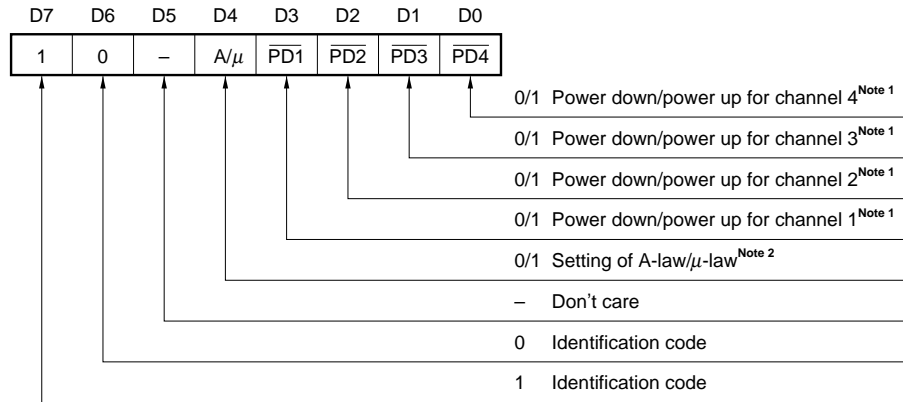
Therefore, when setting 1 word (8 bits) of data, input 17 clocks or more to the SP<sub>CLK</sub> pin.



Ensure that 17 clocks or more are input to the SP<sub>CLK</sub> pin between the rising of SP<sub>SYNC</sub> and the rising of the next SP<sub>SYNC</sub>.

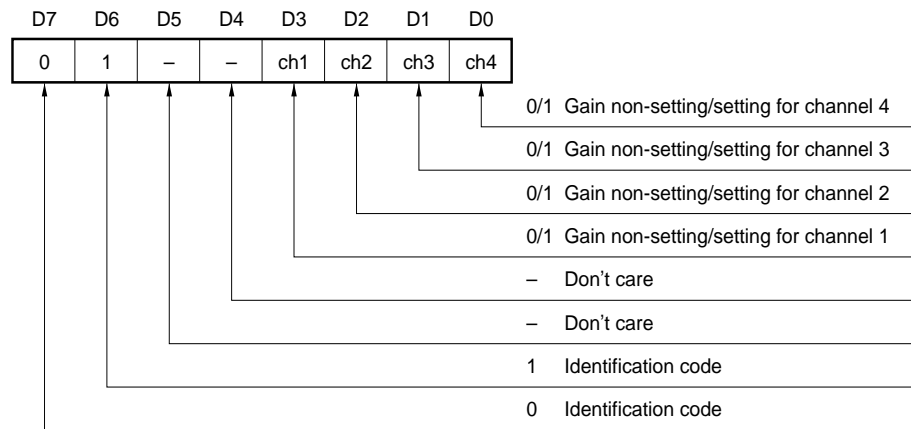


- A/ $\mu$ -law, power down control



- Notes** 1. Default setting is power down mode.  
 2. Default setting is A-law mode.

- Transmit/receive gain setting control (1st word)



**Transmit/receive gain setting control (2nd word)**

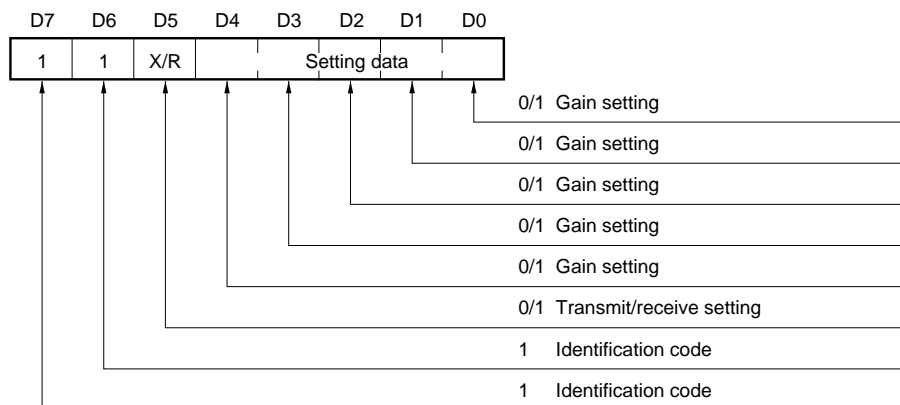


Table of Gain Setting Codes

(1/2)

Setting Item	Setting Level	1st Word								2nd Word							
		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Gain setting for transmit	+7.5 dB	0	1	–	–	ch1	ch2	ch3	ch4	1	1	0	1	0	0	0	0
	+7.0 dB									1	1	0	1	0	0	0	1
	+6.5 dB									1	1	0	1	0	0	1	0
	+6.0 dB									1	1	0	1	0	0	1	1
	+5.5 dB									1	1	0	1	0	1	0	0
	+5.0 dB									1	1	0	1	0	1	0	1
	+4.5 dB									1	1	0	1	0	1	1	0
	+4.0 dB									1	1	0	1	0	1	1	1
	+3.5 dB									1	1	0	1	1	0	0	0
	+3.0 dB									1	1	0	1	1	0	0	1
	+2.5 dB									1	1	0	1	1	0	1	0
	+2.0 dB									1	1	0	1	1	0	1	1
	+1.5 dB									1	1	0	1	1	1	0	0
	+1.0 dB									1	1	0	1	1	1	0	1
	+0.5 dB									1	1	0	1	1	1	1	0
	0.0 dB <sup>Note</sup>									1	1	0	1	1	1	1	1
	–0.5 dB									1	1	0	0	0	0	0	0
	–1.0 dB									1	1	0	0	0	0	0	1
	–1.5 dB									1	1	0	0	0	0	1	0
	–2.0 dB									1	1	0	0	0	0	1	1
	–2.5 dB									1	1	0	0	0	1	0	0
	–3.0 dB									1	1	0	0	0	1	0	1
	–3.5 dB									1	1	0	0	0	1	1	0
	–4.0 dB									1	1	0	0	0	1	1	1
	–4.5 dB									1	1	0	0	1	0	0	0
	–5.0 dB									1	1	0	0	1	0	0	1
	–5.5 dB									1	1	0	0	1	0	1	0
	–6.0 dB									1	1	0	0	1	0	1	1
	–6.5 dB									1	1	0	0	1	1	0	0
	–7.0 dB									1	1	0	0	1	1	0	1
	–7.5 dB									1	1	0	0	1	1	1	0
	–8.0 dB									1	1	0	0	1	1	1	1

**Note** Default setting

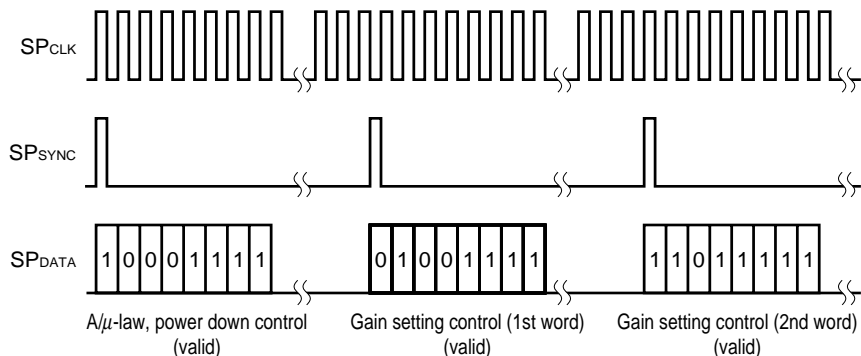
(2/2)

Setting Item	Setting Level	1st Word								2nd Word							
		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Gain setting for receive	0.0 dB <sup>Note</sup>	0	1	–	–	ch1	ch2	ch3	ch4	1	1	1	1	1	1	1	1
	–0.5 dB									1	1	1	1	1	1	1	0
	–1.0 dB									1	1	1	1	1	1	0	1
	–1.5 dB									1	1	1	1	1	1	0	0
	–2.0 dB									1	1	1	1	1	0	1	1
	–2.5 dB									1	1	1	1	1	0	1	0
	–3.0 dB									1	1	1	1	1	0	0	1
	–3.5 dB									1	1	1	1	1	0	0	0
	–4.0 dB									1	1	1	1	0	1	1	1
	–4.5 dB									1	1	1	1	0	1	1	0
	–5.0 dB									1	1	1	1	0	1	0	1
	–5.5 dB									1	1	1	1	0	1	0	0
	–6.0 dB									1	1	1	1	0	0	1	1
	–6.5 dB									1	1	1	1	0	0	1	0
	–7.0 dB									1	1	1	1	0	0	0	1
	–7.5 dB									1	1	1	1	0	0	0	0
	–8.0 dB									1	1	1	0	1	1	1	1
	–8.5 dB									1	1	1	0	1	1	1	0
	–9.0 dB									1	1	1	0	1	1	0	1
	–9.5 dB									1	1	1	0	1	1	0	0
	–10.0 dB									1	1	1	0	1	0	1	1
	–10.5 dB									1	1	1	0	1	0	1	0
	–11.0 dB									1	1	1	0	1	0	0	1
	–11.5 dB									1	1	1	0	1	0	0	0
	–12.0 dB									1	1	1	0	0	1	1	1
	–12.5 dB									1	1	1	0	0	1	1	0
	–13.0 dB									1	1	1	0	0	1	0	1
	–13.5 dB									1	1	1	0	0	1	0	0
	–14.0 dB									1	1	1	0	0	0	1	1
	–14.5 dB									1	1	1	0	0	0	1	0
	–15.0 dB									1	1	1	0	0	0	0	1
	–15.5 dB									1	1	1	0	0	0	0	0

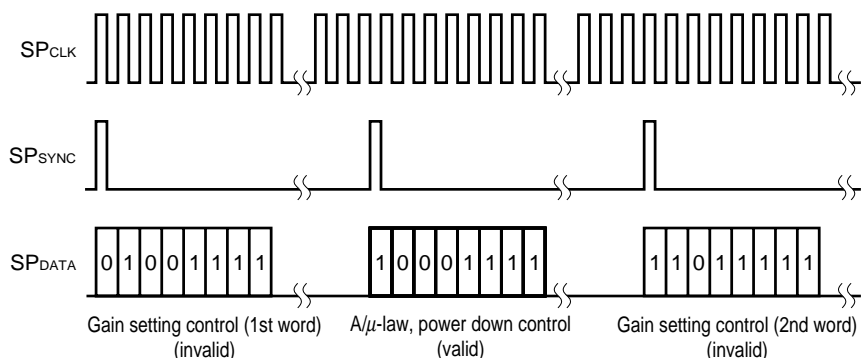
**Note** Default setting

Gain setting control is set by inputting 8-bit data to the 1st word first and inputting 8-bit data of the 2nd word in synchronization with the next rising edge of SP<sub>SYNC</sub>. However, if data other than the identification code of the 2nd word is input after the input of the 1st word, the contents of the 1st word are ignored.

(i) When gain setting control is valid

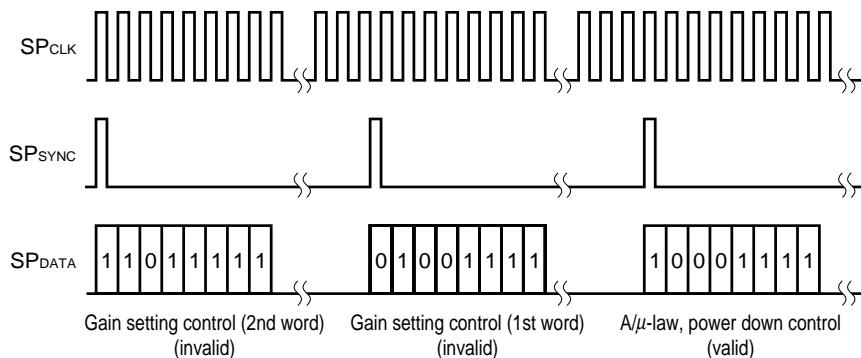


(ii) When gain setting control is invalid –1



**Remark** Because A/μ-law, power down control is input after input of gain setting control (1st word), gain setting control (1st word) becomes invalid and gain setting control (2nd word) also becomes invalid.

(iii) When gain setting control is invalid –2



**Remark** Because gain setting control (2nd word) is input before gain setting control (1st word), gain setting control (1st word) becomes invalid. Then, because A/μ-law, power down control is input even if gain setting control (1st word) is input, gain setting control (1st word) becomes invalid.

#### 4. ELECTRICAL SPECIFICATIONS (PRELIMINARY)

##### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25 °C)

Item	Symbol	Condition	Rating	Unit
Supply voltage	V <sub>DD</sub>	AV <sub>DD1</sub> , AV <sub>DD2</sub> , AV <sub>DD3</sub> , AV <sub>DD4</sub> , DV <sub>DD</sub>	−0.3 to +7.0	V
Analog input voltage	V <sub>AIN</sub>	A <sub>IN1</sub> , A <sub>IN2</sub> , A <sub>IN3</sub> , A <sub>IN4</sub> , ACOM <sub>IN1</sub> , ACOM <sub>IN2</sub> , ACOM <sub>IN3</sub> , ACOM <sub>IN4</sub>	−0.3 to V <sub>DD</sub> +0.3	
Digital input voltage	V <sub>DIN</sub>	D <sub>R</sub> , DCLR, FSC, LAW, $\overline{\text{PD1}}$ , $\overline{\text{PD2}}$ , $\overline{\text{PD3}}$ , $\overline{\text{PD4}}$ , SP <sub>CLK</sub> , SP <sub>SYNC</sub> , SP <sub>DATA</sub> , $\overline{\text{RST}}$	−0.3 to V <sub>DD</sub> +0.3	
Voltage applied to analog output pin	V <sub>AOUT</sub>	A <sub>OUT1</sub> , A <sub>OUT2</sub> , A <sub>OUT3</sub> , A <sub>OUT4</sub> , ACOM <sub>OUT1</sub> , ACOM <sub>OUT2</sub> , ACOM <sub>OUT3</sub> , ACOM <sub>OUT4</sub>	−0.3 to V <sub>DD</sub> +0.3	
Voltage applied to digital output pin	V <sub>DOUT</sub>	D <sub>X</sub>	−0.3 to V <sub>DD</sub> +0.3	
Power dissipation	P <sub>T</sub>		500	mW
Ambient operating temperature	T <sub>A</sub>		−20 to +85	°C
Storage temperature	T <sub>stg</sub>		−65 to +150	

**Caution** Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter or even momentarily. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.

##### RECOMMENDED OPERATION CONDITIONS (T<sub>A</sub> = −20 to +85 °C, V<sub>DD</sub> = 5 V ± 5 %, GND = 0 V, f<sub>DCLK</sub> = 2048 kHz)

###### (1) DC condition

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Ambient operating temperature	T <sub>A</sub>		−20	+25	+85	°C
Supply voltage	V <sub>DD</sub>	AV <sub>DD1</sub> , AV <sub>DD2</sub> , AV <sub>DD3</sub> , AV <sub>DD4</sub> , DV <sub>DD</sub>	4.75	5.0	5.25	V
Analog input voltage	V <sub>AI</sub>	A <sub>IN1</sub> , A <sub>IN2</sub> , A <sub>IN3</sub> , A <sub>IN4</sub> (ACOM as reference)	−1.0		+1.0	
Analog output load resistance	R <sub>LOAD</sub>	A <sub>OUT1</sub> , A <sub>OUT2</sub> , A <sub>OUT3</sub> , A <sub>OUT4</sub>	50			kΩ
Analog output load capacitance	C <sub>LOAD</sub>				50	pF
High level input voltage	V <sub>IH1</sub>	D <sub>R</sub> , DCLK, FSC, LAW, $\overline{\text{PD1}}$ , $\overline{\text{PD2}}$ , $\overline{\text{PD3}}$ , $\overline{\text{PD4}}$ , SP <sub>CLK</sub> , SP <sub>SYNC</sub> , SP <sub>DATA</sub>	2.0		V <sub>DD</sub>	V
	V <sub>IH2</sub>	$\overline{\text{RST}}$	0.8×V <sub>DD</sub>		V <sub>DD</sub>	
Low level input voltage	V <sub>IL1</sub>	D <sub>R</sub> , DCLK, FSC, LAW, $\overline{\text{PD1}}$ , $\overline{\text{PD2}}$ , $\overline{\text{PD3}}$ , $\overline{\text{PD4}}$ , SP <sub>CLK</sub> , SP <sub>SYNC</sub> , SP <sub>DATA</sub>	0		0.8	
	V <sub>IL2</sub>	$\overline{\text{RST}}$	0		0.2×V <sub>DD</sub>	

## (2) AC condition

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Data clock frequency	f <sub>CLK</sub>	(= 1/t <sub>cy</sub> ) $\pm 50$ ppm		2048		kHz
Data clock pulse width	t <sub>CLK</sub>		200			ns
Frame synchronous clock frequency	f <sub>s</sub>	$\pm 50$ ppm		8.0		kHz
High level frame synchronous pulse width	t <sub>WHS</sub>		200			ns
Low level frame synchronous pulse width	t <sub>WLS</sub>		8			$\mu$ s
Clock rise time	t <sub>r</sub>				50	ns
Clock fall time	t <sub>f</sub>				50	ns
Float in synchronous timing	t <sub>CSD1</sub>				100	ns
	t <sub>CSD2</sub>		40			ns
Frame synchronous clock and data clock high level width	t <sub>WHSC</sub>		100			ns
D <sub>R</sub> setup time	t <sub>DSR</sub>	<b>Note</b>	65			ns
D <sub>R</sub> hold time	t <sub>DHR</sub>	<b>Note</b>	120			ns
SP <sub>DATA</sub> clock frequency	f <sub>SPCLK</sub>				2048	kHz
SP <sub>DATA</sub> setup time	t <sub>GSR</sub>	<b>Note</b>	100			ns
SP <sub>DATA</sub> hold time	t <sub>GHR</sub>	<b>Note</b>	100			ns
Float in SP synchronous timing	t <sub>FSD</sub>		40			ns

**Note** Set the rise time and fall time of the digital input waveform and clock signal used for measuring timings to 5 ns.

**DC CHARACTERISTICS**(T<sub>A</sub> = -20 to +85 °C, V<sub>DD</sub> = 5 ± 0.25 V, GND = 0 V, f<sub>DCLK</sub> = 2048 kHz, and all output pins are unloaded.)**(1) Power consumption**

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Circuit current	I <sub>DD</sub>	All channels in normal operation		23	30	mA
Power-down circuit current	I <sub>DDPD</sub>	All channels in power-down mode		5	6	

**(2) Digital interface**

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Digital input current	I <sub>ID</sub>	D <sub>R</sub> , DCLK, FSC, LAW, $\overline{\text{PD1}}$ , $\overline{\text{PD2}}$ , $\overline{\text{PD3}}$ , $\overline{\text{PD4}}$ , SP <sub>CLK</sub> , SP <sub>SYNC</sub> , SP <sub>DATA</sub> , $\overline{\text{RST}}$ Each pin 0 ≤ V <sub>DIN</sub> ≤ V <sub>DD</sub>	-10		+10	μA
3-state leakage current	I <sub>L</sub>	D <sub>x</sub> pin 0 ≤ V <sub>DIN</sub> ≤ V <sub>DD</sub>	-10		+10	
High level output voltage	V <sub>OH</sub>	D <sub>x</sub> pin I <sub>OH</sub> = -150 μA	V <sub>DD</sub> -0.3			V
Low level output voltage	V <sub>OL</sub>	D <sub>x</sub> pin I <sub>OL</sub> = 0.8 mA			0.4	
Digital output pin output capacitance	C <sub>OD</sub>	f = 1 MHz, 0 V other than unmeasured pins			15	pF
Digital input pin input capacitance	C <sub>ID</sub>	f = 1 MHz, 0 V other than unmeasured pins			10	

**(3) Transmit amplifier (A<sub>IN1</sub>, A<sub>IN2</sub>, A<sub>IN3</sub>, A<sub>IN4</sub> pins)**

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input bias current	I <sub>B</sub>		-10		+10	μA
Input resistance	R <sub>IN</sub>		1			MΩ
Input capacitance	C <sub>IN</sub>				10	pF

**(4) Receive power amplifier (A<sub>OUT1</sub>, A<sub>OUT2</sub>, A<sub>OUT3</sub>, A<sub>OUT4</sub> pins)**

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output offset voltage	V <sub>OA</sub>	D <sub>R</sub> = +0 code ACOM as reference	-50		+50	mV
Maximum output voltage	V <sub>OM</sub>	ACOM as reference	-1.02		+1.02	V
Output resistance	R <sub>OUT</sub>			1		Ω

**(5) Signal reference voltage output (ACOM<sub>OUT1</sub>, ACOM<sub>OUT2</sub>, ACOM<sub>OUT3</sub>, ACOM<sub>OUT4</sub> pins)**

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output voltage	V <sub>ACOM</sub>		2.35	2.4	2.45	V



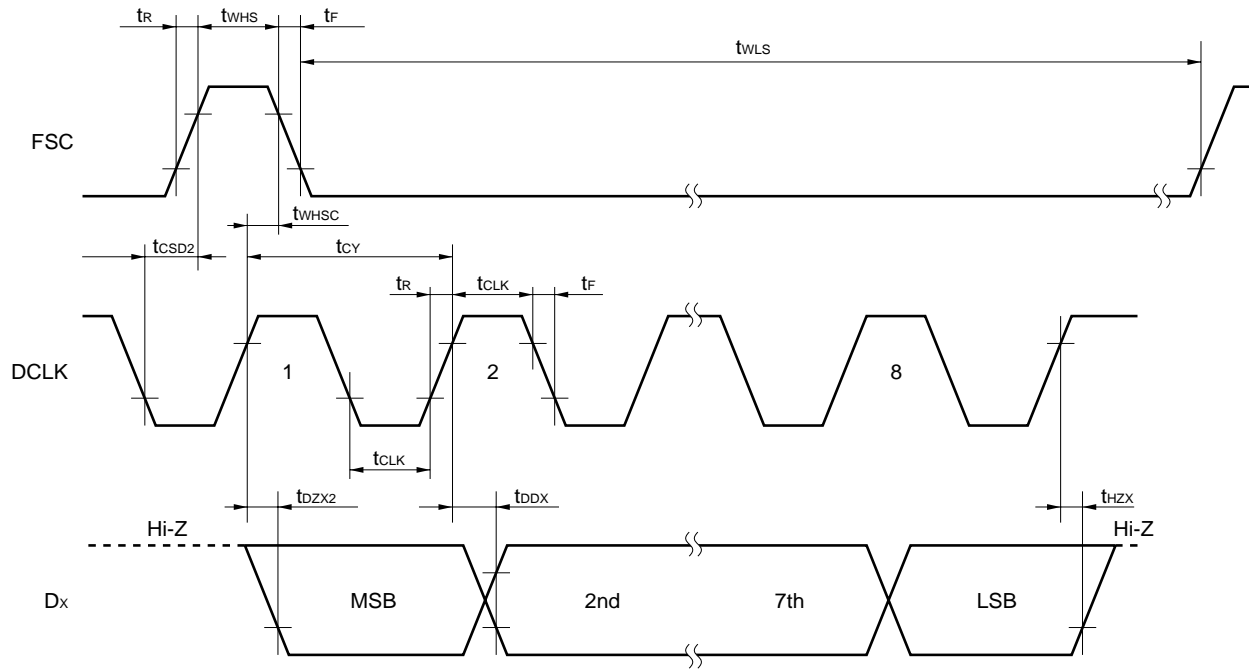
**AC CHARACTERISTICS ( $T_A = -20$  to  $+85$  °C,  $V_{DD} = 5 \pm 0.25$  V, GND = 0 V,  $f_{DCLK} = 2048$  kHz)**

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Data enable delay time	$t_{DZX1}$	Dx when FSC is behind DCLK			100	ns
	$t_{DZX2}$	Dx when FSC is ahead of DCLK			100	ns
Data delay time	$t_{DDX}$	Dx pin			100	ns
Data hold time	$t_{HZX}$	Dx pin		25		ns

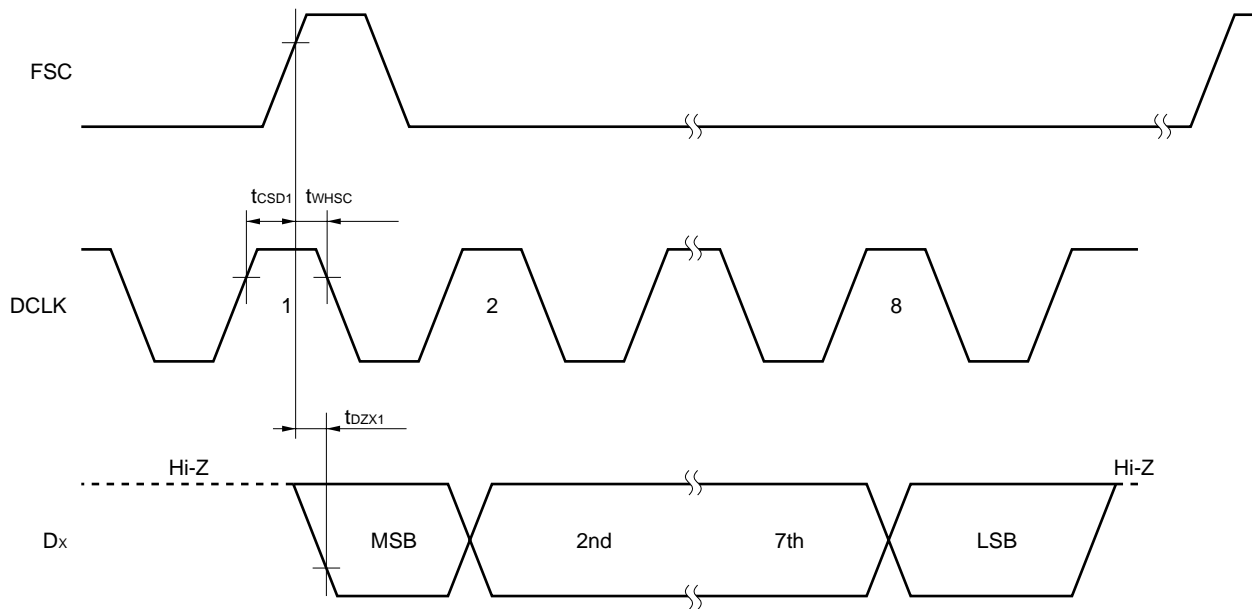
## TIMING CHARTS

## (1) Transmit timing

## (a) When FSC is ahead of DCLK

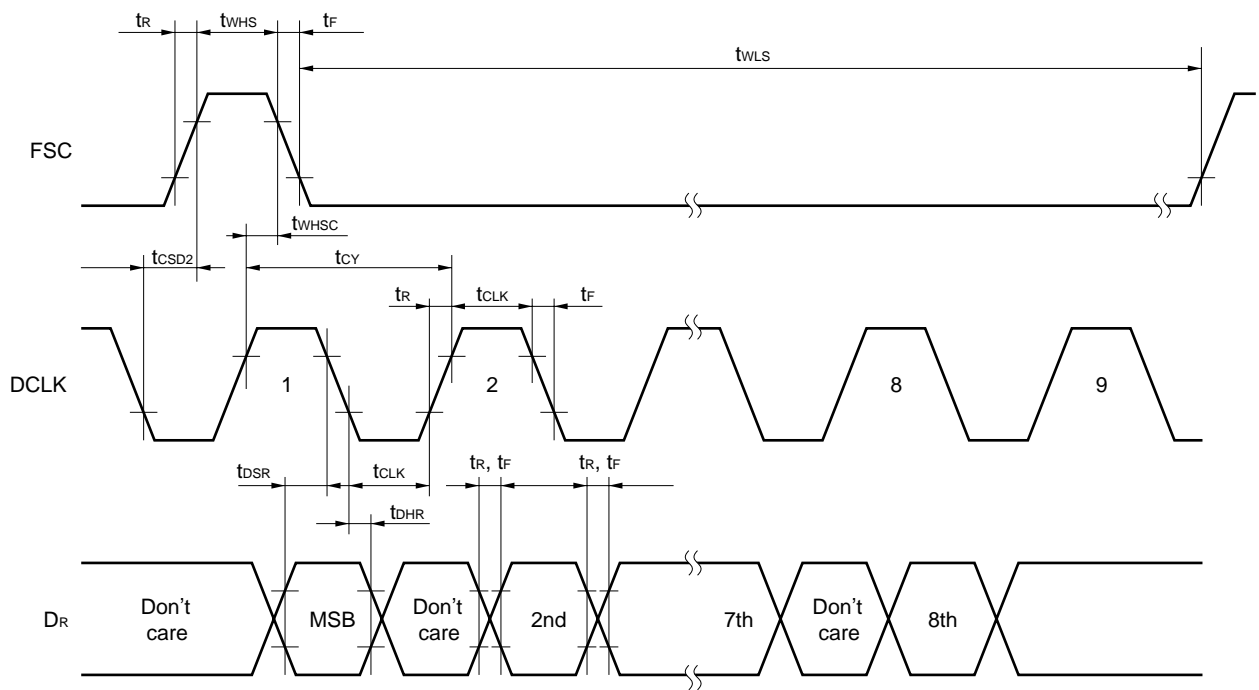


## (b) When FSC is behind DCLK

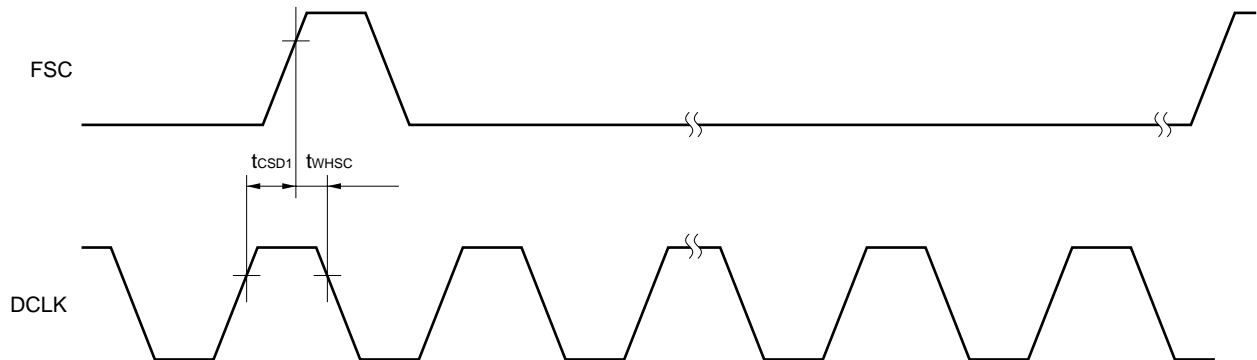


## (2) Receive timing

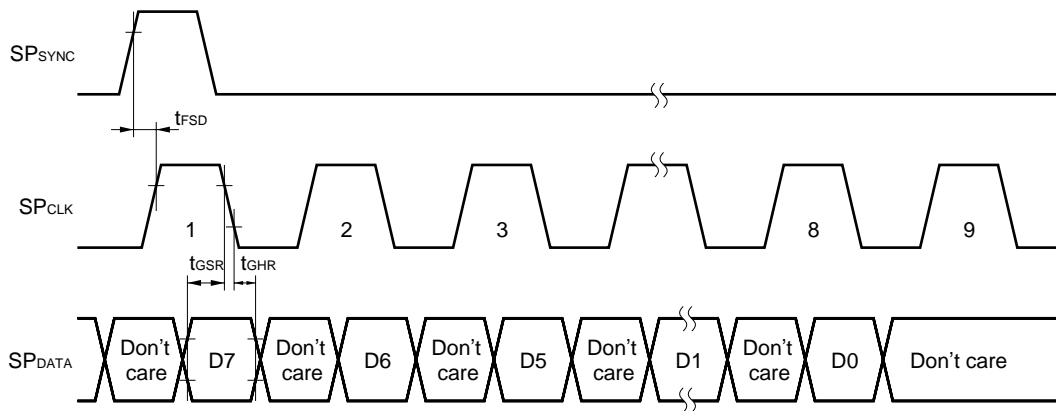
### (a) When FSC is ahead of DCLK



### (b) When FSC is behind DCLK

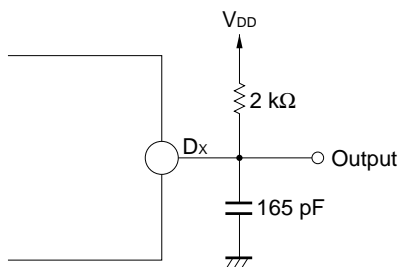


### (3) Gain setting timing

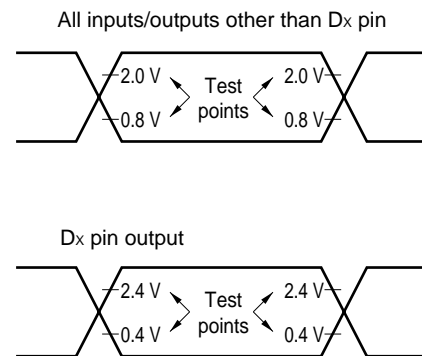


**Remark** The relationship between SP<sub>SYNC</sub> and SP<sub>CLK</sub> is the same as in the receive timing.

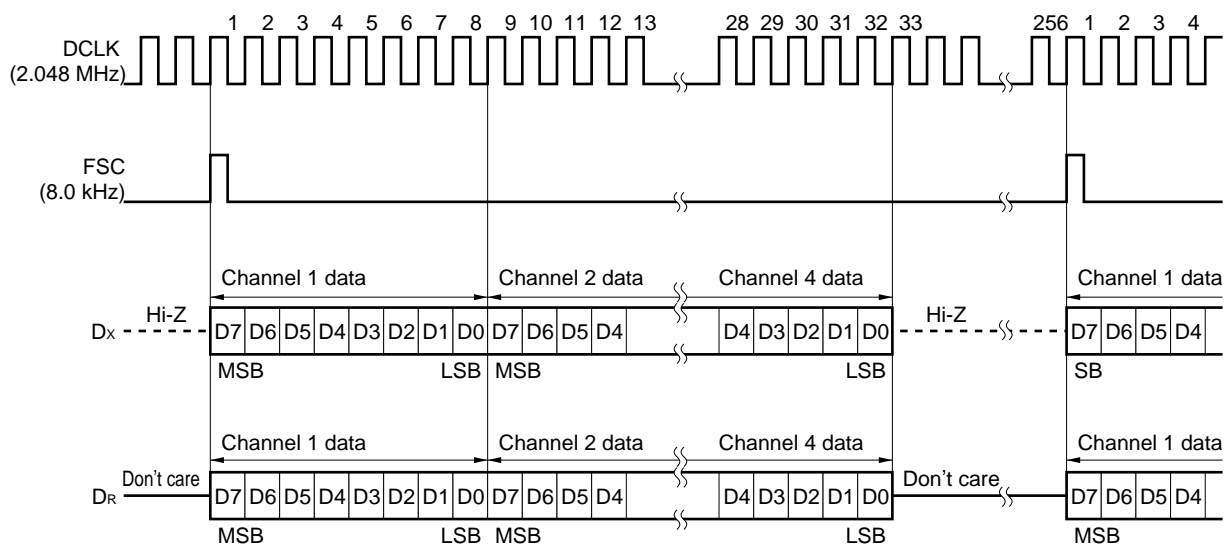
#### Dx output measuring circuit



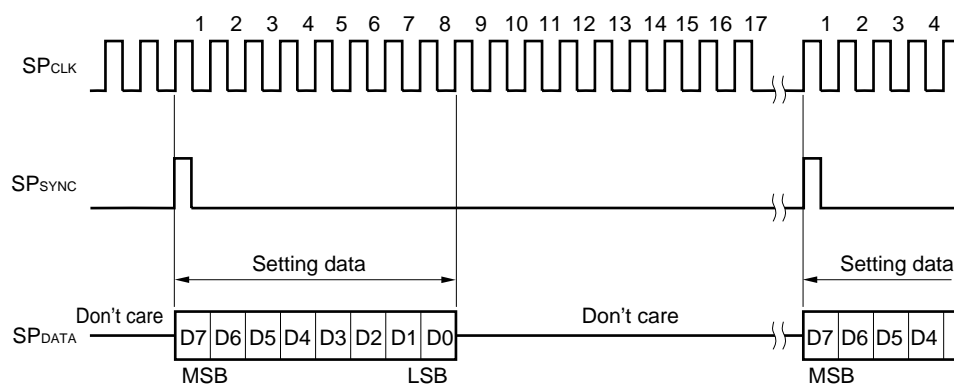
#### Timing test waveform



### (4) Transmit, receive PCM data input/output timing charts



## (5) Setting data input timing



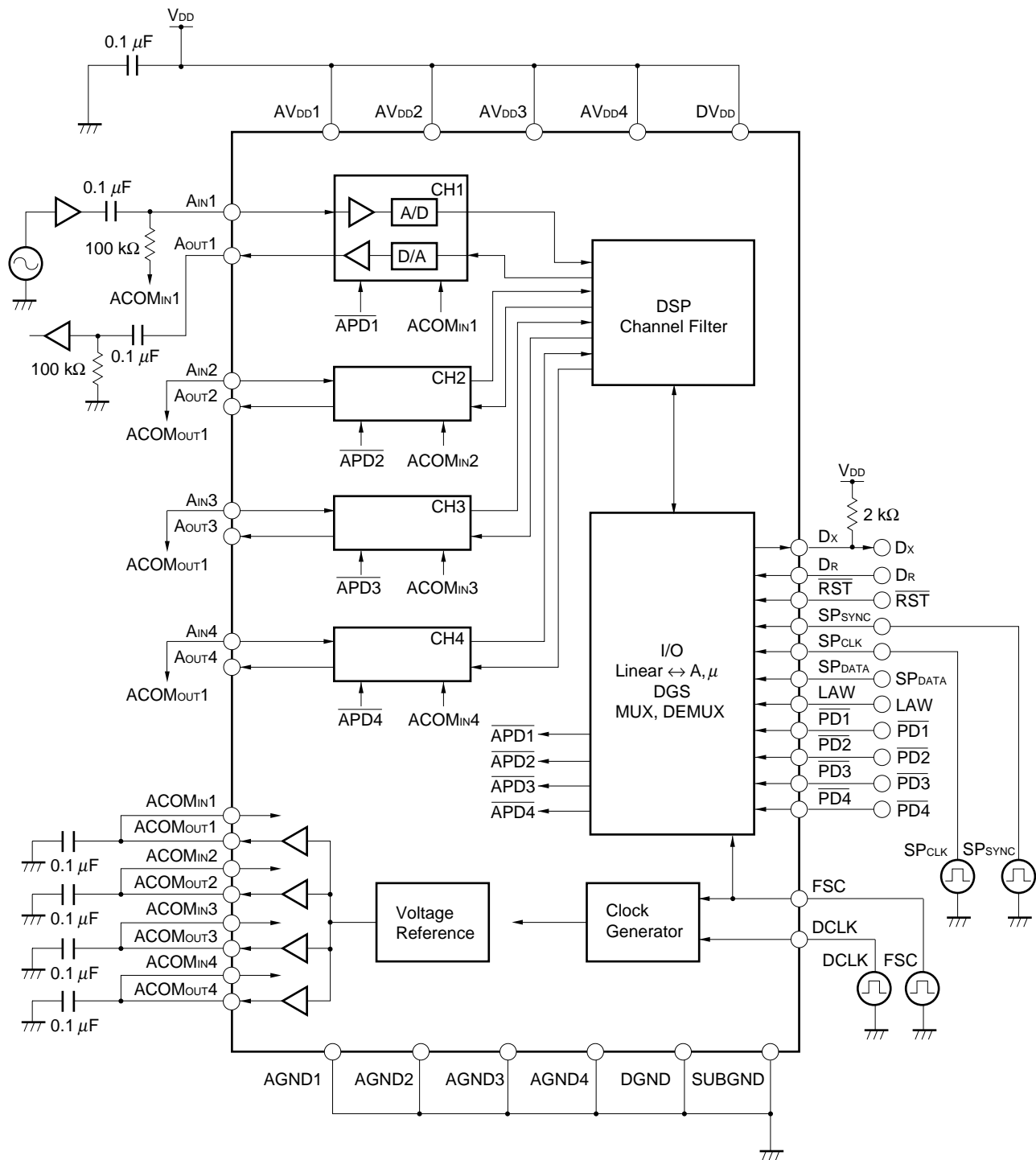
**TRANSMISSION CHARACTERISTICS (T<sub>A</sub> = –20 to +85 °C, V<sub>DD</sub> = 5 ± 0.25 V, GND = 0 V, f<sub>DCLK</sub> = 2048 kHz)**

Item	Symbol	Condition	Setting Value	Unit
Zero transmission level point (transmit)	OTLP <sub>x</sub>	Referenced to 600 $\Omega$	–3.8	dBm
Zero transmission level point (receive)	OTLP <sub>x</sub>	Referenced to 600 $\Omega$	–3.8	dBm

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Insertion loss	IL	A/D input signal 0 dBm0 1 kHz	–0.3		+0.3	dB
		D/A input signal 0 dBm0 1 kHz	–0.3		+0.3	
Transmission loss frequency characteristics	F <sub>RX</sub>	A/D Reference input signal 1015 Hz 0 dBm0	60 Hz	24.0	–	dB
			200 Hz	0	2.0	
			300 to 3000 Hz	–0.15	+0.15	
			3200 Hz	–0.15	+0.65	
			3400 Hz	0	0.8	
			3780 Hz	+6.5		
	F <sub>RR</sub>	D/A Reference input signal 1015 Hz 0 dBm0	0 to 3000 Hz	–0.15	+0.15	
			3200 Hz	–0.15	+0.65	
			3400 Hz	0	+0.8	
			3780 Hz	+6.5		
Gain tracking (tone method)	GT <sub>X</sub>	A/D Reference input signal –10 dBm0 f = 700 to 1100 Hz	+3 to –40 dBm0	–0.2	+0.2	dB
			–50 dBm0	–0.5	+0.5	
			–55 dBm0	–1.0	+1.0	
	GT <sub>R</sub>	D/A Reference input signal –10 dBm0 f = 700 to 1100 Hz	+3 to –40 dBm0	–0.2	+0.2	
			–50 dBm0	–0.5	+0.5	
			–55 dBm0	–1.0	+1.0	
Transmit/receive channel overall power distortion ratio (tone method)	SD <sub>X</sub>	A/D Input signal f = 700 to 1100 Hz	+3 to –30 dBm0	36		dB
			–40 dBm0	30		
			–45 dBm0	25		
	SD <sub>R</sub>	D/A Input signal f = 700 to 1100 Hz	+3 to –30 dBm0	36		
			–40 dBm0	30		
			–45 dBm0	25		
Absolute delay characteristic	D <sub>A</sub>	A/A Input signal = 0 dBm0			540	$\mu$ s
Absolute delay distortion frequency characteristics	D <sub>O</sub>	A/A	500 Hz		1400	$\mu$ s
			600 Hz		700	
			1000 to 2600 Hz		200	
			2800 Hz		1400	
Idle channel noise	ICN <sub>ADA</sub>	A/D A-law Psophometric weighted			–72	dBm0p
	ICN <sub>DAA</sub>	D/A A-law Psophometric weighted			–80	
	ICN <sub>AD<math>\mu</math></sub>	A/D $\mu$ -law C-message weighted			18	dB <sub>Brnc0</sub>
	ICN <sub>DA<math>\mu</math></sub>	D/A $\mu$ -law C-message weighted			10	

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Cross talk between channels	CT	A/A Input signal = 0 dBm0			-70	dB
Power supply rejection ratio	PSRR	AV <sub>DD1</sub> , AV <sub>DD2</sub> , AV <sub>DD3</sub> , AV <sub>DD4</sub> , DV <sub>DD</sub> = 5 V ± 100 mV <sub>P-P</sub>			-25	dB
Coder offset		A/D Input signal 0 V	-5		+5	-
Mutual modulation (2 tones)	IMD	A/D Input signal: f1, f2; 300 to 3400 Hz, -4 to -21 dBm0 Measuring signal: 2 × f1 - f2 level (2 × f1 - f2) vs level (f1, f2)	44.0			dB
		D/A Input signal: f1, f2; 300 to 3400Hz, -4 to -21 dBm0 Measuring signal: 2 × f1 - f2 level (2 × f1 - f2) vs level (f1, f2)	44.0			dB
Discrimination		A/D Input signal: f; 4396 to 7796 Hz 0 dBm0 Measuring signal: 8000 - fHz			-27	dB
Out-of-band spurious		D/A Input signal: f; 204 to 3604 Hz 0 dBm0 Measuring signal: 8000 - fHz			-27	dB
In-band spurious		A/D Input signal: f; 700 to 1100 Hz 0 dBm0 Measuring signal: Any frequency			-45	dB
		D/A Input signal: f; 700 to 1100 Hz 0 dBm0 Measuring signal: Any frequency			-45	dB
Single frequency noise	N <sub>SF</sub>	D/A Gain setting = 0 dB Measuring signal: f = up to 256 kHz			-54	dBm0
Transmit gain setting	ΔDGS <sub>x</sub>	A/D difference from reference setting value	-0.15		+0.15	dB
Receive gain setting	ΔDGS <sub>R</sub>	D/A difference from reference setting value	-0.15		+0.15	

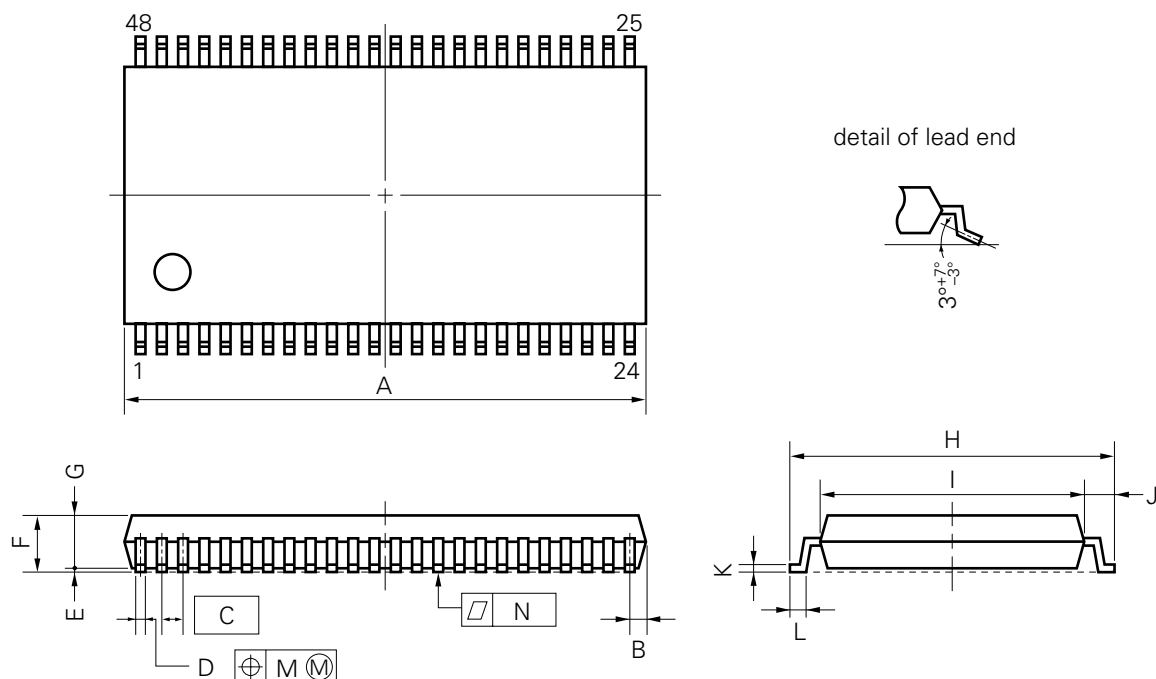
## 5. APPLICATION CIRCUIT EXAMPLE





## 6. PACKAGE DRAWINGS

## 48 PIN PLASTIC SHRINK SOP (375 mil)

**NOTE**

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

P48GT-65-375B-1

ITEM	MILLIMETERS	INCHES
A	16.21 MAX.	0.639 MAX.
B	0.63 MAX.	0.025 MAX.
C	0.65 (T.P.)	0.026 (T.P.)
D	0.30±0.10	0.012 <sup>+0.004</sup> <sub>-0.005</sub>
E	0.125±0.075	0.005±0.003
F	2.0 MAX.	0.079 MAX.
G	1.7±0.1	0.067±0.004
H	10.0±0.3	0.394 <sup>+0.012</sup> <sub>-0.013</sub>
I	8.0±0.2	0.315±0.008
J	1.0±0.2	0.039 <sup>+0.009</sup> <sub>-0.008</sub>
K	0.15 <sup>+0.10</sup> <sub>-0.05</sub>	0.006 <sup>+0.004</sup> <sub>-0.002</sub>
L	0.5±0.2	0.020 <sup>+0.008</sup> <sub>-0.009</sub>
M	0.10	0.004
N	0.10	0.004

## 7. RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the conditions recommended below.

For details of recommended soldering conditions, refer to the information document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended, please contact your NEC sales representative.

### SURFACE MOUNT TYPE

μPD9611GT: 48-pin shrink SOP (375 mil)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235 °C Duration: 30 sec. max. (210 °C or above) Number of times: 2 max. Time limit: 3 days <sup>Note</sup> (thereafter, 10-hour prebaking at 125 °C required.) <b>&lt;Cautions&gt;</b> (1) Wait for the device temperature to return to normal after the first reflow before starting the second reflow. (2) Do not perform flux cleaning with water after the first reflow.	IR-35-103-2
Pin heating	Pin temperature: 300 °C max. Duration: 3 sec. max. (per side of device)	—

**Note** For the storage period after unpacking from the dry-pack, storage conditions are max. 25 °C, 65 % RH.

## NOTES FOR CMOS DEVICES

### ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

**Note:** Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

### ② HANDLING OF UNUSED INPUT PINS FOR CMOS

**Note:** No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

**Note:** Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

## [MEMO]

The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

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NEC devices are classified into the following three quality grades:

"Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.

Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

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