

PEMH19; PUMH19

NPN/NPN resistor-equipped transistors;
R1 = 22 k Ω , R2 = open

Rev. 03 — 15 November 2009

Product data sheet

1. Product profile

1.1 General description

NPN/NPN Resistor-Equipped Transistors (RET).

Table 1. Product overview

Type number	Package		NPN/PNP complement	PNP/PNP complement
	NXP	JEITA		
PEMH19	SOT666	-	PEMD19	PEMB19
PUMH19	SOT363	SC-88	PUMD19	PUMB19

1.2 Features

- Built-in bias resistor
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs

1.3 Applications

- Low current peripheral driver
- Control of IC inputs
- Replaces general-purpose transistors in digital applications

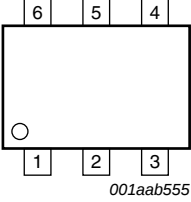
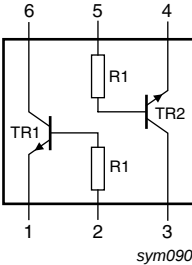
1.4 Quick reference data

Table 2. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CEO}	collector-emitter voltage	open base	-	-	50	V
I _O	output current (DC)		-	-	100	mA
R1	bias resistor 1 (input)		15.4	22	28.6	k Ω

2. Pinning information

Table 3. Pinning

Pin	Description	Simplified outline	Symbol
1	GND (emitter) TR1	 001aab555	 sym090
2	input (base) TR1		
3	output (collector) TR2		
4	GND (emitter) TR2		
5	input (base) TR2		
6	output (collector) TR1		

3. Ordering information

Table 4. Ordering information

Type number	Package		
	Name	Description	Version
PEMH19	-	plastic surface mounted package; 6 leads	SOT666
PUMH19	SC-88	plastic surface mounted package; 6 leads	SOT363

4. Marking

Table 5. Marking codes

Type number	Marking code ^[1]
PEMH19	6F
PUMH19	H6*

[1] * = -: made in Hong Kong
* = p: made in Hong Kong
* = t: made in Malaysia
* = W: made in China

5. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Per transistor					
V _{CBO}	collector-base voltage	open emitter	-	50	V
V _{CEO}	collector-emitter voltage	open base	-	50	V
V _{EBO}	emitter-base voltage	open collector	-	5	V
I _O	output current (DC)		-	100	mA
I _{CM}	peak collector current		-	100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C			
	SOT363		[1]	200	mW
	SOT666		[1][2]	200	mW
T _{stg}	storage temperature		-65	+150	°C
T _j	junction temperature		-	150	°C
T _{amb}	ambient temperature		-65	+150	°C
Per device					
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C			
	SOT363		[1]	300	mW
	SOT666		[1][2]	300	mW

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[2] Reflow soldering is the only recommended soldering method.

6. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
R _{th(j-a)}	thermal resistance from junction to ambient	in free air				
	SOT363		[1]	-	625	K/W
	SOT666		[1][2]	-	625	K/W
Per device						
R _{th(j-a)}	thermal resistance from junction to ambient	in free air				
	SOT363		[1]	-	416	K/W
	SOT666		[1][2]	-	416	K/W

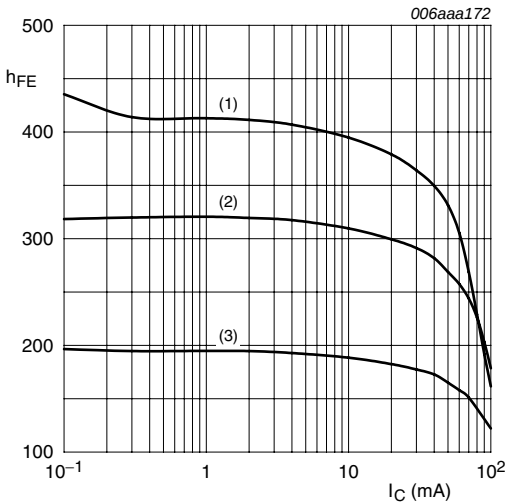
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Reflow soldering is the only recommended soldering method.

7. Characteristics

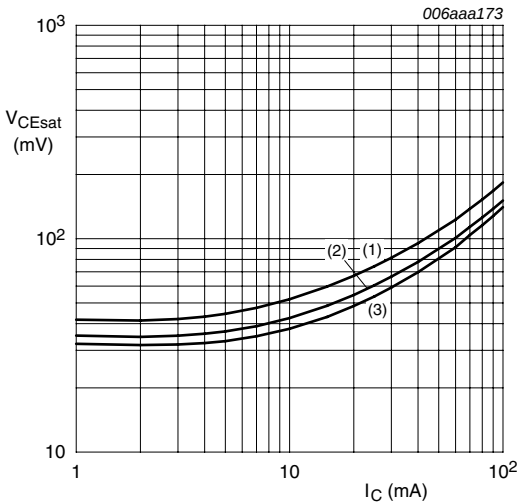
Table 8. Characteristics
T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
I _{CBO}	collector-base cut-off current	V _{CB} = 50 V; I _E = 0 A	-	-	100	nA
I _{CEO}	collector-emitter cut-off current	V _{CE} = 30 V; I _B = 0 A	-	-	1	μA
		V _{CE} = 30 V; I _B = 0 A; T _j = 150 °C	-	-	50	μA
I _{EBO}	emitter-base cut-off current	V _{EB} = 5 V; I _C = 0 A	-	-	100	nA
h _{FE}	DC current gain	V _{CE} = 5 V; I _C = 1 mA	100	-	-	
V _{CEsat}	collector-emitter saturation voltage	I _C = 10 mA; I _B = 0.5 mA	-	-	150	mV
R1	bias resistor 1 (input)		15.4	22	28.6	kΩ
C _c	collector capacitance	V _{CB} = 10 V; I _E = i _e = 0 A; f = 1 MHz	-	-	2.5	pF



V_{CE} = 5 V
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = -40 °C

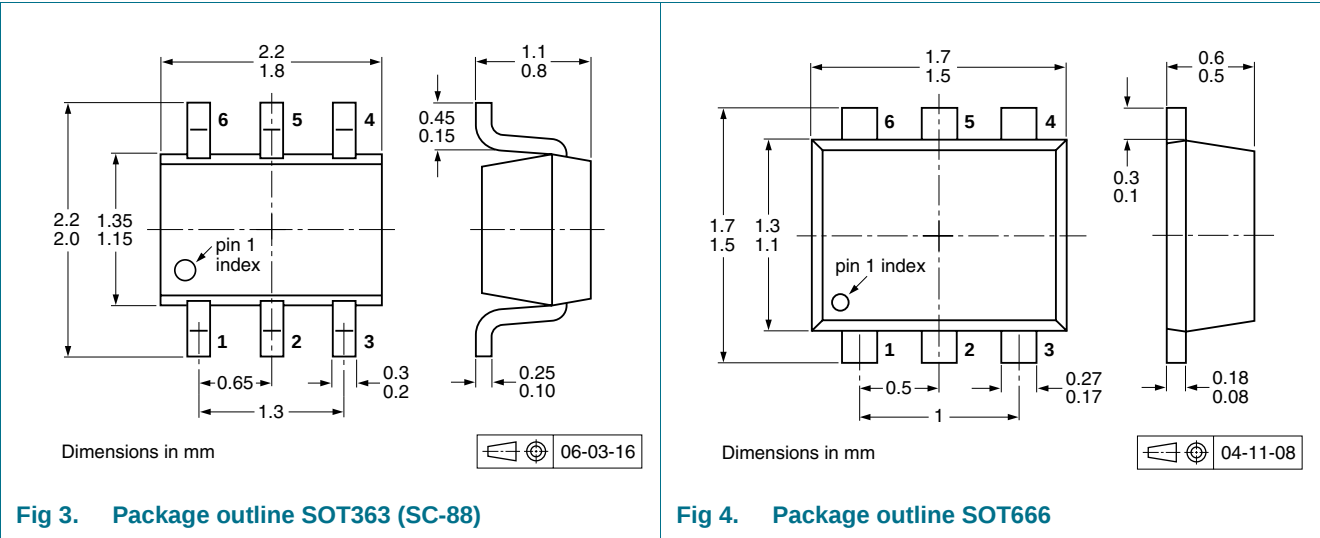
Fig 1. DC current gain as a function of collector current; typical values



I_C/I_B = 20
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = -40 °C

Fig 2. Collector-emitter saturation voltage as a function of collector current; typical values

8. Package outline



9. Packing information

Table 9. Packing methods
The indicated -xxx are the last three digits of the 12NC ordering code.^[1]

Type number	Package	Description	Packing quantity			
			3000	4000	8000	10000
PEMH19	SOT666	2 mm pitch, 8 mm tape and reel	-	-	-315	-
		4 mm pitch, 8 mm tape and reel	-	-115	-	-
PUMH19	SOT363	4 mm pitch, 8 mm tape and reel; T1 ^[2]	-115	-	-	-135
		4 mm pitch, 8 mm tape and reel; T2 ^[3]	-125	-	-	-165

[1] For further information and the availability of packing methods, see [Section 12](#).
[2] T1: normal taping
[3] T2: reverse taping

10. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PEMH19_PUMH19_3	20091115	Product data sheet	-	PEMH19_PUMH19_2
Modifications:	- This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content. Figure 3 "Package outline SOT363 (SC-88)": updated			
PEMH19_PUMH19_2	20050502	Product data sheet	-	PUMH19_1
PUMH19_1	20031016	Product specification	-	-

11. Legal information

11.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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