Integrated Device Technology, Inc.

# FAST CMOS 12-BIT SYNCHRONOUS BUS EXCHANGER

**IDT54/74FCT162H272AT/CT/ET**

## FEATURES:

- 0.5 MICRON CMOS Technology
- **Typical tsk(o) (Output Skew) < 250ps**
- **Low input and output leakage ≤ 1μA (max.)**
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Packages include 25 mil pitch SSOP, 19.6 mil pitch TSSOP, 15.7 mil pitch TVSOP and 25 mil pitch Cerpack
- Extended commercial range of -40°C to +85°C
- Balanced Output Drivers: ±24mA (commercial)
  ±16mA (military)
- Reduced system switching noise
- Typical VOLP (Output Ground Bounce) < 0.6V at VCC = 5V, TA = 25°C
- Bus Hold retains last active bus state during 3-state
- Eliminates the need for external pull up resistors

## DESCRIPTION:

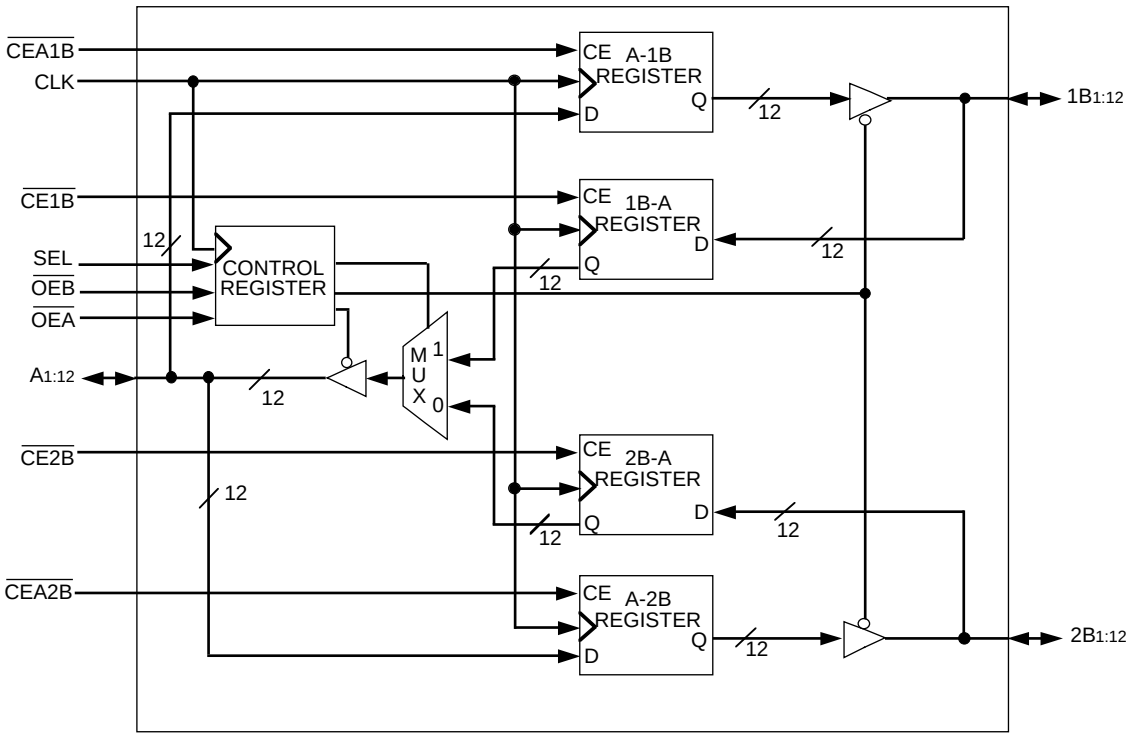
The FCT162H272AT/CT/ET synchronous tri-port bus exchangers are high-speed, bidirectional,12-bit, registered, bus multiplexers for use in synchronous memory interleaving applications. All registers have a common clock and use a clock enable ($\overline{CE}$xxx) on each data register to control data sequencing. The output enables and mux select ($\overline{OEA}$, $\overline{OEB}$ and SEL) are also under synchronous control allowing direction changes to be edge triggered events.

The tri-port bus exchanger has three 12-bit ports. Data may be transferred between the A port and either/both of the B ports. The clock enable ($\overline{CE1B}$, $\overline{CE2B}$, $\overline{CEA1B}$ and $\overline{CEA2B}$) inputs control the data storage. Both B ports have a common output enable ($\overline{OEB}$) to aid in synchronously loading the B registers from the B port.

The FCT162H272AT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times-reducing the need for external series terminating resistors.

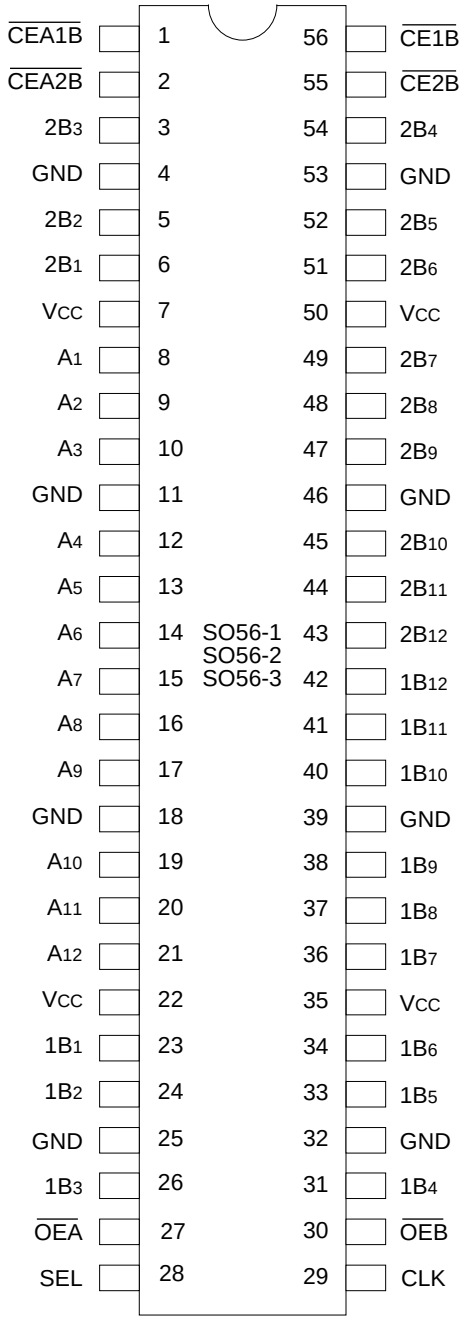
The FCT162H272AT/CT/ET have "Bus Hold" which retains the input's last state whenever the input goes to high impedance. This prevents "floating" inputs and eliminates the need for pull-up/down resistors.

## FUNCTIONAL BLOCK DIAGRAM



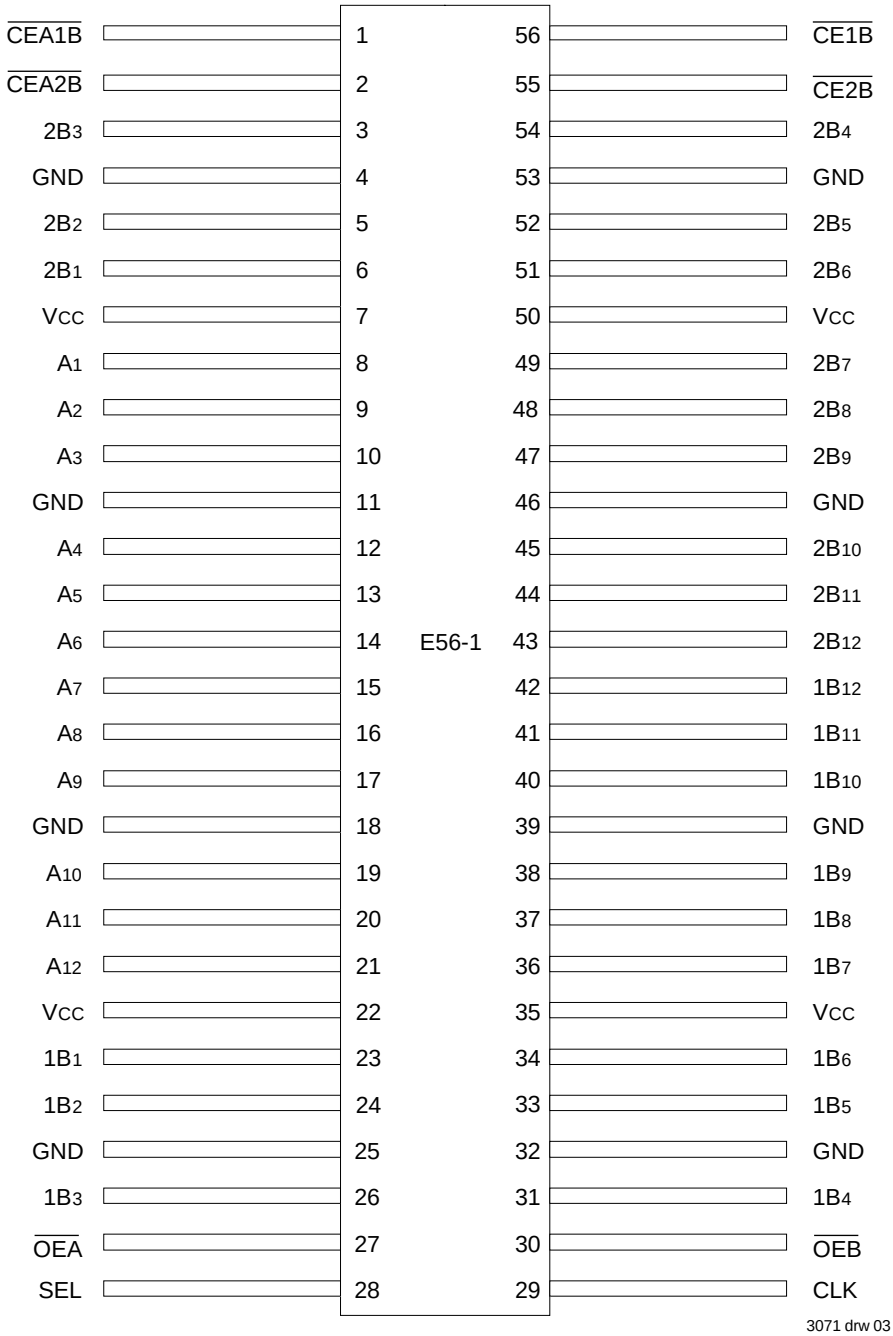

3071 drw 01

## PIN CONFIGURATIONS




3071 drw 02

**SSOP/ TSSOP/TVSOP TOP VIEW**




3071 drw 03

**CERPACK TOP VIEW**

## PIN DESCRIPTION

| Signal | I/O | Description |
|---|---|---|
| A(1:12) | I/O | Bidirectional Data Port A. Usually connected to the CPU's Address/Data bus.(1) |
| 1B(1:12) | I/O | Bidirectional Data Port 1B. Usually connected to the even path or even bank of memory.(1) |
| 2B(1:12) | I/O | Bidirectional Data Port 2B. Usually connected to the odd path or odd bank of memory.(1) |
| CLK | I | Clock Input. |
| $\overline{CEA1B}$ | I | Clock Enable Input for the A-1B Register. If $\overline{CEA1B}$ is LOW during the rising edge of CLK, data will be clocked into register A-1B (Active LOW). |
| $\overline{CEA2B}$ | I | Clock Enable Input for the A-2B Register. If $\overline{CEA2B}$ is LOW during the rising edge of CLK, data will be clocked into register A-2B (Active LOW). |
| $\overline{CE1B}$ | I | Clock Enable Input for the 1B-A Register. If $\overline{CE1B}$ is LOW during the rising edge of CLK, data will be clocked into register 1B-A (Active LOW). |
| $\overline{CE2B}$ | I | Clock Enable Input for the 2B-A Register. If $\overline{CE2B}$ is LOW during the rising edge of CLK, data will be clocked into register 2B-A (Active LOW). |
| SEL | I | 1B or 2B Path Selection. When HIGH during the rising edge of CLK, SEL enables data transfer from 1B Port to A Port. When LOW during the rising edge of CLK, SEL enables data transfer from 2B Port to A Port. |
| $\overline{OEA}$ | I | Synchronous Output Enable for A Port (Active LOW). |
| $\overline{OEB}$ | I | Synchronous Output Enable for 1B Port and 2B Port (Active LOW). |

**NOTES:** 3071 tbl 01
1. On FCT162H272T these pins have "Bus Hold". All other pins are standard inputs, outputs or I/Os.

## ABSOLUTE MAXIMUM RATINGS(1)

| Symbol | Description | Max. | Unit |
|---|---|---|---|
| $V_{TERM}$(2) | Terminal Voltage with Respect to GND | –0.5 to +7.0 | V |
| $V_{TERM}$(3) | Terminal Voltage with Respect to GND | –0.5 to $V_{CC}$ +0.5 | V |
| $T_{STG}$ | Storage Temperature | –65 to +150 | °C |
| $I_{OUT}$ | DC Output Current | –60 to +120 | mA |

**NOTES:** 3071 tbl 02
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

## CAPACITANCE ($T_A$ = +25°C, F = 1.0MHz)

| Symbol | Parameter(1) | Conditions | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 3.5 | 6.0 | pF |
| $C_{I/O}$ | I/O Capacitance | $V_{OUT}$ = 0V | 3.5 | 8.0 | pF |

**NOTE:** 3071 tbl 03
1. This parameter is measured at characterization but not tested.

## FUNCTION TABLES(2)

| Inputs | | | | | | | Output |
|---|---|---|---|---|---|---|---|
| 1B | 2B | SEL | $\overline{CE1B}$ | $\overline{CE2B}$ | $\overline{OEA}$ | CLK | A |
| H | X | H | L | X | L | ↑ | H |
| L | X | H | L | X | L | ↑ | L |
| X | X | H | H | X | L | ↑ | A(1) |
| X | H | L | X | L | L | ↑ | H |
| X | L | L | X | L | L | ↑ | L |
| X | X | L | X | H | L | ↑ | A(1) |
| X | X | X | X | X | H | ↑ | Z |

3071 tbl 04

| Inputs | | | | | Outputs | |
|---|---|---|---|---|---|---|
| A | $\overline{CEA1B}$ | $\overline{CEA2B}$ | $\overline{OEB}$ | CLK | 1B | 2B |
| H | L | L | L | ↑ | H | H |
| L | L | L | L | ↑ | L | L |
| H | L | H | L | ↑ | H | B(1) |
| L | L | H | L | ↑ | L | B(1) |
| H | H | L | L | ↑ | B(1) | H |
| L | H | L | L | ↑ | B(1) | L |
| X | H | H | L | ↑ | B(1) | B(1) |
| X | X | X | H | ↑ | Z | Z |
| X | X | X | L | ↑ | Active | Active |

**NOTES:** 3071 tbl 05
1. Output level before the indicated steady-state input conditions were established.
2. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance
   ↑ = LOW-to-HIGH Transition

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (BUS HOLD)

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A$ = –40°C to +85°C, $V_{CC}$ = 5.0V ± 10%; Military: $T_A$ = –55°C to +125°C, $V_{CC}$ = 5.0V ± 10%

| Symbol | Parameter | | Test Conditions[1] | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Level | | Guaranteed Logic HIGH Level | | 2.0 | — | — | V |
| $V_{IL}$ | Input LOW Level | | Guaranteed Logic LOW Level | | — | — | 0.8 | V |
| $I_{IH}$ | Input HIGH Current[4] | Standard Input[5] | $V_{CC}$ = Max. | $V_I$ = $V_{CC}$ | — | — | ±1 | µA |
| | | Standard I/O[5] | | | — | — | ±1 | |
| | | Bus-Hold Input | | | — | — | ±100 | |
| | | Bus-Hold I/O | | | — | — | ±100 | |
| $I_{IL}$ | Input LOW Current[4] | Standard Input[5] | | $V_I$ = GND | — | — | ±1 | |
| | | Standard I/O[5] | | | — | — | ±1 | |
| | | Bus-Hold Input | | | — | — | ±100 | |
| | | Bus-Hold I/O | | | — | — | ±100 | |
| $I_{BHH}$ | Bus Hold | Bus-Hold Input | $V_{CC}$ = Min. | $V_I$ = 2.0V | –50 | — | — | µA |
| $I_{BHL}$ | Sustain Current[4] | | | $V_I$ = 0.8V | +50 | — | — | |
| $I_{OZH}$ | High Impedance Output Current | | $V_{CC}$ = Max. | $V_O$ = 2.7V | — | — | ±1 | µA |
| $I_{OZL}$ | (3-State Output pins)[5,6] | | | $V_O$ = 0.5V | — | — | ±1 | |
| $V_{IK}$ | Clamp Diode Voltage | | $V_{CC}$ = Min., $I_{IN}$ = –18mA | | — | –0.7 | –1.2 | V |
| $I_{OS}$ | Short Circuit Current | | $V_{CC}$ = Max., $V_O$ = GND[3] | | –80 | –140 | –225 | mA |
| $V_H$ | Input Hysteresis | | — | | — | 100 | — | mV |
| $I_{CCL}$ $I_{CCH}$ $I_{CCZ}$ | Quiescent Power Supply Current | | $V_{CC}$ = Max., $V_{IN}$ = GND or $V_{CC}$ | | — | 5 | 500 | µA |

3071 tbl 06

## OUTPUT DRIVE CHARACTERISTICS FOR FCT162H272T

| Symbol | Parameter | Test Conditions[1] | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $I_{ODL}$ | Output LOW Current | $V_{CC}$ = 5V, $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $V_{OUT}$ = 1.5V[3] | | 60 | 115 | 200 | mA |
| $I_{ODH}$ | Output HIGH Current | $V_{CC}$ = 5V, $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $V_{OUT}$ = 1.5V[3] | | –60 | –115 | –200 | mA |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min. $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = –16mA MIL. $I_{OH}$ = –24mA COM'L. | 2.4 | 3.3 | — | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min. $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 16mA MIL. $I_{OL}$ = 24mA COM'L. | — | 0.3 | 0.55 | V |

3071 lnk 08

**NOTES:**

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Pins with Bus Hold are identified in the pin description.
5. The test limit for this parameter is ± 5µA at $T_A$ = –55°C.
6. Does not include Bus Hold I/O pins.

## POWER SUPPLY CHARACTERISTICS

| Symbol | Parameter | Test Conditions[1] | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $\Delta I_{CC}$ | Quiescent Power Supply Current<br>TTL Inputs HIGH | $V_{CC}$ = Max.<br>$V_{IN}$ = 3.4V[3] | | — | 0.5 | 1.5 | mA |
| $I_{CCD}$ | Dynamic Power Supply Current[4] | $V_{CC}$ = Max.<br>Outputs Open<br>One Output Port Enabled<br>$\overline{CExx}$ = GND<br>One Input Bit Toggling<br>One Output Bit Toggling<br>50% Duty Cycle | $V_{IN}$ = $V_{CC}$<br>$V_{IN}$ = GND | — | 60 | 100 | µA/<br>MHz |
| $I_C$ | Total Power Supply Current[6] | $V_{CC}$ = Max.<br>Outputs Open<br>fi = 10MHz | $V_{IN}$ = $V_{CC}$<br>$V_{IN}$ = GND | — | 0.6 | 1.5 | mA |
| | | 50% Duty Cycle<br>One Output Port Enabled<br>$\overline{CExx}$ = GND<br>One Input Bit Toggling<br>One Output Bit Toggling | $V_{IN}$ = 3.4V<br>$V_{IN}$ = GND | — | 0.9 | 2.3 | |
| | | $V_{CC}$ = Max.<br>Outputs Open<br>fi = 2.5MHz | $V_{IN}$ = $V_{CC}$<br>$V_{IN}$ = GND | — | 1.8 | 3.5[5] | |
| | | 50% Duty Cycle<br>One Output Port Enabled<br>$\overline{CExx}$ = GND<br>Twelve Input Bits Toggling<br>Twelve Output Bits Toggling | $V_{IN}$ = 3.4V<br>$V_{IN}$ = GND | — | 4.8 | 12.5[5] | |

3071 tbl 09

**NOTES:**

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC}$ = 5.0V, +25°C ambient.
3. Per TTL driven input ($V_{IN}$ = 3.4V). All other inputs at $V_{CC}$ or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the $I_{CC}$ formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   $I_{CC}$ = Quiescent Current ($I_{CCL}$, $I_{CCH}$ and $I_{CCZ}$)
   $\Delta I_{CC}$ = Power Supply Current for a TTL High Input ($V_{IN}$ = 3.4V)
   $D_H$ = Duty Cycle for TTL Inputs High
   $N_T$ = Number of TTL Inputs at $D_H$
   $I_{CCD}$ = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   $f_{CP}$ = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   $N_{CP}$ = Number of Clock Inputs at $f_{CP}$
   $f_i$ = Input Frequency
   $N_i$ = Number of Inputs at $f_i$

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

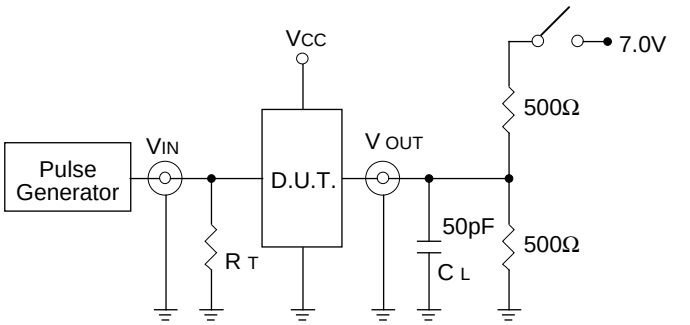
| Symbol | Parameter | | Condition[1] | FCT162H272AT | | | | FCT162H272CT | | | | FCT162H272ET | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Com'l. | | Mil. | | Com'l. | | Mil. | | Com'l. | | Mil. | | |
| | | | | Min.[2] | Max. | Min.[2] | Max. | Min.[2] | Max. | Min.[2] | Max. | Min.[2] | Max. | Min.[2] | Max. | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>CLK to 1Bx or CLK to 2Bx | | $C_L$ = 50pF<br>$R_L$ = 500Ω | 1.5 | 5.8 | 1.5 | 6.2 | 1.5 | 5.2 | 1.5 | 5.6 | 1.5 | 4.8 | — | — | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>CLK to Ax | $\overline{SEL}$ Stable<br>$\overline{CE}$xB Enabled | | 1.5 | 6.0 | 1.5 | 6.4 | 1.5 | 5.4 | 1.5 | 5.8 | 1.5 | 5.0 | — | — | ns |
| | | $\overline{SEL}$ Changing<br>$\overline{CE}$xB Disabled | | 1.5 | 6.0 | 1.5 | 6.4 | 1.5 | 5.4 | 1.5 | 5.8 | 1.5 | 5.4 | — | — | ns |
| | | $\overline{SEL}$ Changing<br>$\overline{CE}$xB Enabled | | 1.5 | 7.6 | 1.5 | 7.9 | 1.5 | 6.6 | 1.5 | 7.0 | 1.5 | 5.6 | — | — | ns |
| $t_{PZH}$<br>$t_{PZL}$ | Output Enable Time<br>CLK to Ax, CLK to 1Bx, or CLK to 2Bx | | | 1.5 | 7.7 | 1.5 | 8.1 | 1.5 | 6.8 | 1.5 | 7.2 | 1.5 | 6.0 | — | — | ns |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output Disable Time<br>CLK to Ax, CLK to 1Bx, or CLK to 2Bx | | | 1.5 | 6.4 | 1.5 | 6.8 | 1.5 | 6.0 | 1.5 | 6.4 | 1.5 | 5.6 | — | — | ns |
| $t_{SU}$ | Set-Up Time, HIGH or LOW Data to CLK | | | 2.0 | — | 2.0 | — | 2.0 | — | 2.0 | — | 2.0 | — | — | — | ns |
| $t_{SU}$ | Set-Up Time, $\overline{OEA}$ to CLK, $\overline{OEB}$ to CLK | | | 2.0 | — | 2.0 | — | 2.0 | — | 2.0 | — | 2.0 | — | — | — | ns |
| $t_{SU}$ | Set-Up Time, SEL to CLK | | | 2.0 | — | 2.0 | — | 2.0 | — | 2.0 | — | 2.0 | — | — | — | ns |
| $t_{SU}$ | Set-Up Time, $\overline{CEA1B}$ to CLK, $\overline{CE1B}$ to CLK, $\overline{CE2B}$ to CLK, or $\overline{CEA2B}$ to CLK | | | 2.0 | — | 2.0 | — | 2.0 | — | 2.0 | — | 2.0 | — | — | — | ns |
| $t_H$ | Hold Time, CLK to Data | | | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | — | — | ns |
| $t_H$ | Hold Time, CLK to $\overline{OEA}$, CLK to $\overline{OEB}$, CLK to SEL | | | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | — | — | ns |
| $t_H$ | Hold Time, CLK to $\overline{CEA1B}$, CLK to $\overline{CE1B}$, CLK to $\overline{CE2B}$, CLK to $\overline{CEA2B}$ | | | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | — | — | ns |
| $t_W$ | Pulse Width, CLK HIGH[4] | | | 3.0 | — | 3.0 | — | 3.0 | — | 3.0 | — | 3.0 | — | — | — | ns |
| $t_{SK}(o)$ | Output Skew[3] | | | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | — | ns |

3071 tbl 10

**NOTES:**
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This parameter is guaranteed but not tested.

## TEST CIRCUITS AND WAVEFORMS

### TEST CIRCUITS FOR ALL OUTPUTS




3071 lnk 04

### SWITCH POSITION

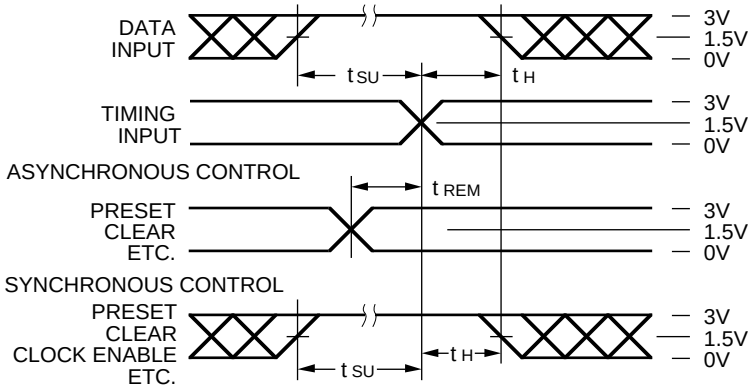
| Test | Switch |
|---|---|
| Open Drain<br>Disable Low<br>Enable Low | Closed |
| All Other Tests | Open |

3032 tbl 11

**DEFINITIONS:**

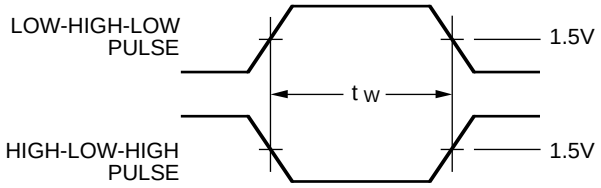
$C_L$ = Load capacitance: includes jig and probe capacitance.
$R_T$ = Termination resistance: should be equal to $Z_{OUT}$ of the Pulse Generator.

## SET-UP, HOLD AND RELEASE TIMES



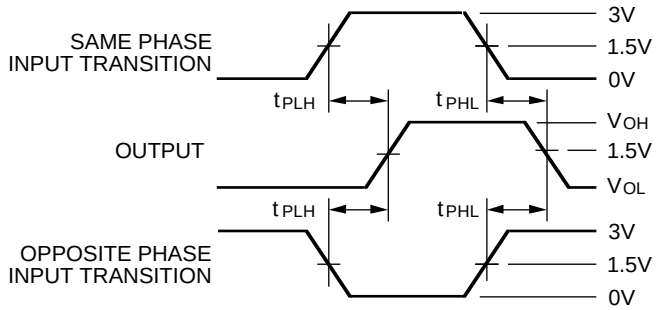

3071 lnk 05

## PULSE WIDTH



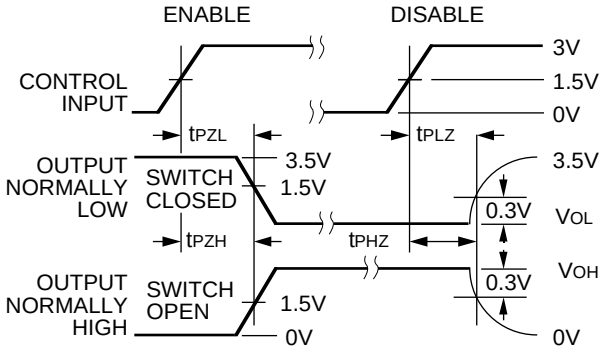

3071 lnk 06

## PROPAGATION DELAY




3071 lnk 07

## ENABLE AND DISABLE TIMES

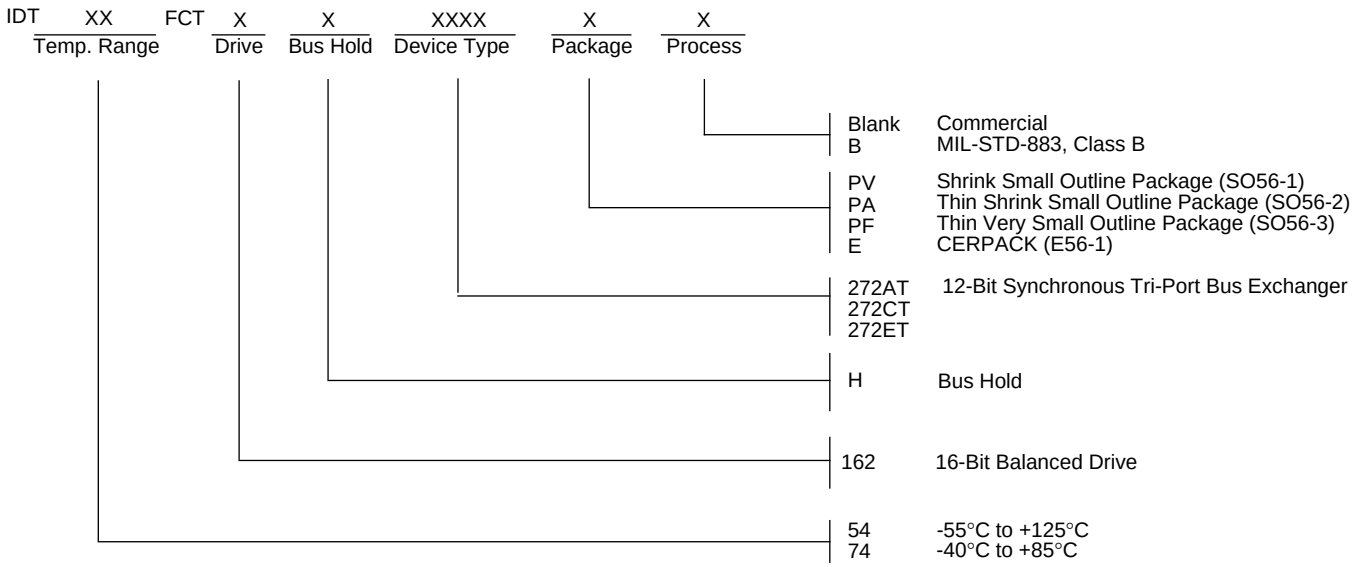



3071 drw 08

**NOTES:**

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $t_F$ ≤ 2.5ns; $t_R$ ≤ 2.5ns

## ORDERING INFORMATION




3071 drw 09