# SN5454, SN54LS54, SN7454, SN74LS54
# 4-WIDE AND-OR-INVERT GATES

SDLS115

DECEMBER 1983—REVISED MARCH 1988

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

## description

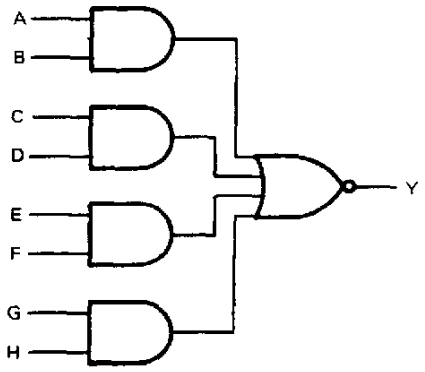
These devices contain 4-wide AND-OR-INVERT gates. They perform the following Boolean functions:

$$'54 \quad Y = \overline{AB + CD + EF + GH}$$
$$LS54 \quad Y = \overline{AB + CDE + FGH + IJ}$$

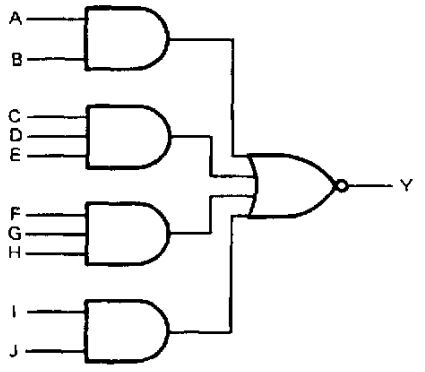
The SN5454 and SN54LS54 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7454 and SN74LS54 are characterized for operation from 0°C to 70°C.

## logic diagrams (positive logic)

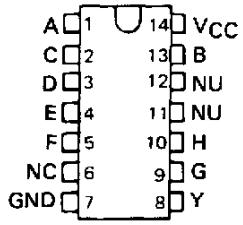
'54



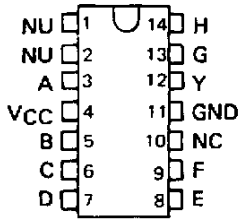

'LS54



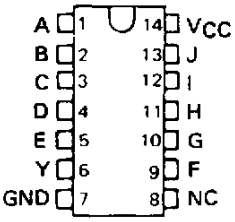

SN5454 . . . J PACKAGE
SN7454 . . . N PACKAGE
(TOP VIEW)



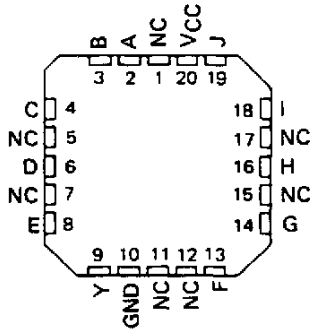

SN5454 . . . W PACKAGE
(TOP VIEW)




SN54LS54 . . . J OR W PACKAGE
SN74LS54 . . . D OR N PACKAGE
(TOP VIEW)




SN54LS54 . . . FK PACKAGE
(TOP VIEW)

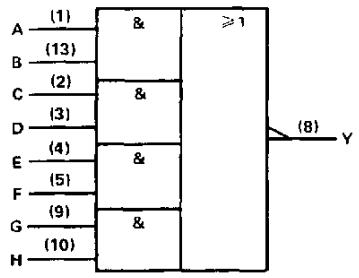



NC—No internal connection
NU—Make no external connection

# SN5454, SN54LS54, SN7454, SN74LS54
# 4-WIDE AND-OR-INVERT GATES

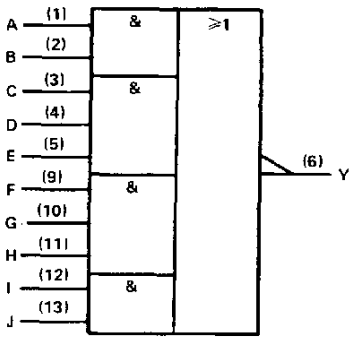
## logic symbols†

'54




positive logic: $Y = \overline{AB + CD + EF + GH}$

'LS54

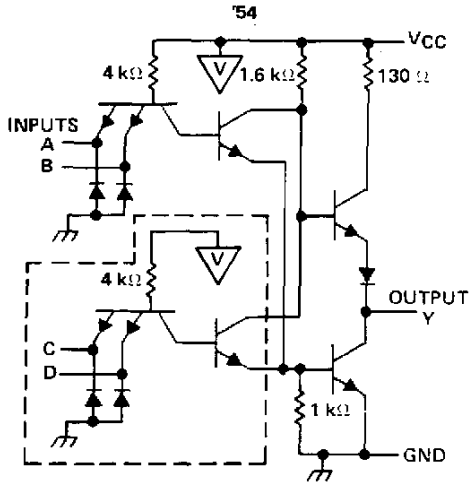



positive logic: $Y = \overline{AB + CDE + FGH + IJ}$

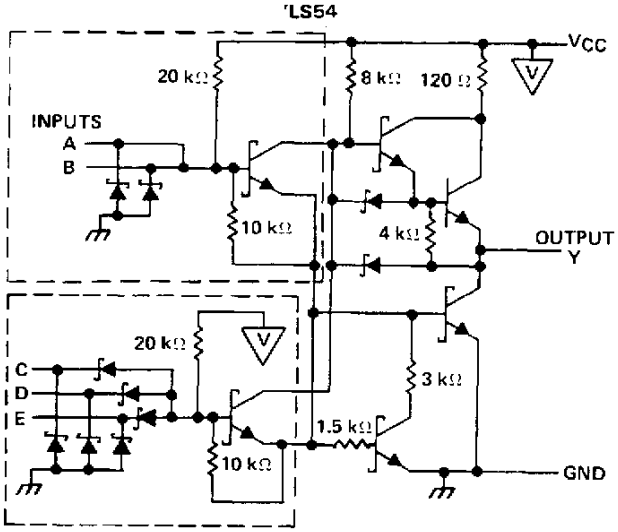
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N package. For the SN54LS54 only, they apply also for the W package.

## schematics

'54




'LS54




Resistor values shown are nominal.
The portion of the circuits within the dashed lines is repeated for each additional 2- or 3-input AND section, as shown in the logic diagram and logic symbols.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature: SN5454 . . . . . −55°C to 125°C
SN7454 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

### recommended operating conditions

| | | SN5454 | | | SN7454 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | −0.4 | | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | | | 16 | | | 16 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

### electrical characterics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS† | | | SN5454 | | | SN7454 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IK}$ | $V_{CC}$ = MIN, | $I_I$ = −12 mA | | | | −1.5 | | | −1.5 | V |
| $V_{OH}$ | $V_{CC}$ = MIN, | $V_{IL}$ = 0.8 V, | $I_{OH}$ = −0.4 mA | 2.4 | 3.4 | | 2.4 | 3.4 | | V |
| $V_{OL}$ | $V_{CC}$ = MIN, | $V_{IH}$ = 2 V, | $I_{OL}$ = 16 mA | | 0.2 | 0.4 | | 0.2 | 0.4 | V |
| $I_I$ | $V_{CC}$ = MAX, | $V_I$ = 5.5 V | | | | 1 | | | 1 | mA |
| $I_{IH}$ | $V_{CC}$ = MAX, | $V_I$ = 2.4 V | | | | 40 | | | 40 | μA |
| $I_{IL}$ | $V_{CC}$ = MAX, | $V_I$ = 0.4 V | | | | −1.6 | | | −1.6 | mA |
| $I_{OS}$§ | $V_{CC}$ = MAX | | | −20 | | −55 | −18 | | −55 | mA |
| $I_{CCH}$ | $V_{CC}$ = MAX, | $V_I$ = 0 V | | | 4 | 8 | | 4 | 8 | mA |
| $I_{CCL}$ | $V_{CC}$ = MAX, | See Note 2 | | | 5.1 | 9.5 | | 5.1 | 9.5 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§ Not more than one output should be shorted at a time.
NOTE 2: All inputs of one AND gate at 4.5 V, all others at GND.

### switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C (see note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Any | Y | $R_L$ = 400 Ω, | $C_L$ = 15 pF | | 13 | 22 | ns |
| $t_{PHL}$ | | | | | | 8 | 15 | ns |

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature: SN54LS54 . . . . . −55°C to 125°C
SN74LS54 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

### recommended operating conditions

| | | SN54LS54 | | | SN74LS54 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.7 | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | −0.4 | | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | | | 4 | | | 8 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS† | | | SN54LS54 | | | SN74LS54 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IK}$ | $V_{CC}$ = MIN, | $I_I$ = −18 mA | | | | −1.5 | | | −1.5 | V |
| $V_{OH}$ | $V_{CC}$ = MIN, | $V_{IL}$ = MAX, | $I_{OH}$ = −0.4 mA | 2.5 | 3.4 | | 2.7 | 3.4 | | V |
| $V_{OL}$ | $V_{CC}$ = MIN, | $V_{IH}$ = 2 V, | $I_{OL}$ = 4 mA | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | $V_{CC}$ = MIN, | $V_{IH}$ = 2 V, | $I_{OL}$ = 8 mA | | | | | 0.35 | 0.5 | |
| $I_I$ | $V_{CC}$ = MAX, | $V_I$ = 7 V | | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = MAX, | $V_I$ = 2.7 V | | | | 20 | | | 20 | μA |
| $I_{IL}$ | $V_{CC}$ = MAX, | $V_I$ = 0.4 V | | | | −0.4 | | | −0.4 | mA |
| $I_{OS}$§ | $V_{CC}$ = MAX | | | −20 | | −100 | −20 | | −100 | mA |
| $I_{CCH}$ | $V_{CC}$ = MAX, | $V_I$ = 0 V | | | 0.8 | 1.6 | | 0.8 | 1.6 | mA |
| $I_{CCL}$ | $V_{CC}$ = MAX, | See Note 2 | | | 1 | 2 | | 1 | 2 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.
NOTE 2: All inputs of one AND gate at 4.5 V, all others at GND.

### switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C (see note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Any | Y | $R_L$ = 2 kΩ, | $C_L$ = 15 pF | | 12 | 20 | ns |
| $t_{PHL}$ | | | | | | 12.5 | 20 | ns |

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| SN5454J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type |
| SN54LS54J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type |
| SN54LS54J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type |
| SN7454N | OBSOLETE | PDIP | N | 14 | | TBD | Call TI | Call TI |
| SN7454N | OBSOLETE | PDIP | N | 14 | | TBD | Call TI | Call TI |
| SN74LS54D | OBSOLETE | SOIC | D | 14 | | TBD | Call TI | Call TI |
| SN74LS54D | OBSOLETE | SOIC | D | 14 | | TBD | Call TI | Call TI |
| SN74LS54DR | OBSOLETE | SOIC | D | 14 | | TBD | Call TI | Call TI |
| SN74LS54DR | OBSOLETE | SOIC | D | 14 | | TBD | Call TI | Call TI |
| SN74LS54J | OBSOLETE | CDIP | J | 14 | | TBD | Call TI | Call TI |
| SN74LS54J | OBSOLETE | CDIP | J | 14 | | TBD | Call TI | Call TI |
| SN74LS54N | OBSOLETE | PDIP | N | 14 | | TBD | Call TI | Call TI |
| SN74LS54N | OBSOLETE | PDIP | N | 14 | | TBD | Call TI | Call TI |
| SNJ5454J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type |
| SNJ5454J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type |
| SNJ5454W | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type |
| SNJ5454W | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type |
| SNJ54LS54FK | OBSOLETE | | | 20 | | TBD | Call TI | Call TI |
| SNJ54LS54FK | OBSOLETE | | | 20 | | TBD | Call TI | Call TI |
| SNJ54LS54J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type |
| SNJ54LS54J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type |
| SNJ54LS54W | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type |
| SNJ54LS54W | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

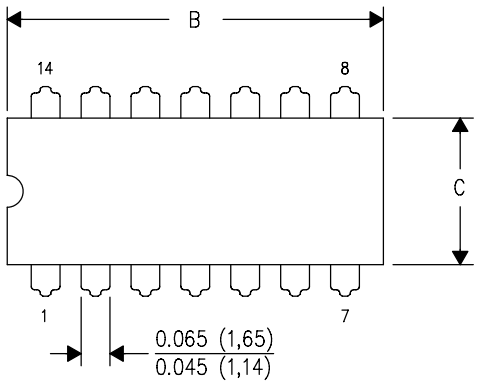
accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

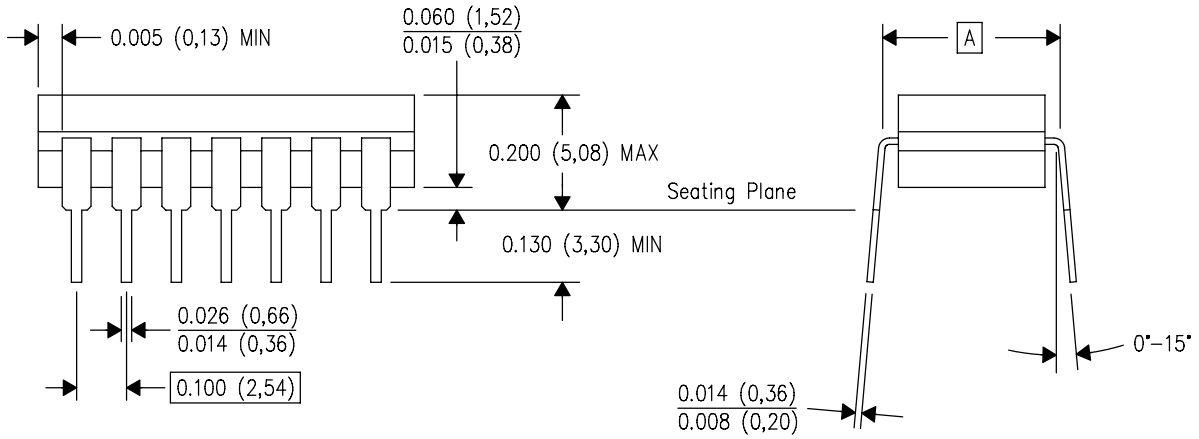
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

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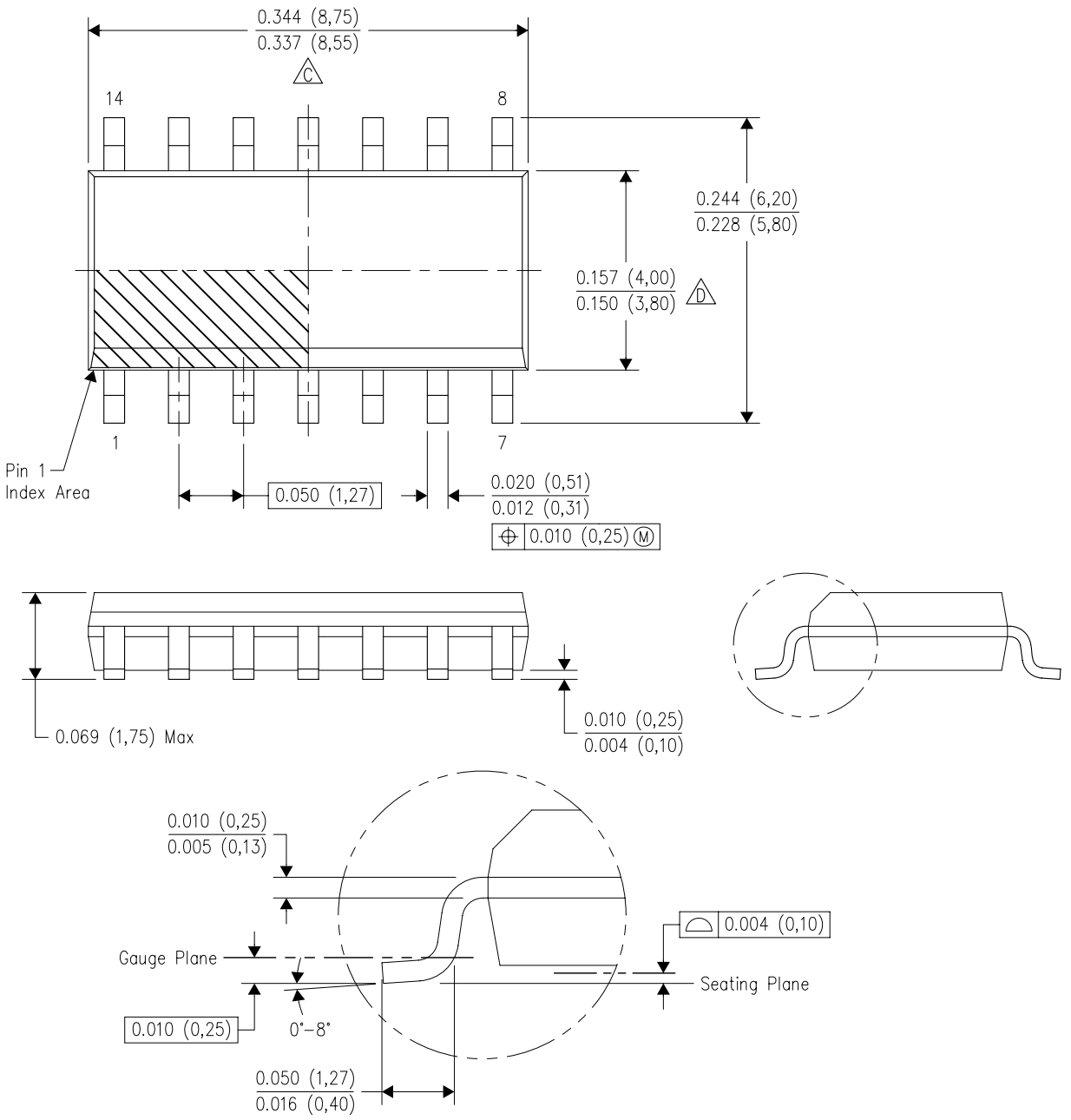
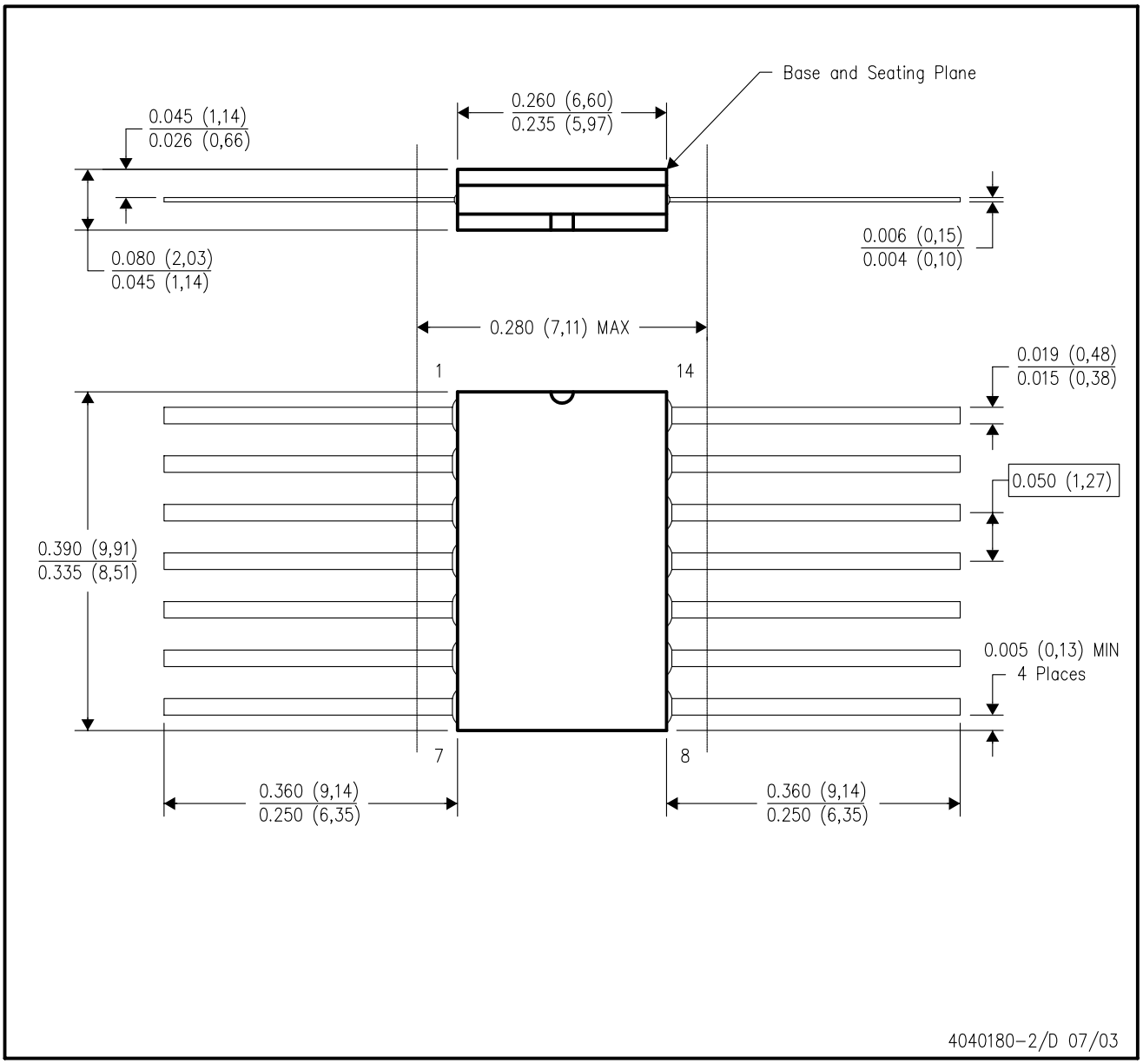
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AB.

## W (R–GDFP–F14) CERAMIC DUAL FLATPACK

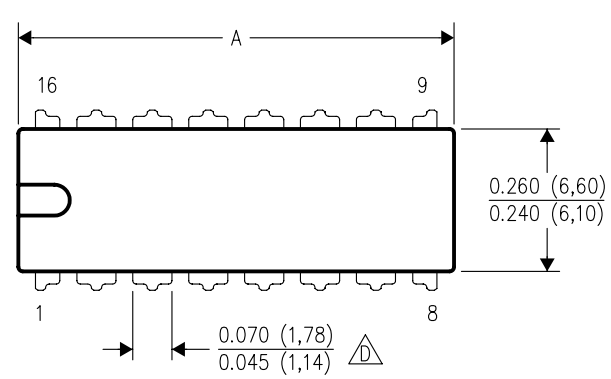



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14 and JEDEC MO–092AB

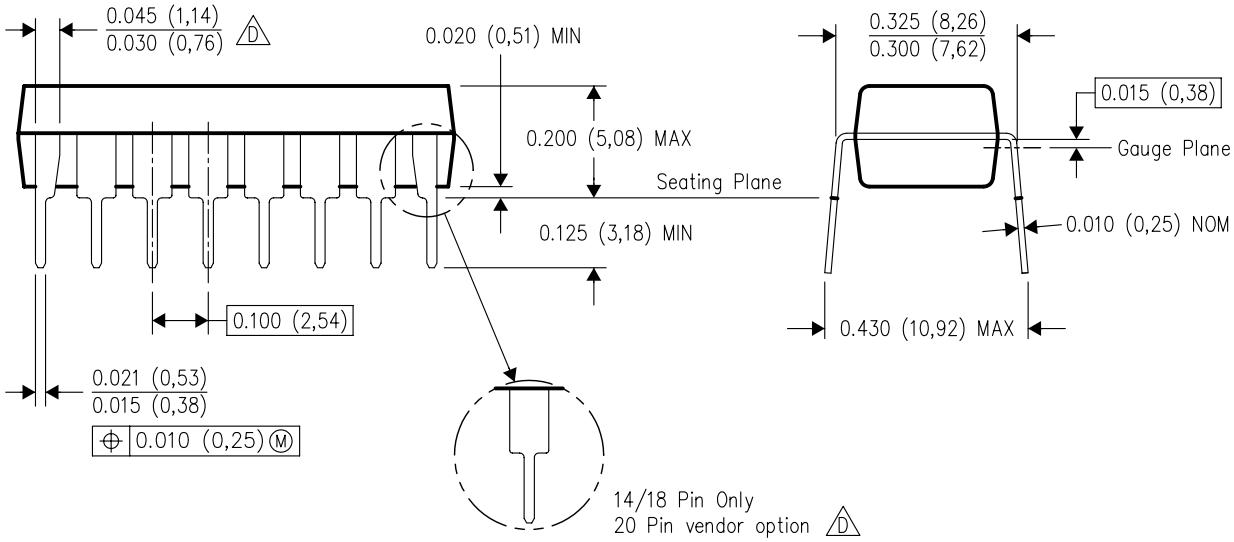
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| SN5454J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type |
| SN54LS54J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type |
| SN54LS54J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type |
| SN7454N | OBSOLETE | PDIP | N | 14 | | TBD | Call TI | Call TI |
| SN7454N | OBSOLETE | PDIP | N | 14 | | TBD | Call TI | Call TI |
| SN74LS54D | OBSOLETE | SOIC | D | 14 | | TBD | Call TI | Call TI |
| SN74LS54D | OBSOLETE | SOIC | D | 14 | | TBD | Call TI | Call TI |
| SN74LS54DR | OBSOLETE | SOIC | D | 14 | | TBD | Call TI | Call TI |
| SN74LS54DR | OBSOLETE | SOIC | D | 14 | | TBD | Call TI | Call TI |
| SN74LS54J | OBSOLETE | CDIP | J | 14 | | TBD | Call TI | Call TI |
| SN74LS54J | OBSOLETE | CDIP | J | 14 | | TBD | Call TI | Call TI |
| SN74LS54N | OBSOLETE | PDIP | N | 14 | | TBD | Call TI | Call TI |
| SN74LS54N | OBSOLETE | PDIP | N | 14 | | TBD | Call TI | Call TI |
| SNJ5454J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type |
| SNJ5454J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type |
| SNJ5454W | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type |
| SNJ5454W | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type |
| SNJ54LS54FK | OBSOLETE | | | 20 | | TBD | Call TI | Call TI |
| SNJ54LS54FK | OBSOLETE | | | 20 | | TBD | Call TI | Call TI |
| SNJ54LS54J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type |
| SNJ54LS54J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type |
| SNJ54LS54W | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type |
| SNJ54LS54W | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type |

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**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

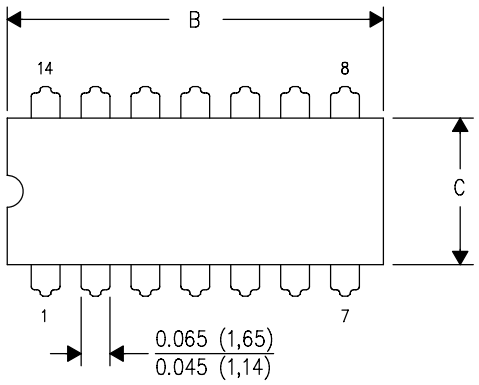
accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

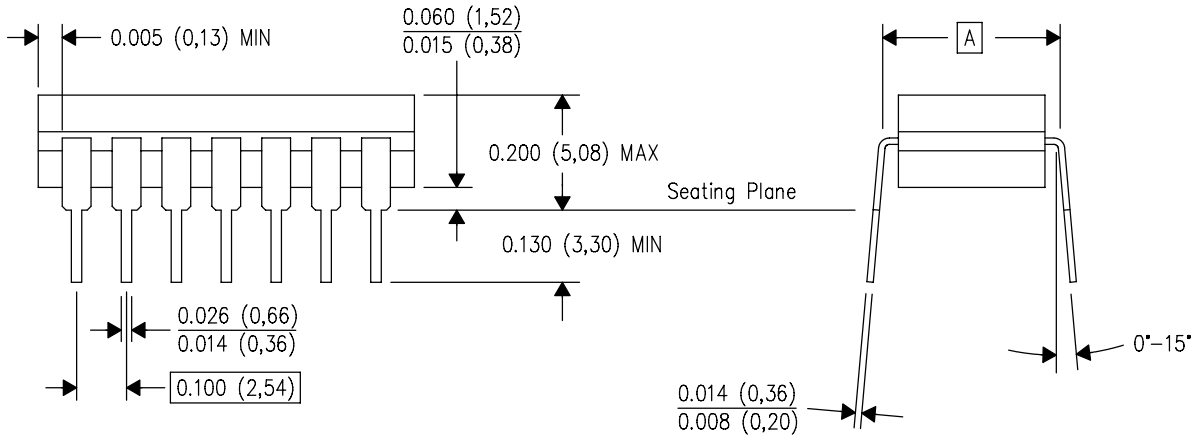
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE



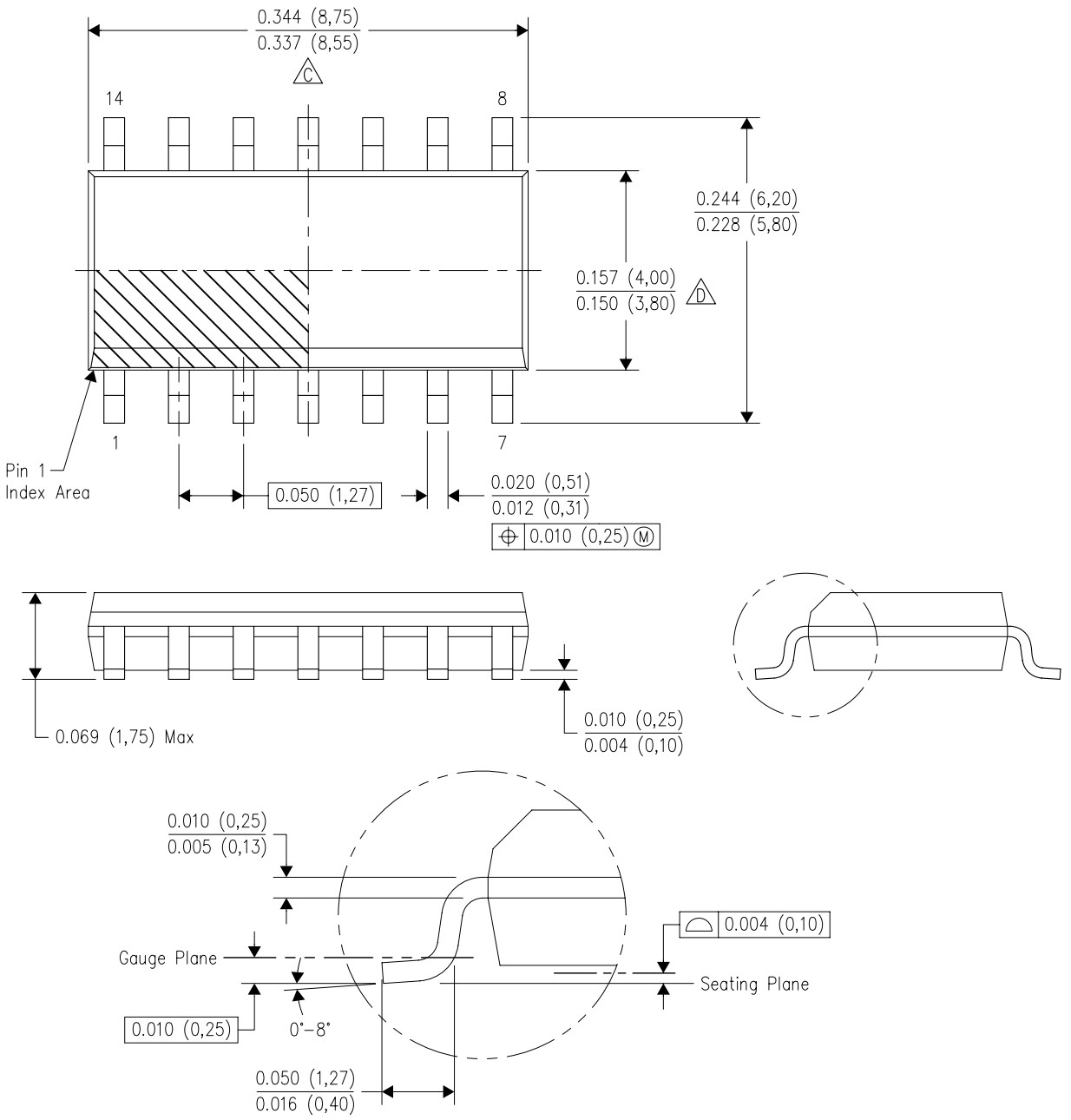

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |




4040083/F 03/03

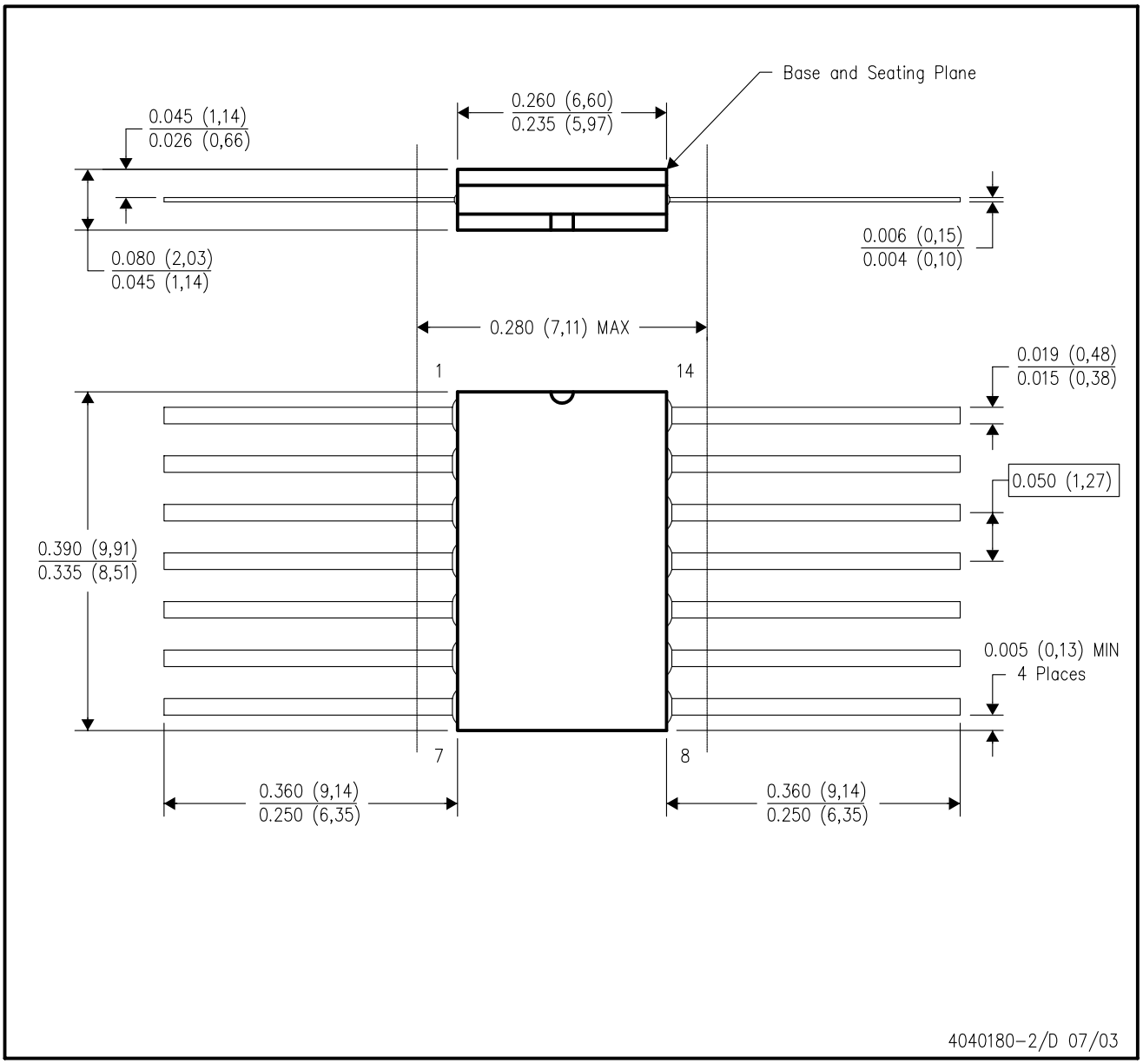
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AB.

## W (R–GDFP–F14) CERAMIC DUAL FLATPACK

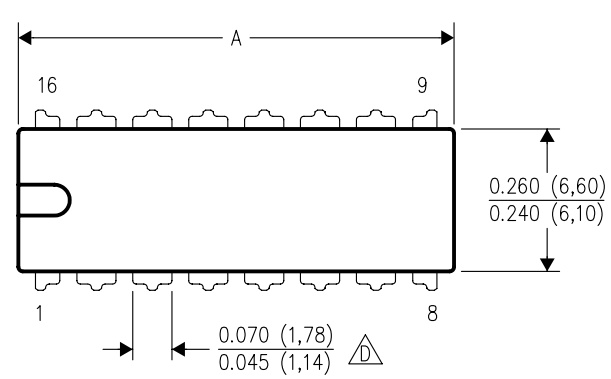



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14 and JEDEC MO–092AB

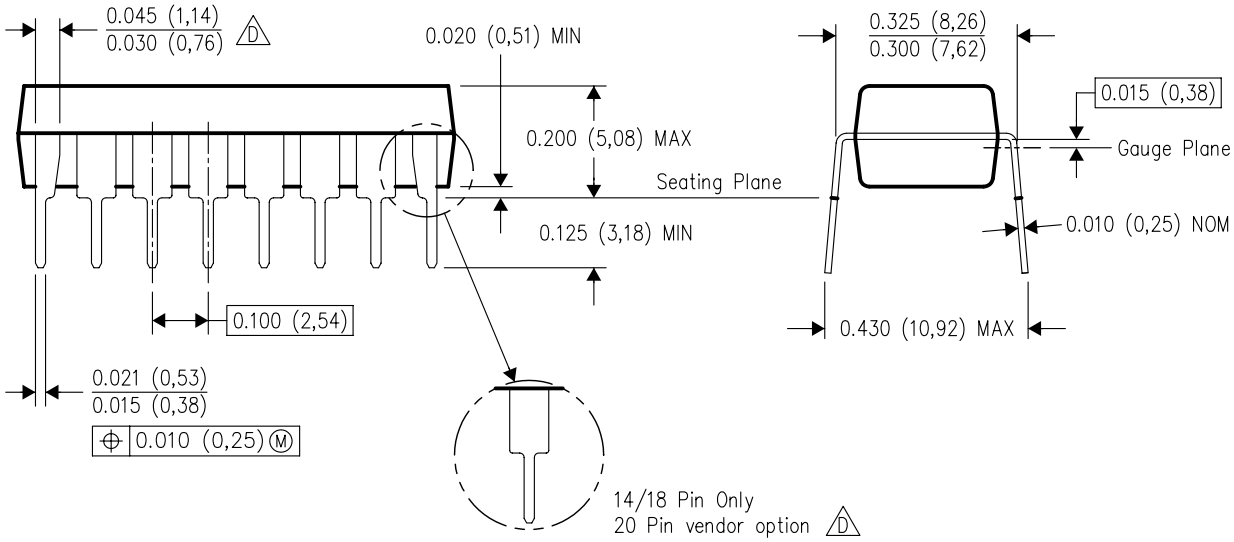
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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