# DATA SHEET

## 74F1240
## Octal inverter buffer (3-State)

Product specification
Supercedes data of 1999 Jan 08
IC15 Data Handbook

2000 Jun 30

Philips
Semiconductors

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# Octal inverter buffer (3-State) 74F1240

## FEATURES

- High impedance NPN base inputs for reduced loading (20µA in High and Low states)
- Low power, light loading
- Functional pin-for-pin equivalent of 74F240
- 1/30th the bus loading of 74F240
- Provides ideal interface and increase fan-out of MOS microprocessors
- Octal bus interface
- 3-State buffer outputs sink 64mA
- 15mA source current

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74F1240 | 3.5ns | 40mA |

## ORDERING INFORMATION

| DESCRIPTION | COMMERCIAL RANGE $V_{CC}$ = 5V ±10%, $T_{amb}$ = 0°C to +70°C | DRAWING NUMBER |
|---|---|---|
| 20-pin plastic DIP | N74F1240N | SOT146-1 |
| 20-pin plastic SOL | N74F1240D | SOT163-1 |

## DESCRIPTION

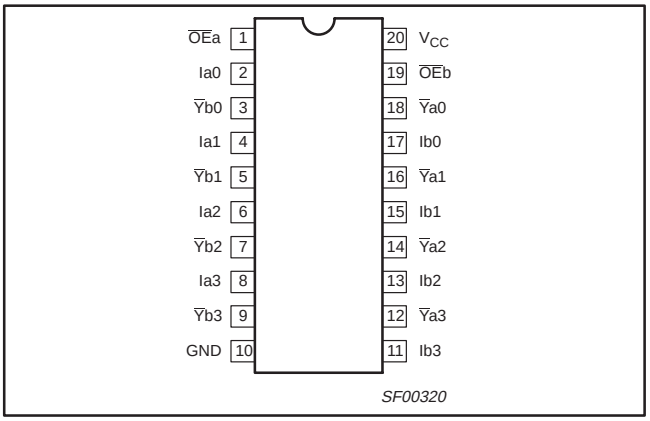
The 74F1240 is an octal buffer that is ideal for driving bus lines or buffer memory address registers. The outputs are capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features two Output Enables, $\overline{OE}$a and $\overline{OE}$b, each controlling four of the 3-State outputs.

## INPUT AND OUTPUT LOADING AND FAN OUT TABLE

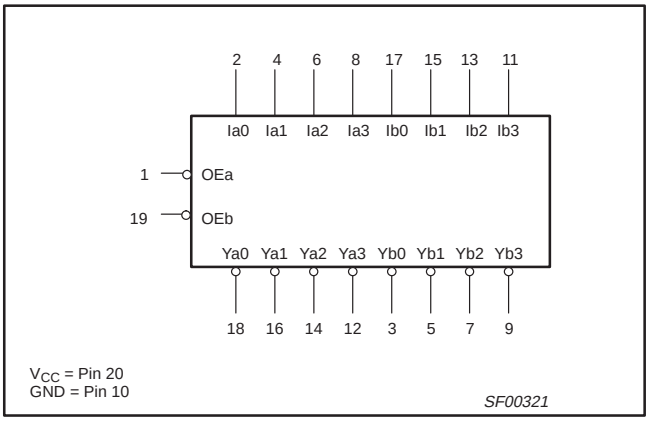
| PINS | DESCRIPTION | 74F (U.L.) HIGH/LOW | LOAD VALUE HIGH/LOW |
|---|---|---|---|
| Ian, Ibn | Data inputs | 1.0/0.033 | 20µA/20µA |
| $\overline{OE}$a, $\overline{OE}$b | Output enable inputs (active Low) | 1.0/0.033 | 20µA/20µA |
| $\overline{Y}$an, $\overline{Y}$bn | Data outputs (74F1240) | 750/106.7 | 15mA/64mA |

**NOTE:** One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

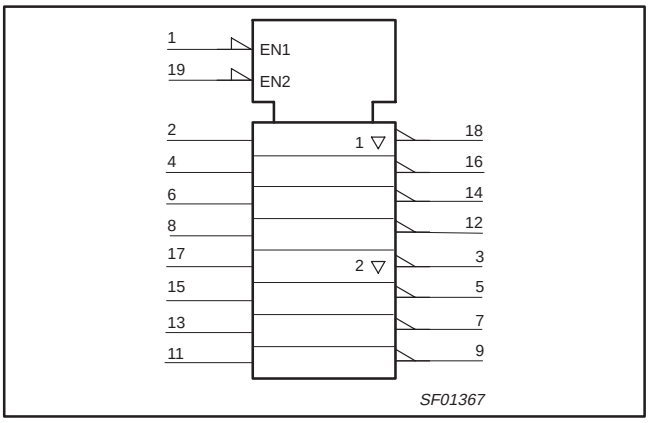
## PIN CONFIGURATION




## LOGIC SYMBOL




## IEC/IEEE SYMBOL

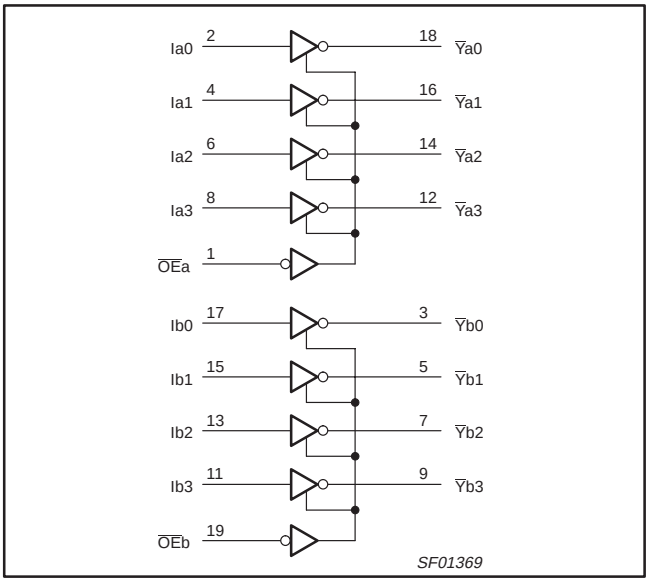



## FUNCTION TABLE

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| $\overline{OE}a$ | Ia | $\overline{OE}b$ | Ib | $\overline{Y}a$ | $\overline{Y}b$ |
| L | L | L | L | H | H |
| L | H | L | H | L | L |
| H | X | H | X | Z | Z |

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

## LOGIC DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | –0.5 to +7.0 | V |
| $V_{IN}$ | Input voltage | –0.5 to +7.0 | V |
| $I_{IN}$ | Input current | –30 to +5 | mA |
| $V_{OUT}$ | Voltage applied to output in High output state | –0.5 to $V_{CC}$ | V |
| $I_{OUT}$ | Current applied to output in Low output state | 128 | mA |
| $T_{amb}$ | Operating free-air temperature range | 0 to +70 | °C |
| $T_{stg}$ | Storage temperature range | –65 to +150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2.0 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | –18 | mA |
| $I_{OH}$ | High-level output current | | | –15 | mA |
| $I_{OL}$ | Low-level output current | | | 64 | mA |
| $T_{amb}$ | Operating free-air temperature range | 0 | | +70 | °C |

## DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

| SYMBOL | PARAMETER | TEST CONDITIONS[1] | | | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP[2] | MAX | |
| $V_{OH}$ | High-level output voltage | $V_{CC}$ = MIN, $V_{IL}$ = MAX, $V_{IH}$ = MIN | $I_{OH}$ = –3mA | ±10% $V_{CC}$ | 2.4 | | | V |
| | | | | ±5% $V_{CC}$ | 2.7 | 3.3 | | V |
| | | | $I_{OH}$ = –15mA | ±10% $V_{CC}$ | 2.0 | | | V |
| | | | | ±5% $V_{CC}$ | 2.0 | | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, $V_{IL}$ = MAX, $V_{IH}$ = MIN | $I_{OL}$ = 48mA | ±10% $V_{CC}$ | | 0.38 | 0.55 | V |
| | | | $I_{OL}$ = 64mA | ±5% $V_{CC}$ | | 0.42 | 0.55 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = MIN, $I_I$ = $I_{IK}$ | | | | –0.73 | –1.2 | V |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = 0.0V, $V_I$ = 7.0V | | | | | 100 | µA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = MAX, $V_I$ = 2.7V | | | | | 20 | µA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = MAX, $V_I$ = 0.5V | | | | | –20 | µA |
| $I_{OZH}$ | Off-state output current, High-level voltage applied | $V_{CC}$ = MAX, $V_O$ = 2.7V | | | | | 50 | µA |
| $I_{OZL}$ | Off-state output current, Low-level voltage applied | $V_{CC}$ = MAX, $V_O$ = 0.5V | | | | | –50 | µA |
| $I_{OS}$ | Short-circuit output current[3] | $V_{CC}$ = MAX | | | –100 | | –225 | mA |
| $I_{CC}$ | Supply current (total) | $I_{CCH}$ | $V_{CC}$ = MAX | | | 22 | 30 | mA |
| | | $I_{CCL}$ | | | | 58 | 75 | mA |
| | | $I_{CCZ}$ | | | | 44 | 58 | mA |

**NOTES:**

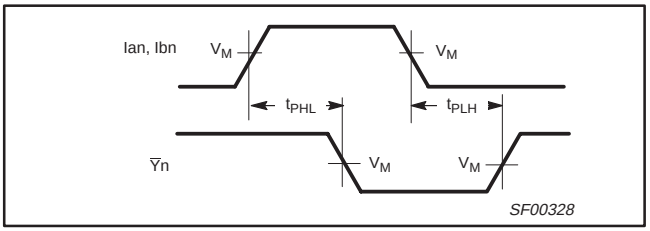
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at $V_{CC}$ = 5V, $T_{amb}$ = 25°C.
3. Not more than one output should be shorted at a time. For testing $I_{OS}$, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, $I_{OS}$ tests should be performed last.

## AC ELECTRICAL CHARACTERISTICS

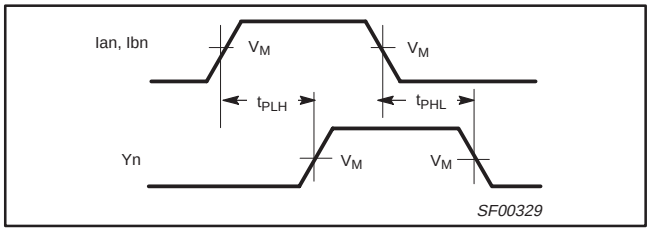
| SYMBOL | PARAMETER | TEST CONDITION | LIMITS | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $T_{amb}$ = +25°C, $V_{CC}$ = +5.0V, $C_L$ = 50pF, $R_L$ = 500Ω | | | $T_{amb}$ = 0°C to +70°C, $V_{CC}$ = +5.0V ± 10%, $C_L$ = 50pF, $R_L$ = 500Ω | | |
| | | | MIN | TYP | MAX | MIN | MAX | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>Ian, Ibn, to $\overline{Y}$n | Waveform 1 | 3.0<br>1.5 | 4.5<br>2.5 | 6.5<br>4.5 | 2.5<br>1.5 | 7.5<br>5.0 | ns<br>ns |
| $t_{PZH}$<br>$t_{PZL}$ | Output Enable time<br>to High or Low level | Waveform 3<br>Waveform 4 | 3.0<br>4.0 | 5.5<br>7.0 | 7.5<br>9.0 | 3.0<br>4.0 | 8.0<br>9.5 | ns<br>ns |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output Disable time<br>to High or Low level | Waveform 3<br>Waveform 4 | 2.0<br>2.0 | 4.0<br>4.0 | 6.0<br>5.5 | 2.0<br>2.0 | 6.5<br>6.0 | ns<br>ns |

## AC WAVEFORMS

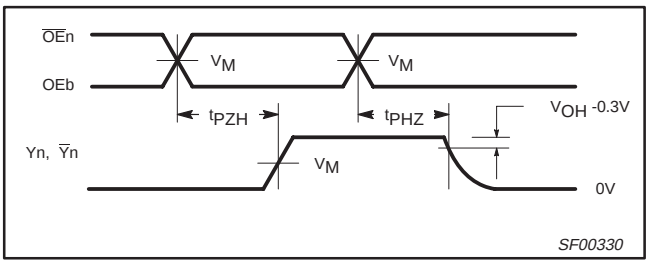
For all waveforms, $V_M$ = 1.5V.



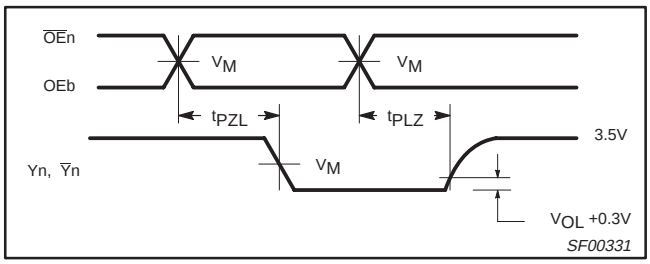

**Waveform 1. For Inverting Outputs**




**Waveform 2. For Non-inverting Outputs**

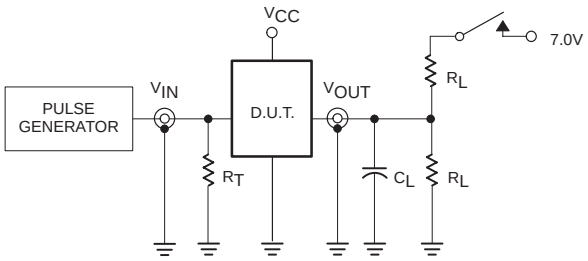



**Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level**

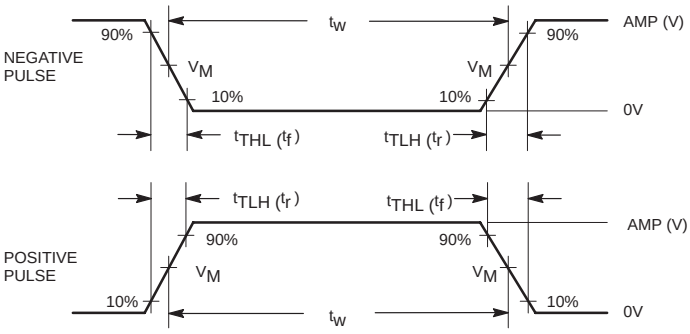



**Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level**

## TEST CIRCUIT AND WAVEFORMS




**Test Circuit for Open Collector Outputs**




**Input Pulse Definition**

**SWITCH POSITION**

| TEST | SWITCH |
|---|---|
| $t_{PLZ}$ | closed |
| $t_{PZL}$ | closed |
| All other | open |

**DEFINITIONS:**

$R_L$ = Load resistor; see AC electrical characteristics for value.

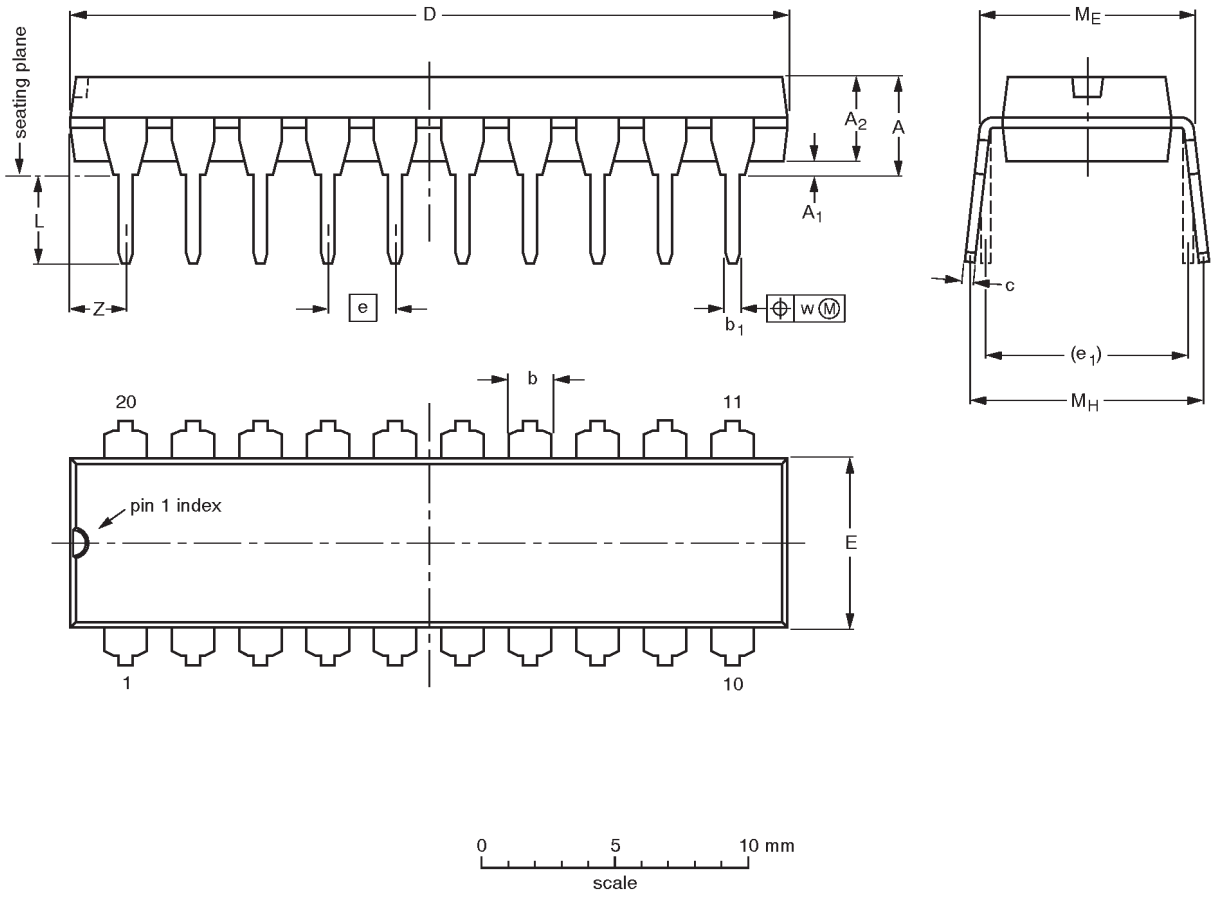
$C_L$ = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

$R_T$ = Termination resistance should be equal to $Z_{OUT}$ of pulse generators.

| family | INPUT PULSE REQUIREMENTS | | | | | |
|---|---|---|---|---|---|---|
| | amplitude | $V_M$ | rep. rate | $t_W$ | $t_{TLH}$ | $t_{THL}$ |
| 74F | 3.0V | 1.5V | 1MHz | 500ns | 2.5ns | 2.5ns |

SF00128

**DIP20: plastic dual in-line package; 20 leads (300 mil)** **SOT146-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

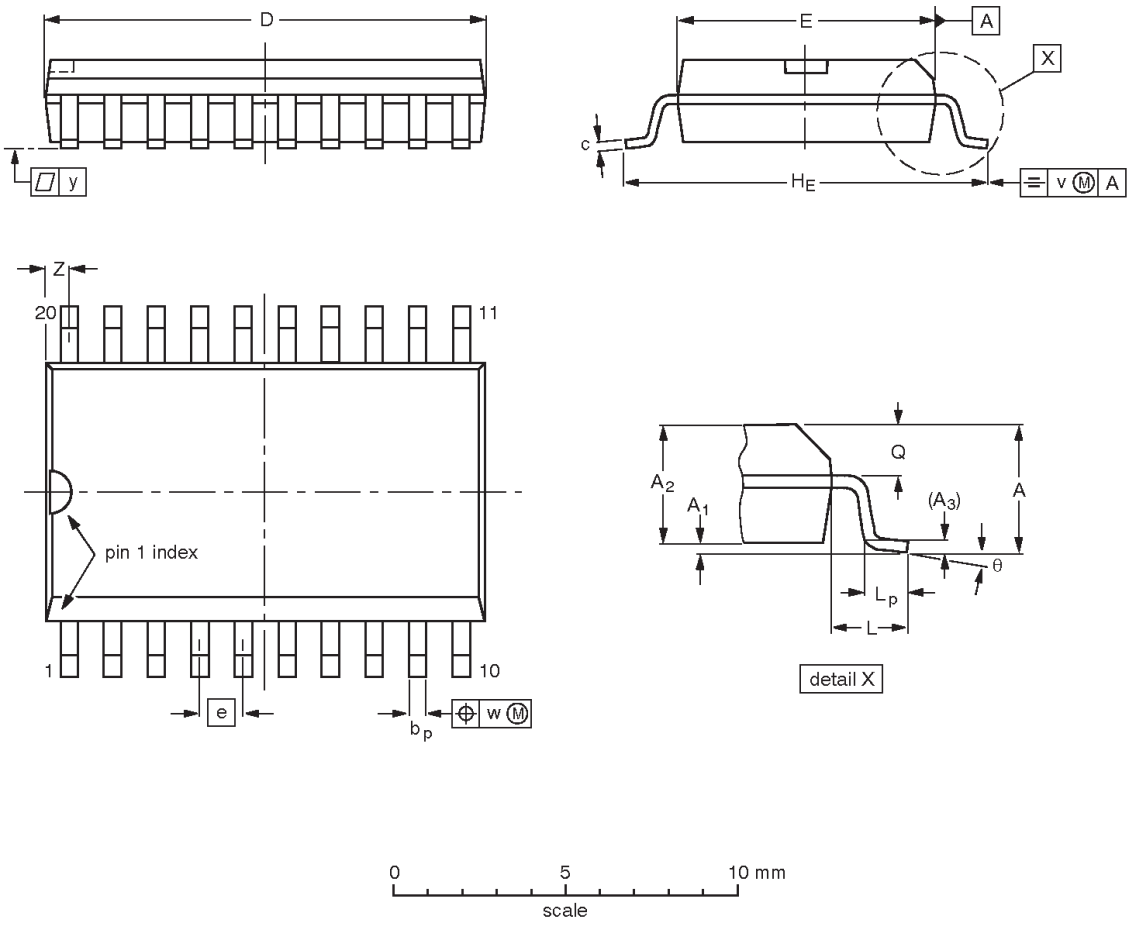
| UNIT | A max. | $A_1$ min. | $A_2$ max. | b | $b_1$ | c | D (1) | E (1) | e | $e_1$ | L | $M_E$ | $M_H$ | w | Z (1) max. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.2 | 0.51 | 3.2 | 1.73<br>1.30 | 0.53<br>0.38 | 0.36<br>0.23 | 26.92<br>26.54 | 6.40<br>6.22 | 2.54 | 7.62 | 3.60<br>3.05 | 8.25<br>7.80 | 10.0<br>8.3 | 0.254 | 2.0 |
| inches | 0.17 | 0.020 | 0.13 | 0.068<br>0.051 | 0.021<br>0.015 | 0.014<br>0.009 | 1.060<br>1.045 | 0.25<br>0.24 | 0.10 | 0.30 | 0.14<br>0.12 | 0.32<br>0.31 | 0.39<br>0.33 | 0.01 | 0.078 |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT146-1 | | | SC603 | | | ~~92-11-17~~<br>95-05-24 |

**SO20: plastic small outline package; 20 leads; body width 7.5 mm** **SOT163-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.65 | 0.30<br>0.10 | 2.45<br>2.25 | 0.25 | 0.49<br>0.36 | 0.32<br>0.23 | 13.0<br>12.6 | 7.6<br>7.4 | 1.27 | 10.65<br>10.00 | 1.4 | 1.1<br>0.4 | 1.1<br>1.0 | 0.25 | 0.25 | 0.1 | 0.9<br>0.4 | $8^o$<br>$0^o$ |
| inches | 0.10 | 0.012<br>0.004 | 0.096<br>0.089 | 0.01 | 0.019<br>0.014 | 0.013<br>0.009 | 0.51<br>0.49 | 0.30<br>0.29 | 0.050 | 0.419<br>0.394 | 0.055 | 0.043<br>0.016 | 0.043<br>0.039 | 0.01 | 0.01 | 0.004 | 0.035<br>0.016 | |

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT163-1 | 075E04 | MS-013AC | | | | ~~95-01-24~~<br>97-05-22 |

**NOTES**

## Data sheet status

| Data sheet status | Product status | Definition [1] |
|---|---|---|
| Objective specification | Development | This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice. |
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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