

DS90CR287/DS90CR288A +3.3V Rising Edge Data Strobe LVDS 28-Bit Channel Link - 85MHz

Check for Samples: [DS90CR287](#), [DS90CR288A](#)

FEATURES

- 20 to 85 MHz Shift Clock Support
- 50% Duty Cycle on Receiver Output Clock
- 2.5 / 0 ns Set & Hold Times on TxINPUTS
- Low Power Consumption
- $\pm 1V$ Common-Mode Range (around +1.2V)
- Narrow Bus Reduces Cable Size and Cost
- Up to 2.38 Gbps Throughput
- Up to 297.5 Mbytes/sec Bandwidth
- 345 mV (typ) Swing LVDS Devices for Low EMI
- PLL Requires no External Components
- Rising Edge Data Strobe
- Compatible with TIA/EIA-644 LVDS Standard
- Low Profile 56-Lead TSSOP Package

DESCRIPTION

The DS90CR287 transmitter converts 28 bits of LVCMOS/LVTTL data into four LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. Every cycle of the transmit clock 28 bits of input data are sampled and transmitted.

The DS90CR288A receiver converts the four LVDS data streams back into 28 bits of LVCMOS/LVTTL data. At a transmit clock frequency of 85 MHz, 28 bits of TTL data are transmitted at a rate of 595 Mbps per LVDS data channel. Using a 85 MHz clock, the data throughput is 2.38 Gbit/s (297.5 Mbytes/sec).

This chipset is an ideal means to solve EMI and cable size problems associated with wide, high-speed TTL interfaces.

Block Diagram

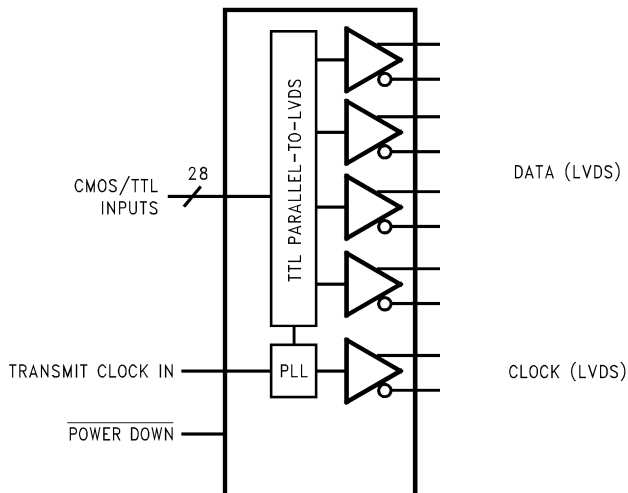


Figure 1. DS90CR287
See Package Number DGG-56 (TSSOP)

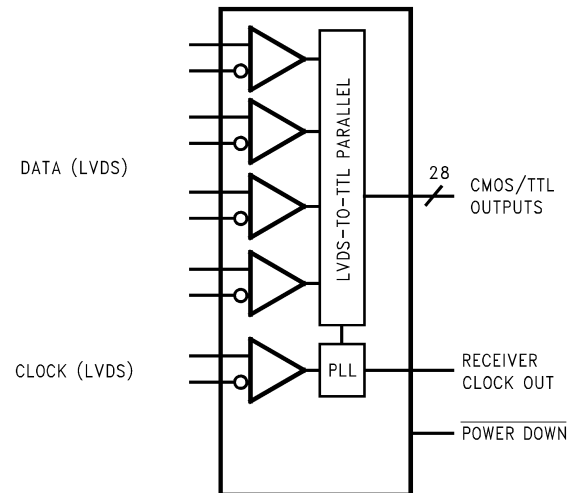


Figure 2. DS90CR288A
See Package Number DGG-56 (TSSOP)



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Pin Diagram for TSSOP Packages

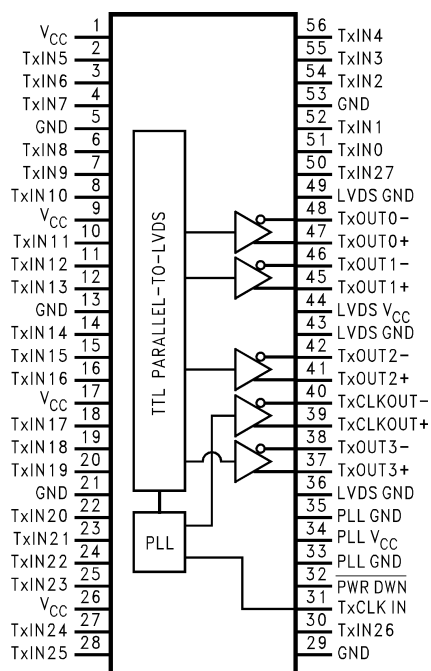


Figure 3. DS90CR287

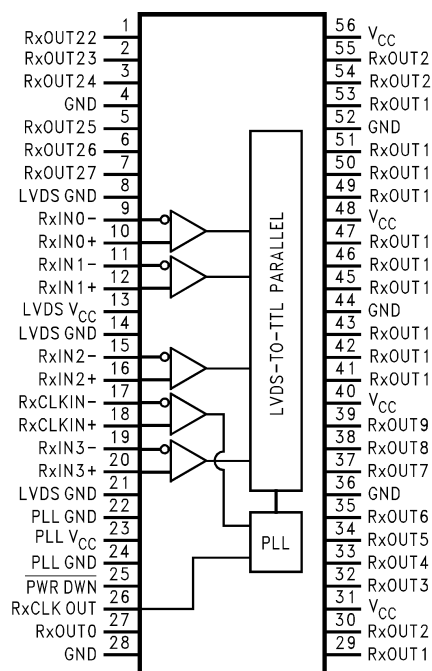


Figure 4. DS90CR288A

Typical Application

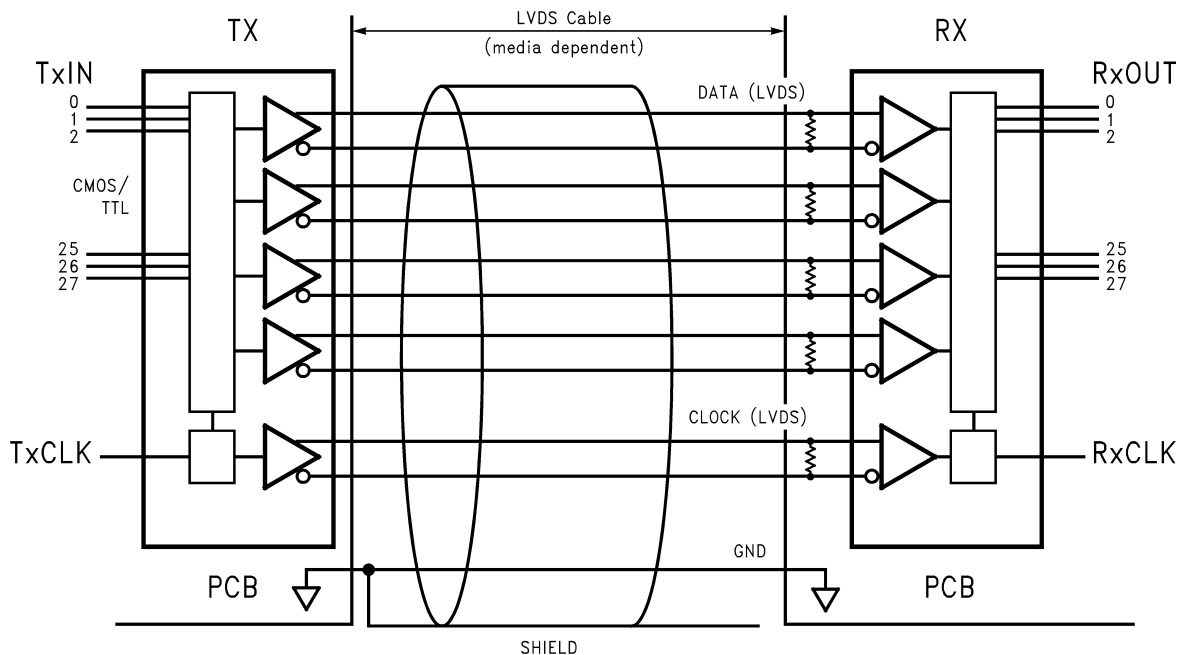


Figure 5. DS90CR288A



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾

Supply Voltage (V_{CC})			-0.3V to +4V
CMOS/TTL Input Voltage			-0.5V to ($V_{CC} + 0.3V$)
CMOS/TTL Output Voltage			-0.3V to ($V_{CC} + 0.3V$)
LVDS Receiver Input Voltage			-0.3V to ($V_{CC} + 0.3V$)
LVDS Driver Output Voltage			-0.3V to ($V_{CC} + 0.3V$)
LVDS Output Short Circuit Duration			Continuous
Junction Temperature			+150°C
Storage Temperature			-65°C to +150°C
Lead Temperature (Soldering, 4 sec.)			+260°C
Solder Reflow Temperature			
Maximum Package Power Dissipation @ +25°C	TSSOP Package	DS90CR287	1.63 W
		DS90CR288A	1.61 W
Package Derating		DS90CR287	12.5 mW/°C above +25°C
		DS90CR288A	12.4 mW/°C above +25°C
ESD Rating		(HBM, 1.5k Ω , 100pF)	> 7kV
		(EIAJ, 0 Ω , 200pF)	> 700V
		Latch Up Tolerance @ +25°C	> $\pm 300mA$

- (1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. "Electrical Characteristics" specify conditions for device operation.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Operating Free Air Temperature (T_A)	-10	+25	+70	°C
Receiver Input Range	0		2.4	V
Supply Noise Voltage (V_{CC})			100	mV _{pp}

Electrical Characteristics⁽¹⁾

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ ⁽²⁾	Max	Units	
LVCMOS/LVTTL DC SPECIFICATIONS							
V _{IH}	High Level Input Voltage		2.0		V _{CC}	V	
V _{IL}	Low Level Input Voltage		GND		0.8	V	
V _{OH}	High Level Output Voltage	I _{OH} = −0.4 mA	2.7	3.3		V	
V _{OL}	Low Level Output Voltage	I _{OL} = 2 mA		0.06	0.3	V	
V _{CL}	Input Clamp Voltage	I _{CL} = −18 mA		−0.79	−1.5	V	
I _{IN}	Input Current	V _{IN} = 0.4V, 2.5V or V _{CC}		+1.8	+15	μA	
		V _{IN} = GND	−10	0		μA	
I _{OS}	Output Short Circuit Current	V _{OUT} = 0V		−60	−120	mA	
LVDS DRIVER DC SPECIFICATIONS							
V _{OD}	Differential Output Voltage	R _L = 100Ω	250	290	450	mV	
ΔV _{OD}	Change in V _{OD} between Complimentary Output States				35	mV	
V _{OS}	Offset Voltage ⁽³⁾		1.125	1.25	1.375	V	
ΔV _{OS}	Change in V _{OS} between Complimentary Output States				35	mV	
I _{OS}	Output Short Circuit Current	V _{OUT} = 0V, R _L = 100Ω		−3.5	−5	mA	
I _{OZ}	Output TRI-STATE Current	PWR DWN = 0V, V _{OUT} = 0V or V _{CC}		±1	±10	μA	
LVDS RECEIVER DC SPECIFICATIONS							
V _{TH}	Differential Input High Threshold	V _{CM} = +1.2V			+100	mV	
V _{TL}	Differential Input Low Threshold		−100			mV	
I _{IN}	Input Current	V _{IN} = +2.4V, V _{CC} = 3.6V			±10	μA	
		V _{IN} = 0V, V _{CC} = 3.6V			±10	μA	
TRANSMITTER SUPPLY CURRENT							
I _{CCTW}	Transmitter Supply Current Worst Case (with Loads) ⁽⁴⁾	R _L = 100Ω, C _L = 5 pF, Worst Case Pattern Figure 6, Figure 7	f = 33 MHz		31	45	mA
			f = 40 MHz		32	50	mA
			f = 66 MHz		37	55	mA
			f = 85 MHz		42	60	mA
I _{CCTZ}	Transmitter Supply Current Power Down ⁽⁴⁾	PWR DWN = Low Driver Outputs in TRI-STATE under Powerdown Mode		10	55	μA	
RECEIVER SUPPLY CURRENT							
I _{CCRW}	Receiver Supply Current Worst Case	C _L = 8 pF, Worst Case Pattern Figure 6, Figure 8	f = 33 MHz		49	70	mA
			f = 40 MHz		53	75	mA
			f = 66 MHz		81	114	mA
			f = 85 MHz		96	135	mA
I _{CCRZ}	Receiver Supply Current Power Down	PWR DWN = Low Receiver Outputs Stay Low during Powerdown Mode		140	400	μA	

(1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. "Electrical Characteristics" specify conditions for device operation.

(2) Typical values are given for V_{CC} = 3.3V and T_A = +25°C.

(3) V_{OS} previously referred as V_{CM}.

(4) Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{OD} and ΔV_{OD}).

Transmitter Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter		Min	Typ ⁽¹⁾	Max	Units
LLHT	LVDS Low-to-High Transition Time Figure 7			0.75	1.5	ns
LHLT	LVDS High-to-Low Transition Time Figure 7			0.75	1.5	ns
TCIT	TxCLK IN Transition Time Figure 9		1.0		6.0	ns
TPPos0	Transmitter Output Pulse Position for Bit0 Figure 19	f = 85 MHz	–0.20	0	0.20	ns
TPPos1	Transmitter Output Pulse Position for Bit1		1.48	1.68	1.88	ns
TPPos2	Transmitter Output Pulse Position for Bit2		3.16	3.36	3.56	ns
TPPos3	Transmitter Output Pulse Position for Bit3		4.84	5.04	5.24	ns
TPPos4	Transmitter Output Pulse Position for Bit4		6.52	6.72	6.92	ns
TPPos5	Transmitter Output Pulse Position for Bit5		8.20	8.40	8.60	ns
TPPos6	Transmitter Output Pulse Position for Bit6		9.88	10.08	10.28	ns
TCIP	TxCLK IN Period Figure 10		11.76	T	50	ns
TCIH	TxCLK IN High Time Figure 10		0.35T	0.5T	0.65T	ns
TCIL	TxCLK IN Low Time Figure 10		0.35T	0.5T	0.65T	ns
TSTC	TxIN Setup to TxCLK IN Figure 10	f = 85 MHz	2.5			ns
THTC	TxIN Hold to TxCLK IN Figure 10		0			ns
TCCD	TxCLK IN to TxCLK OUT Delay Figure 12	T _A = 25°C, V _{CC} = 3.3V	3.8		6.3	ns
TPLLS	Transmitter Phase Lock Loop Set Figure 14				10	ms
TPDD	Transmitter Powerdown Delay Figure 17				100	ns
TJIT	TxCLK IN Cycle-to-Cycle Jitter (Input clock requirement)				2	ns

(1) Typical values are given for V_{CC} = 3.3V and T_A = +25°C.

Receiver Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter		Min	Typ ⁽¹⁾	Max	Units
CLHT	CMOS/TTL Low-to-High Transition Time Figure 8			2	3.5	ns
CHLT	CMOS/TTL High-to-Low Transition Time Figure 8			1.8	3.5	ns
RSPos0	Receiver Input Strobe Position for Bit 0 Figure 20	f = 85 MHz	0.49	0.84	1.19	ns
RSPos1	Receiver Input Strobe Position for Bit 1		2.17	2.52	2.87	ns
RSPos2	Receiver Input Strobe Position for Bit 2		3.85	4.20	4.55	ns
RSPos3	Receiver Input Strobe Position for Bit 3		5.53	5.88	6.23	ns
RSPos4	Receiver Input Strobe Position for Bit 4		7.21	7.56	7.91	ns
RSPos5	Receiver Input Strobe Position for Bit 5		8.89	9.24	9.59	ns
RSPos6	Receiver Input Strobe Position for Bit 6		10.57	10.92	11.27	ns
RSKM	RxIN Skew Margin ⁽²⁾ Figure 21	f = 85 MHz	290			ps
RCOP	RxCLK OUT Period Figure 11		11.76	T	50	ns
RCOH	RxCLK OUT High Time Figure 11	f = 85 MHz	4	5	6.5	ns
RCOL	RxCLK OUT Low Time Figure 11		3.5	5	6	ns
RSRC	RxOUT Setup to RxCLK OUT Figure 11		3.5			ns
RHRC	RxOUT Hold to RxCLK OUT Figure 11		3.5			ns
RCCD	RxCLK IN to RxCLK OUT Delay @ 25°C, V _{CC} = 3.3V ⁽³⁾ Figure 13		5.5	7	9.5	ns
RPLLS	Receiver Phase Lock Loop Set Figure 15				10	ms
RPDD	Receiver Powerdown Delay Figure 18				1	μs

(1) Typical values are given for V_{CC} = 3.3V and T_A = +25°C.

(2) Receiver Skew Margin is defined as the valid data sampling region at the receiver inputs. This margin takes into account the transmitter pulse positions (min and max) and the receiver input setup and hold time (internal data sampling window-RSPOS). This margin allows LVDS interconnect skew, inter-symbol interference (both dependent on type/length of cable), and source clock (less than 150 ps).

(3) Total latency for the channel link chipset is a function of clock period and gate delays through the transmitter (TCCD) and receiver (RCCD). The total latency for the 217/287 transmitter and 218/288A receiver is: (T + TCCD) + (2*T + RCCD), where T = Clock period.

AC Timing Diagrams

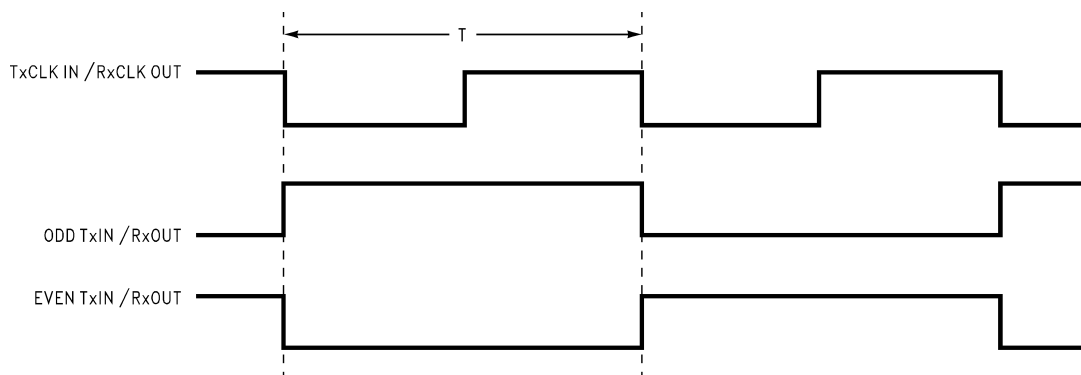


Figure 6. "Worst Case" Test Pattern

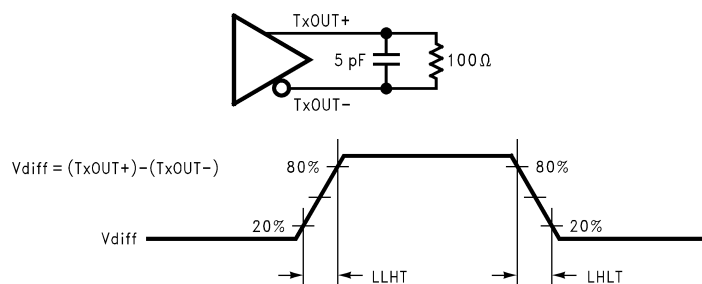


Figure 7. DS90CR287 (Transmitter) LVDS Output Load and Transition Times

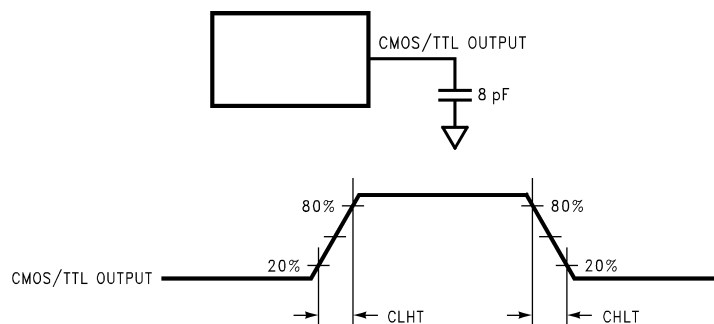


Figure 8. DS90CR288A (Receiver) CMOS/TTL Output Load and Transition Times

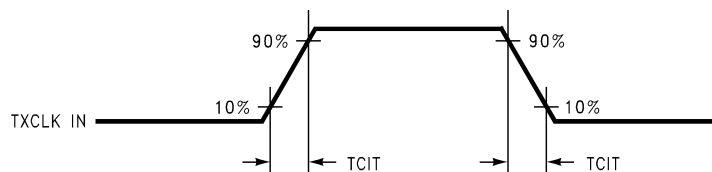


Figure 9. DS90CR287 (Transmitter) Input Clock Transition Time

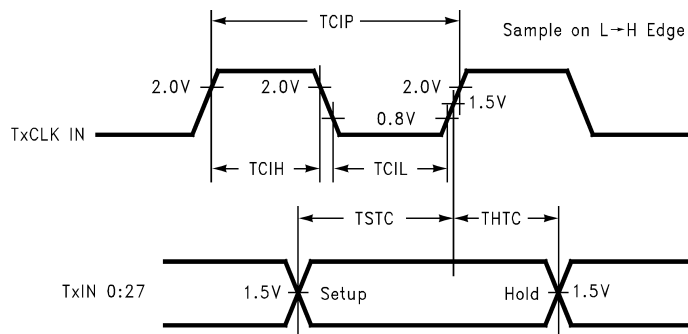


Figure 10. DS90CR287 (Transmitter) Setup/Hold and High/Low Times

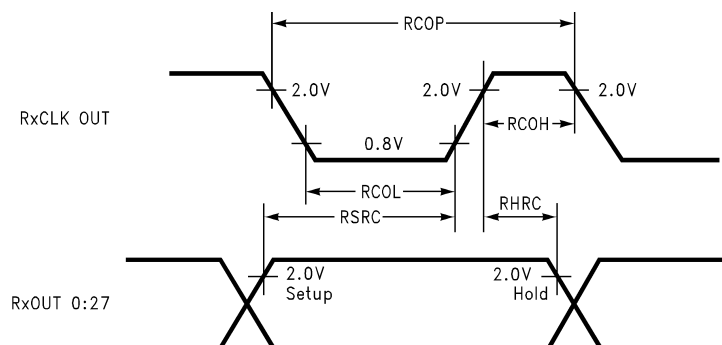


Figure 11. DS90CR288A (Receiver) Setup/Hold and High/Low Times

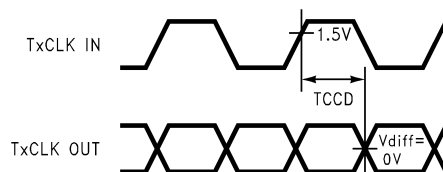


Figure 12. DS90CR287 (Transmitter) Clock In to Clock Out Delay

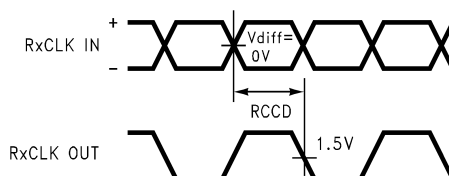


Figure 13. DS90CR288A (Receiver) Clock In to Clock Out Delay

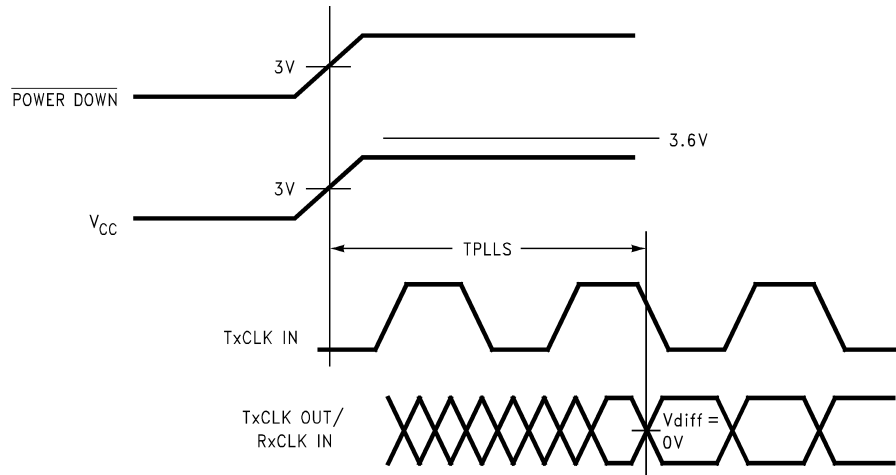


Figure 14. DS90CR287 (Transmitter) Phase Lock Loop Set Time

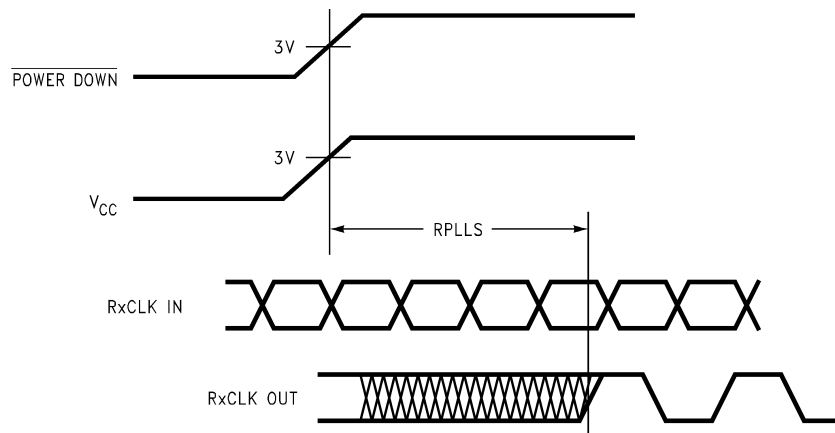


Figure 15. DS90CR288A (Receiver) Phase Lock Loop Set Time

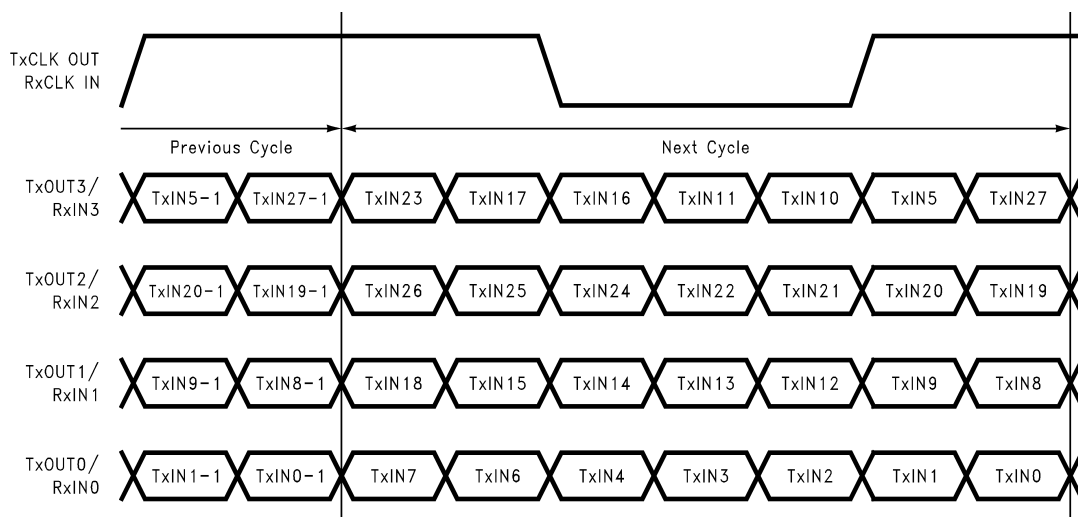


Figure 16. 28 Parallel TTL Data Inputs Mapped to LVDS Outputs

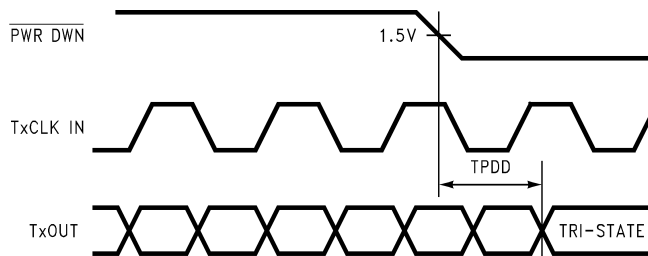


Figure 17. Transmitter Powerdown Delay

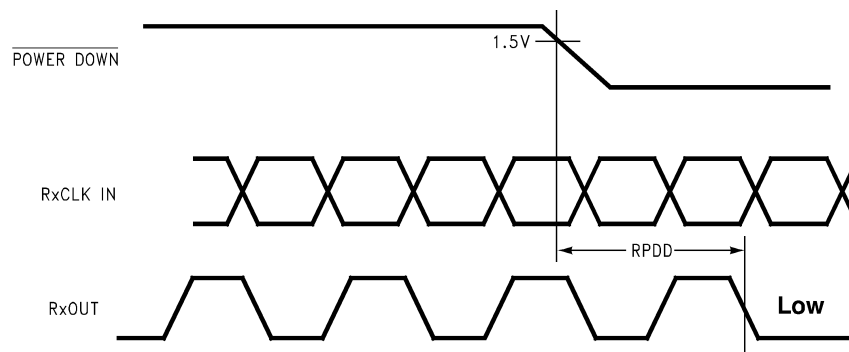


Figure 18. Receiver Powerdown Delay

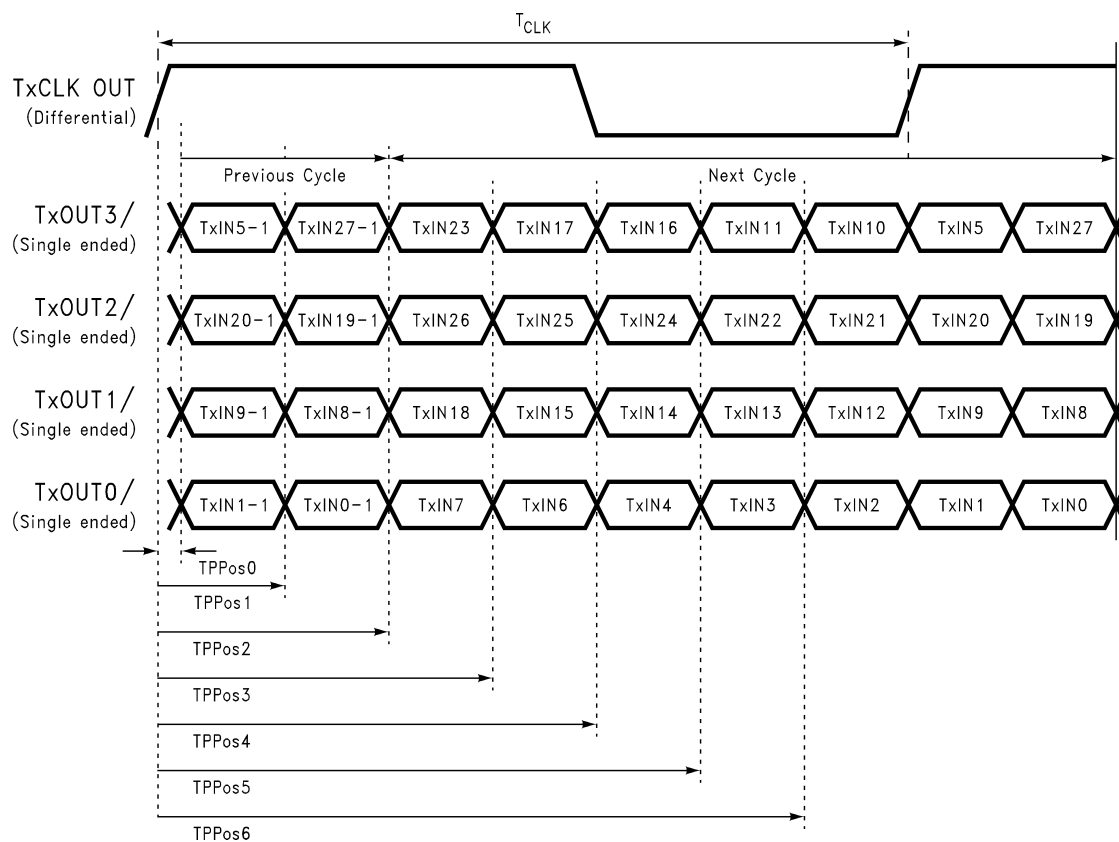


Figure 19. Transmitter LVDS Output Pulse Position Measurement

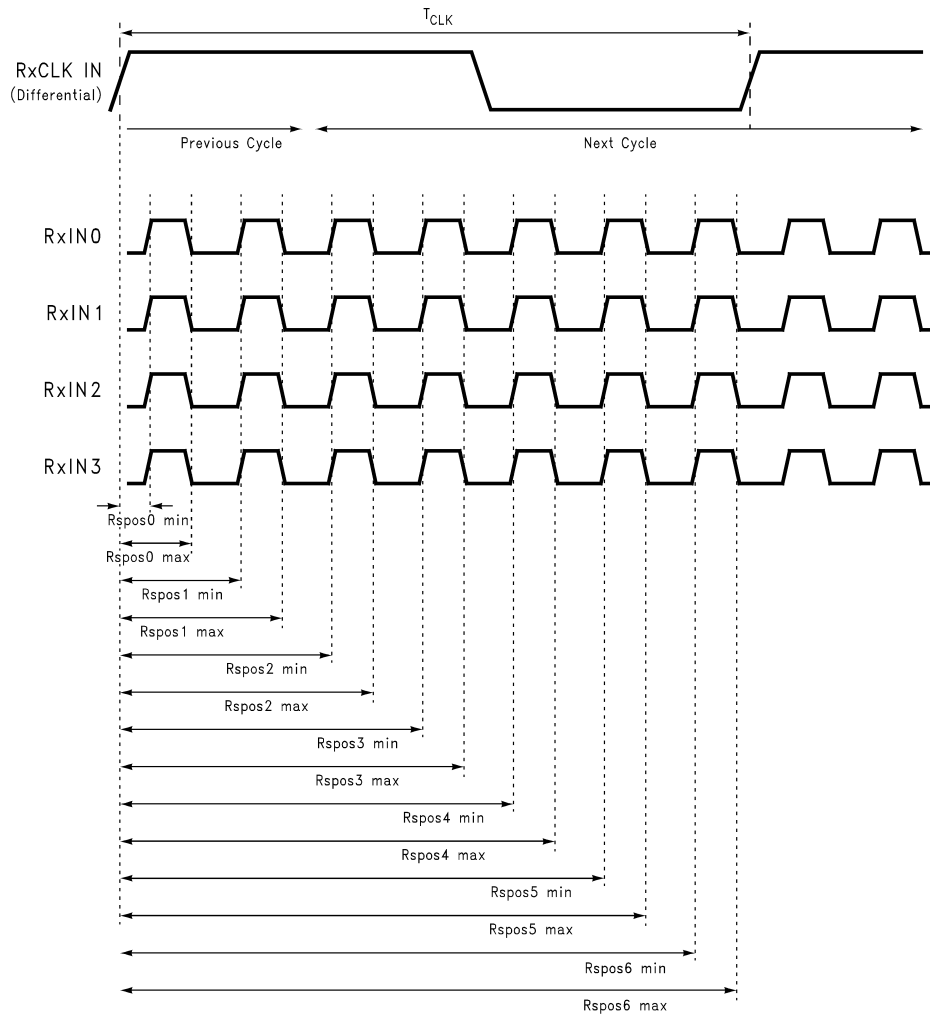
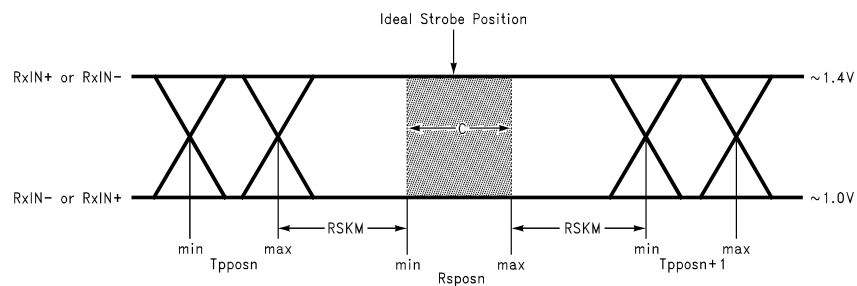


Figure 20. Receiver LVDS Input Strobe Position



C—Setup and Hold Time (Internal data sampling window) defined by Rspos (receiver input strobe position) min and max

Tppos—Transmitter output pulse position (min and max)

$RSKM \geq \text{Cable Skew (type, length)} + \text{Source Clock Jitter (cycle to cycle)}^{(1)} + \text{ISI (Inter-symbol interference)}^{(2)}$

Cable Skew—typically 10 ps–40 ps per foot, media dependent

- (1) Cycle-to-cycle jitter is less than 150ps at 85MHz.
- (2) ISI is dependent on interconnect length; may be zero.

Figure 21. Receiver LVDS Input Skew Margin

DS90CR287 DGG (TSSOP) Package PIN DESCRIPTION — Channel Link Transmitter

Pin Name	I/O	No.	Description
TxIN	I	28	TTL level input.
TxOUT+	O	4	Positive LVDS differential data output.
TxOUT–	O	4	Negative LVDS differential data output.
TxCLK IN	I	1	TTL level clock input. The rising edge acts as data strobe. Pin name TxCLK IN. See APPLICATIONS INFORMATION section.
TxCLK OUT+	O	1	Positive LVDS differential clock output.
TxCLK OUT–	O	1	Negative LVDS differential clock output.
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. Assertion (low input) TRI-STATES the outputs, ensuring low current at power down. See APPLICATIONS INFORMATION section.
V _{CC}	I	4	Power supply pins for TTL inputs.
GND	I	5	Ground pins for TTL inputs.
PLL V _{CC}	I	1	Power supply pin for PLL.
PLL GND	I	2	Ground pins for PLL.
LVDS V _{CC}	I	1	Power supply pin for LVDS outputs.
LVDS GND	I	3	Ground pins for LVDS outputs.

DS90CR288A DGG (TSSOP) Package PIN DESCRIPTION — Channel Link Receiver

Pin Name	I/O	No.	Description
RxIN+	I	4	Positive LVDS differential data inputs.
RxIN–	I	4	Negative LVDS differential data inputs.
RxOUT	O	28	TTL level data outputs.
RxCLK IN+	I	1	Positive LVDS differential clock input.
RxCLK IN–	I	1	Negative LVDS differential clock input.
RxCLK OUT	O	1	TTL level clock output. The rising edge acts as data strobe. Pin name RxCLK OUT.
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. When asserted (low input) the receiver outputs are low.
V _{CC}	I	4	Power supply pins for TTL outputs.
GND	I	5	Ground pins for TTL outputs.
PLL V _{CC}	I	1	Power supply for PLL.
PLL GND	I	2	Ground pin for PLL.
LVDS V _{CC}	I	1	Power supply pin for LVDS inputs.
LVDS GND	I	3	Ground pins for LVDS inputs.

APPLICATIONS INFORMATION

The TSSOP version of the DS90CR287 and DS90CR288A are backward compatible with the existing 5V Channel Link transmitter/receiver pair (DS90CR283, DS90CR284). To upgrade from a 5V to a 3.3V system the following must be addressed:

1. Change 5V power supply to 3.3V. Provide this supply to the V_{CC} , LVDS V_{CC} and PLL V_{CC} .
2. Transmitter input and control inputs except 3.3V TTL/CMOS levels. They are not 5V tolerant.
3. The receiver powerdown feature when enabled will lock receiver output to a logic low.

The Channel Link devices are intended to be used in a wide variety of data transmission applications. Depending upon the application the interconnecting media may vary. For example, for lower data rate (clock rate) and shorter cable lengths (< 2m), the media electrical performance is less critical. For higher speed/long distance applications the media's performance becomes more critical. Certain cable constructions provide tighter skew (matched electrical length between the conductors and pairs). Additional applications information can be found in the following Interface Application Notes:

AN = ####	Topic
AN-1041 (SNLA218)	Introduction to Channel Link
AN-1108(SNLA008)	Channel Link PCB and Interconnect Design-In Guidelines
AN-806 (SNLA026)	Transmission Line Theory
AN-905 (SNLA035)	Transmission Line Calculations and Differential Impedance
AN-916 (SNLA219)	Cable Information

CABLES: A cable interface between the transmitter and receiver needs to support the differential LVDS pairs. The 21-bit CHANNEL LINK chipset (DS90CR217/218A) requires four pairs of signal wires and the 28-bit CHANNEL LINK chipset (DS90CR287/288A) requires five pairs of signal wires. The ideal cable/connector interface would have a constant 100Ω differential impedance throughout the path. It is also recommended that cable skew remain below 140ps (@ 85 MHz clock rate) to maintain a sufficient data sampling window at the receiver.

In addition to the four or five cable pairs that carry data and clock, it is recommended to provide at least one additional conductor (or pair) which connects ground between the transmitter and receiver. This low impedance ground provides a common-mode return path for the two devices. Some of the more commonly used cable types for point-to-point applications include flat ribbon, flex, twisted pair and Twin-Coax. All are available in a variety of configurations and options. Flat ribbon cable, flex and twisted pair generally perform well in short point-to-point applications while Twin-Coax is good for short and long applications. When using ribbon cable, it is recommended to place a ground line between each differential pair to act as a barrier to noise coupling between adjacent pairs. For Twin-Coax cable applications, it is recommended to utilize a shield on each cable pair. All extended point-to-point applications should also employ an overall shield surrounding all cable pairs regardless of the cable type. This overall shield results in improved transmission parameters such as faster attainable speeds, longer distances between transmitter and receiver and reduced problems associated with EMS or EMI.

The high-speed transport of LVDS signals has been demonstrated on several types of cables with excellent results. However, the best overall performance has been seen when using Twin-Coax cable. Twin-Coax has very low cable skew and EMI due to its construction and double shielding. All of the design considerations discussed here and listed in the supplemental application notes provide the subsystem communications designer with many useful guidelines. It is recommended that the designer assess the tradeoffs of each application thoroughly to arrive at a reliable and economical cable solution.

RECEIVER FAILSAFE FEATURE: These receivers have input failsafe bias circuitry to guarantee a stable receiver output for floating or terminated receiver inputs. Under these conditions receiver inputs will be in a HIGH state. If a clock signal is present, data outputs will all be HIGH; if the clock input is also floating/terminated, data outputs will remain in the last valid state. A floating/terminated clock input will result in a HIGH clock output.

BOARD LAYOUT: To obtain the maximum benefit from the noise and EMI reductions of LVDS, attention should be paid to the layout of differential lines. Lines of a differential pair should always be adjacent to eliminate noise interference from other signals and take full advantage of the noise canceling of the differential signals. The board designer should also try to maintain equal length on signal traces for a given differential pair. As with any high-speed design, the impedance discontinuities should be limited (reduce the numbers of vias and no 90 degree angles on traces). Any discontinuities which do occur on one signal line should be mirrored in the other

line of the differential pair. Care should be taken to ensure that the differential trace impedance match the differential impedance of the selected physical media (this impedance should also match the value of the termination resistor that is connected across the differential pair at the receiver's input). Finally, the location of the CHANNEL LINK TxOUT/RxIN pins should be as close as possible to the board edge so as to eliminate excessive pcb runs. All of these considerations will limit reflections and crosstalk which adversely effect high frequency performance and EMI.

INPUTS: The TxIN and control pin inputs are compatible with LVTTTL and LVCMOS levels. This pins are not 5V tolerant.

UNUSED INPUTS: All unused inputs at the TxIN inputs of the transmitter may be tied to ground or left no connect. All unused outputs at the RxOUT outputs of the receiver must then be left floating.

TERMINATION: Use of current mode drivers requires a terminating resistor across the receiver inputs. The CHANNEL LINK chipset will normally require a single 100Ω resistor between the true and complement lines on each differential pair of the receiver input. The actual value of the termination resistor should be selected to match the differential mode characteristic impedance (90Ω to 120Ω typical) of the cable. Figure 22 shows an example. No additional pull-up or pull-down resistors are necessary as with some other differential technologies such as PECL. Surface mount resistors are recommended to avoid the additional inductance that accompanies leaded resistors. These resistors should be placed as close as possible to the receiver input pins to reduce stubs and effectively terminate the differential lines.

DECOUPLING CAPACITORS: Bypassing capacitors are needed to reduce the impact of switching noise which could limit performance. For a conservative approach three parallel-connected decoupling capacitors (Multi-Layered Ceramic type in surface mount form factor) between each V_{CC} and the ground plane(s) are recommended. The three capacitor values are 0.1 μF, 0.01 μF and 0.001 μF. An example is shown in Figure 23. The designer should employ wide traces for power and ground and ensure each capacitor has its own via to the ground plane. If board space is limiting the number of bypass capacitors, the PLL V_{CC} should receive the most filtering/bypassing. Next would be the LVDS V_{CC} pins and finally the logic V_{CC} pins.

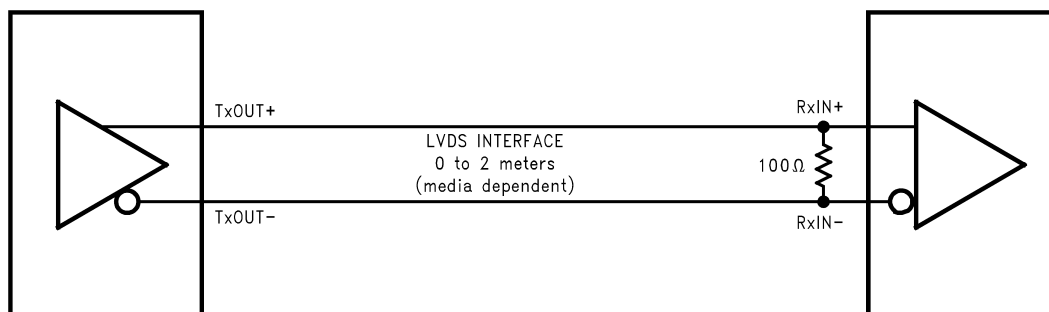


Figure 22. LVDS Serialized Link Termination

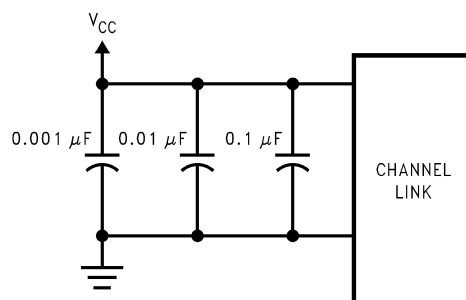


Figure 23. CHANNEL LINK Decoupling Configuration

CLOCK JITTER: The CHANNEL LINK devices employ a PLL to generate and recover the clock transmitted across the LVDS interface. The width of each bit in the serialized LVDS data stream is one-seventh the clock period. For example, a 85 MHz clock has a period of 11.76 ns which results in a data bit width of 1.68 ns. Differential skew (Δt within one differential pair), interconnect skew (Δt of one differential pair to another) and clock jitter will all reduce the available window for sampling the LVDS serial data streams. Care must be taken to ensure that the clock input to the transmitter be a clean low noise signal. Individual bypassing of each V_{CC} to ground will minimize the noise passed on to the PLL, thus creating a low jitter LVDS clock. These measures provide more margin for channel-to-channel skew and interconnect skew as a part of the overall jitter/skew budget.

INPUT CLOCK: The input clock should be present at all times when the part is enabled. If the clock is stopped, the PWR DOWN pin should be asserted to disable the PLL. Once the clock is active again, the part can then be enabled. Do not enable the part without a clock present.

COMMON-MODE vs. DIFFERENTIAL MODE NOISE MARGIN: The typical signal swing for LVDS is 300 mV centered at +1.2V. The CHANNEL LINK receiver supports a 100 mV threshold therefore providing approximately 200 mV of differential noise margin. Common-mode protection is of more importance to the system's operation due to the differential data transmission. LVDS supports an input voltage range of Ground to +2.4V. This allows for a $\pm 1.0V$ shifting of the center point due to ground potential differences and common-mode noise.

TRANSMITTER INPUT CLOCK: The transmitter input clock must always be present when the device is enabled ($\overline{\text{PWR DOWN}} = \text{HIGH}$). If the clock is stopped, the $\overline{\text{PWR DOWN}}$ pin must be used to disable the PLL. The $\overline{\text{PWR DOWN}}$ pin must be held low until after the input clock signal has been reapplied. This will ensure a proper device reset and PLL lock to occur.

POWER SEQUENCING AND POWERDOWN MODE: Outputs of the CHANNEL LINK transmitter remain in TRI-STATE until the power supply reaches 2V. Clock and data outputs will begin to toggle 10 ms after V_{CC} has reached 3V and the Powerdown pin is above 1.5V. Either device may be placed into a powerdown mode at any time by asserting the Powerdown pin (active low). Total power dissipation for each device will decrease to 5 μW (typical).

The transmitter input clock may be applied prior to powering up and enabling the transmitter. The transmitter input clock may also be applied after power up; however, the use of the $\overline{\text{PWR DOWN}}$ pin is required. Do not power up and enable ($\overline{\text{PWR DOWN}} = \text{HIGH}$) the transmitter without a valid clock signal applied to the TxCLK IN pin.

The CHANNEL LINK chipset is designed to protect itself from accidental loss of power to either the transmitter or receiver. If power to the transmit board is lost, the receiver clocks (input and output) stop. The data outputs (RxOUT) retain the states they were in when the clocks stopped. When the receiver board loses power, the receiver inputs are shorted to V_{CC} through an internal diode. Current is limited (5 mA per input) by the fixed current mode drivers, thus avoiding the potential for latchup when powering the device.

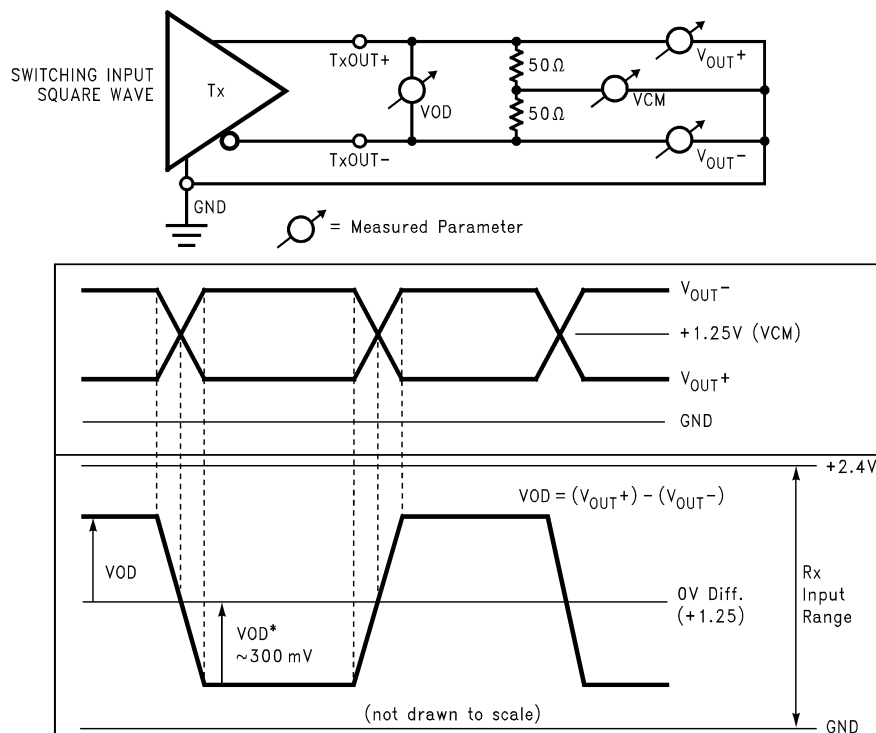


Figure 24. Single-Ended and Differential Waveforms

REVISION HISTORY

Changes from Revision F (March 2013) to Revision G

Page

- Changed layout of National Data Sheet to TI format [16](#)

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS90CR287MTD/NOPB	Active	Production	TSSOP (DGG) 56	34 TUBE	Yes	SN	Level-2-260C-1 YEAR	-10 to 70	DS90CR287MTD >B
DS90CR287MTD/NOPB.B	Active	Production	TSSOP (DGG) 56	34 TUBE	Yes	SN	Level-2-260C-1 YEAR	-10 to 70	DS90CR287MTD >B
DS90CR287MTDX/NOPB	Active	Production	TSSOP (DGG) 56	1000 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-10 to 70	DS90CR287MTD >B
DS90CR287MTDX/NOPB.B	Active	Production	TSSOP (DGG) 56	1000 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-10 to 70	DS90CR287MTD >B
DS90CR287SLC/NOPB	NRND	Production	NFBGA (NZC) 64	360 JEDEC TRAY (10+1)	Yes	SNAGCU	Level-4-260C-72 HR	-	DS90CR287 SLC >B
DS90CR287SLC/NOPB.B	NRND	Production	NFBGA (NZC) 64	360 JEDEC TRAY (10+1)	Yes	SNAGCU	Level-4-260C-72 HR	-10 to 70	DS90CR287 SLC >B
DS90CR288AMTD/NOPB	Active	Production	TSSOP (DGG) 56	34 TUBE	Yes	SN	Level-2-260C-1 YEAR	-10 to 70	DS90CR288AMTD >B
DS90CR288AMTD/NOPB.A	Active	Production	TSSOP (DGG) 56	34 TUBE	Yes	SN	Level-2-260C-1 YEAR	-10 to 70	DS90CR288AMTD >B
DS90CR288AMTDX/NO.A	Active	Production	TSSOP (DGG) 56	1000 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-10 to 70	DS90CR288AMTD >B
DS90CR288AMTDX/NOPB	Active	Production	TSSOP (DGG) 56	1000 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-10 to 70	DS90CR288AMTD >B

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90CR287MTDX/NOPB	TSSOP	DGG	56	1000	330.0	24.4	8.6	14.5	1.8	12.0	24.0	Q1
DS90CR288AMTDX/NOPB	TSSOP	DGG	56	1000	330.0	24.4	8.6	14.5	1.8	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90CR287MTDX/NOPB	TSSOP	DGG	56	1000	356.0	356.0	45.0
DS90CR288AMTDX/NOPB	TSSOP	DGG	56	1000	356.0	356.0	45.0

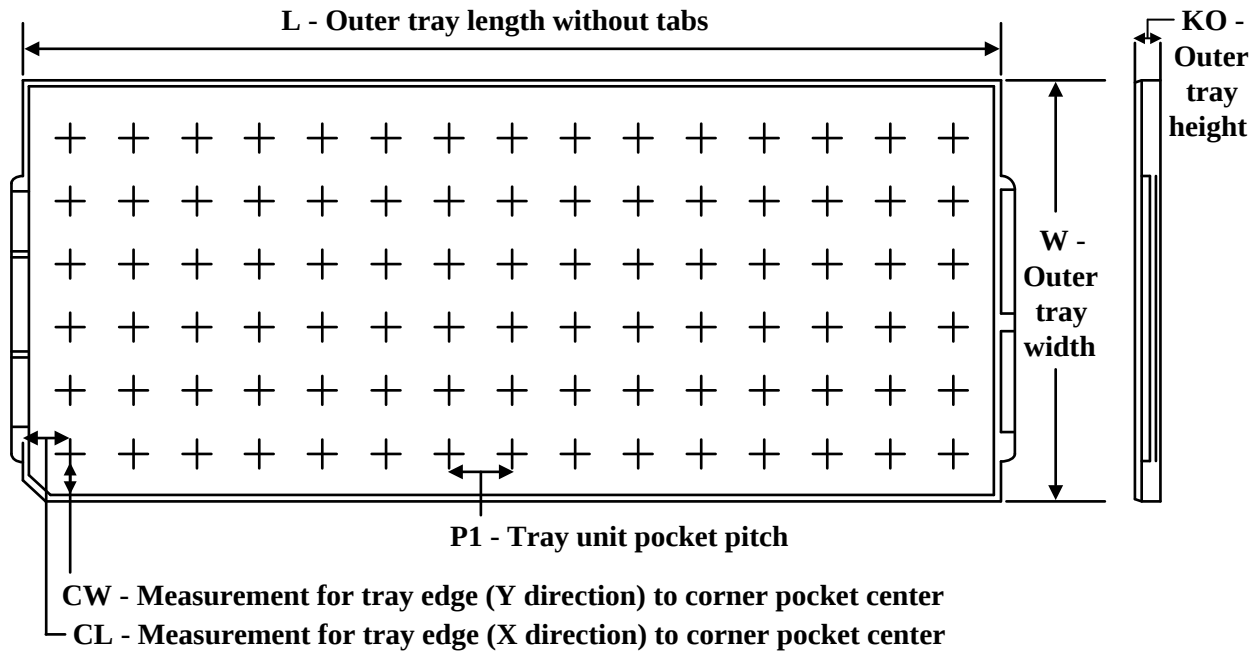
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
DS90CR287MTD/NOPB	DGG	TSSOP	56	34	495	10	2540	5.79
DS90CR287MTD/NOPB.B	DGG	TSSOP	56	34	495	10	2540	5.79
DS90CR288AMTD/NOPB	DGG	TSSOP	56	34	495	10	2540	5.79
DS90CR288AMTD/ NOPB.A	DGG	TSSOP	56	34	495	10	2540	5.79

TRAY

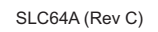


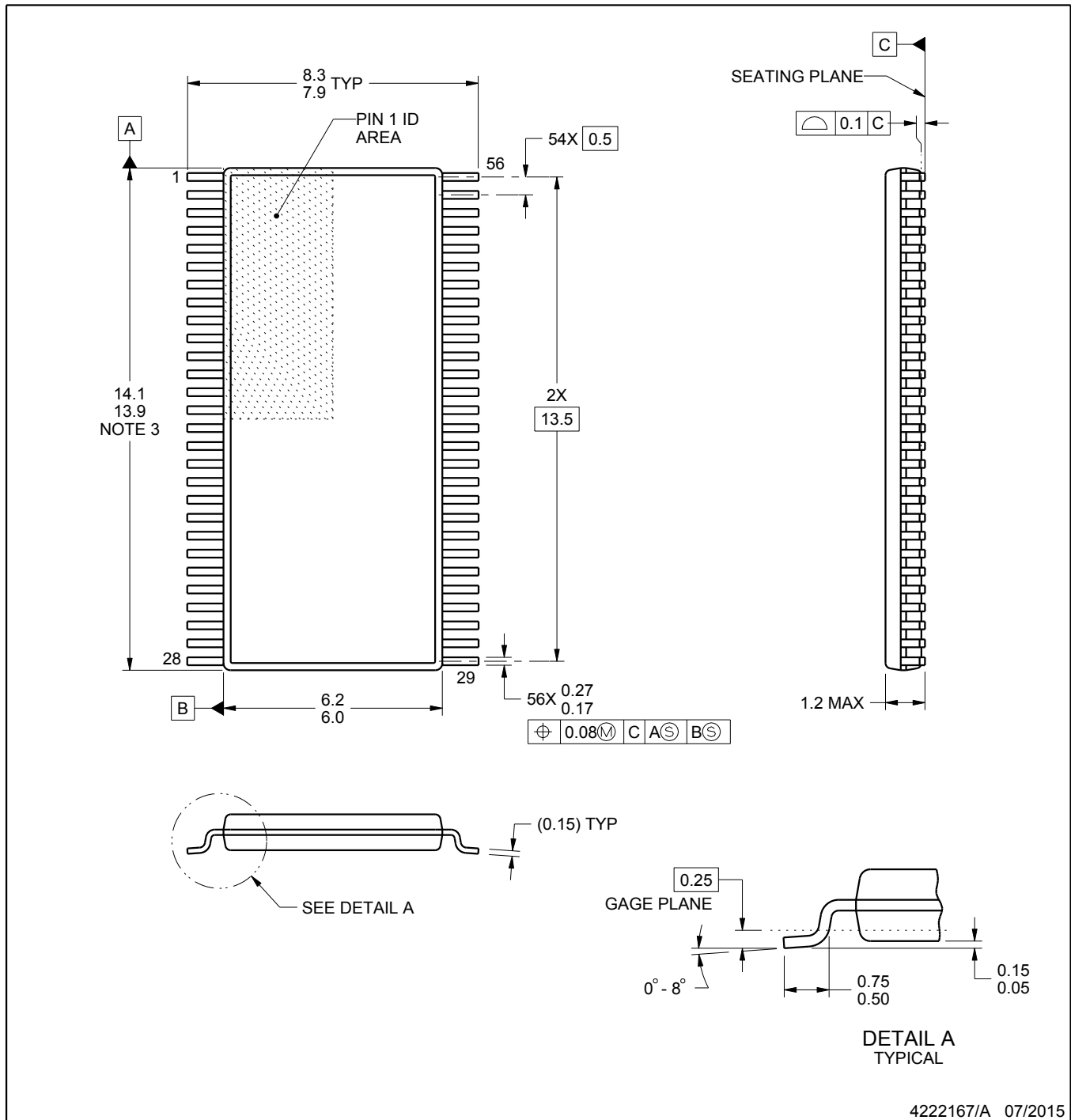
Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (μm)	P1 (mm)	CL (mm)	CW (mm)
DS90CR287SLC/NOPB	NZC	NFBGA	64	360	12 x 30	150	322.6	135.9	7620	10	12.5	12.95
DS90CR287SLC/NOPB.B	NZC	NFBGA	64	360	12 x 30	150	322.6	135.9	7620	10	12.5	12.95

NZC0064A





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NOTES:

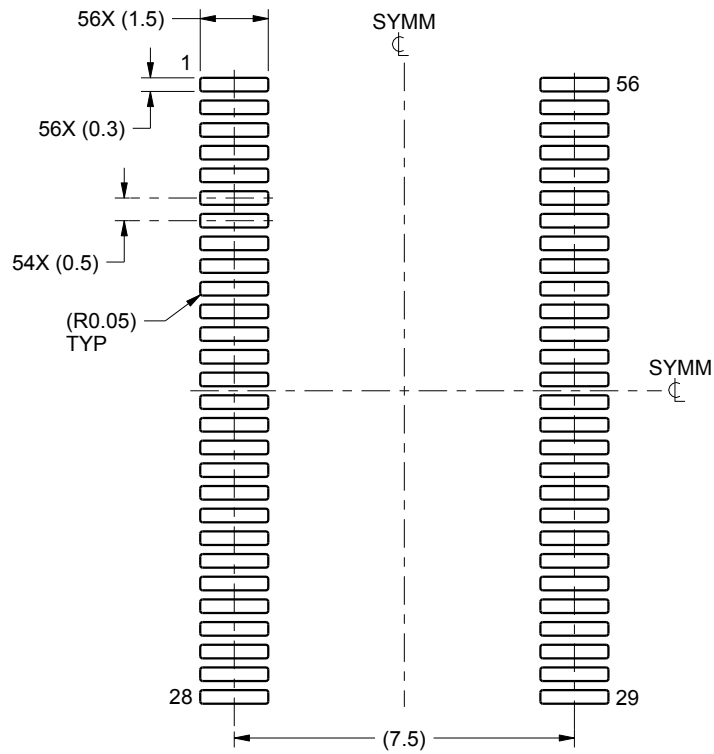
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

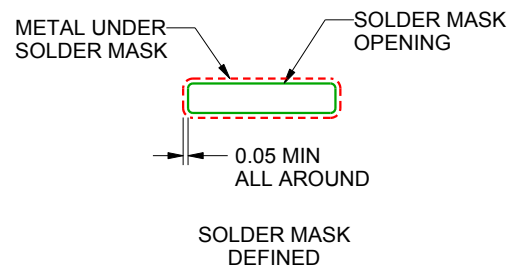
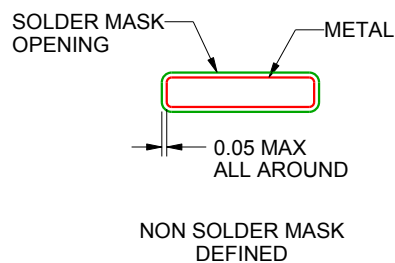
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

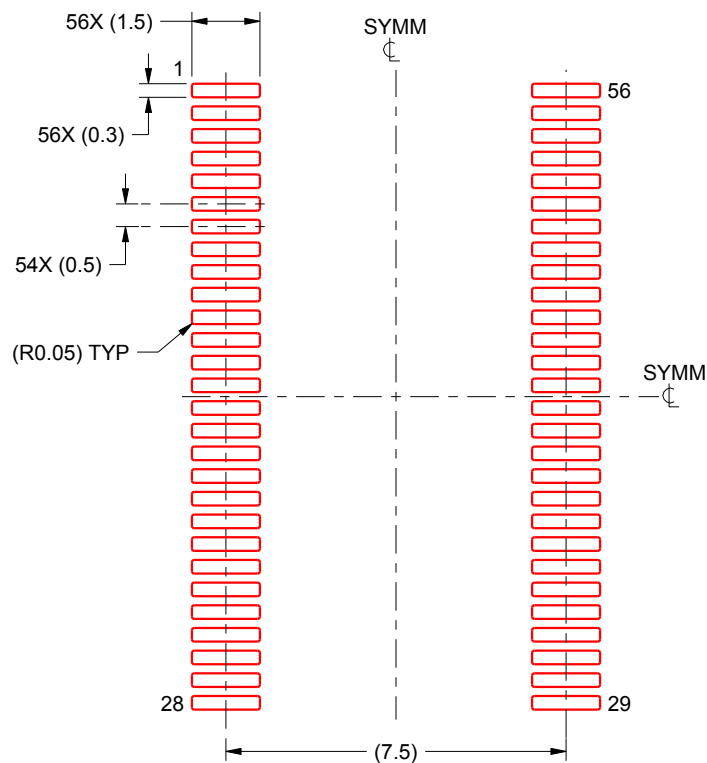
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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