

IR2301(S)

HIGH AND LOW SIDE DRIVER

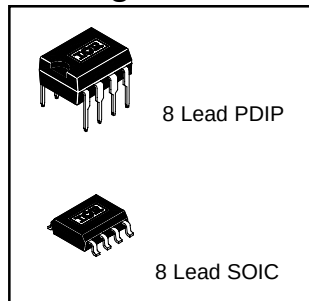
Features

- Floating channel designed for bootstrap operation
Fully operational to +600V
Tolerant to negative transient voltage dV/dt immune
- Gate drive supply range from 5 to 20V
- Undervoltage lockout for both channels
- 3.3V, 5V and 15V input logic compatible
- Matched propagation delay for both channels
- Logic and power ground +/- 5V offset.
- Lower di/dt gate driver for better noise immunity
- Outputs in phase with inputs

Description

The IR2301(S) are high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

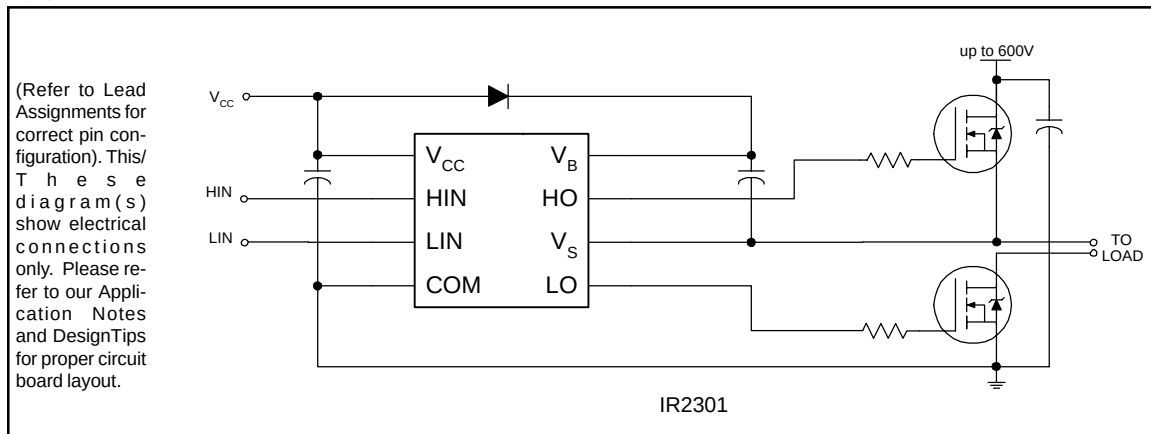
Packages



2106/2301//2108//2109/2302/2304 Feature Comparison

Part	Input logic	Cross-conduction prevention logic	Dead-Time	Ground Pins
2106/2301 21064	HIN/LIN	no	none	COM VSS/COM
2108 21084	HIN/LIN	yes	Internal 540ns Programmable 0.54~5μs	COM VSS/COM
2109/2302 21094	IN/SD	yes	Internal 540ns Programmable 0.54~5μs	COM VSS/COM
2304	HIN/LIN	yes	Internal 100ns	COM

Typical Connection



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating absolute voltage	-0.3	625	V
V_S	High side floating supply offset voltage	$V_B - 25$	$V_B + 0.3$	
V_{HO}	High side floating output voltage	$V_S - 0.3$	$V_B + 0.3$	
V_{CC}	Low side and logic fixed supply voltage	-0.3	25	
V_{LO}	Low side output voltage	-0.3	$V_{CC} + 0.3$	
V_{IN}	Logic input voltage	COM - 0.3	$V_{CC} + 0.3$	
dV_S/dt	Allowable offset supply voltage transient	—	50	
P_D	Package power dissipation @ $T_A \leq +25^\circ\text{C}$	—	1.0	W
	(8 lead PDIP)	—	0.625	
R_{thJA}	Thermal resistance, junction to ambient	—	125	$^\circ\text{C/W}$
	(8 lead SOIC)	—	200	
T_J	Junction temperature	—	150	$^\circ\text{C}$
T_S	Storage temperature	-50	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply absolute voltage	$V_S + 5$	$V_S + 20$	V
V_S	High side floating supply offset voltage	Note 1	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage	5	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage	COM	V_{CC}	
T_A	Ambient temperature	-40	125	$^\circ\text{C}$

Note 1: Logic operational for V_S of -5V to +600V. Logic state held for V_S of -5V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).

Dynamic Electrical Characteristics

 $V_{BIAS} (V_{CC}, V_{BS}) = 15V$, $C_L = 1000\text{ pF}$, $T_A = 25^\circ\text{C}$.

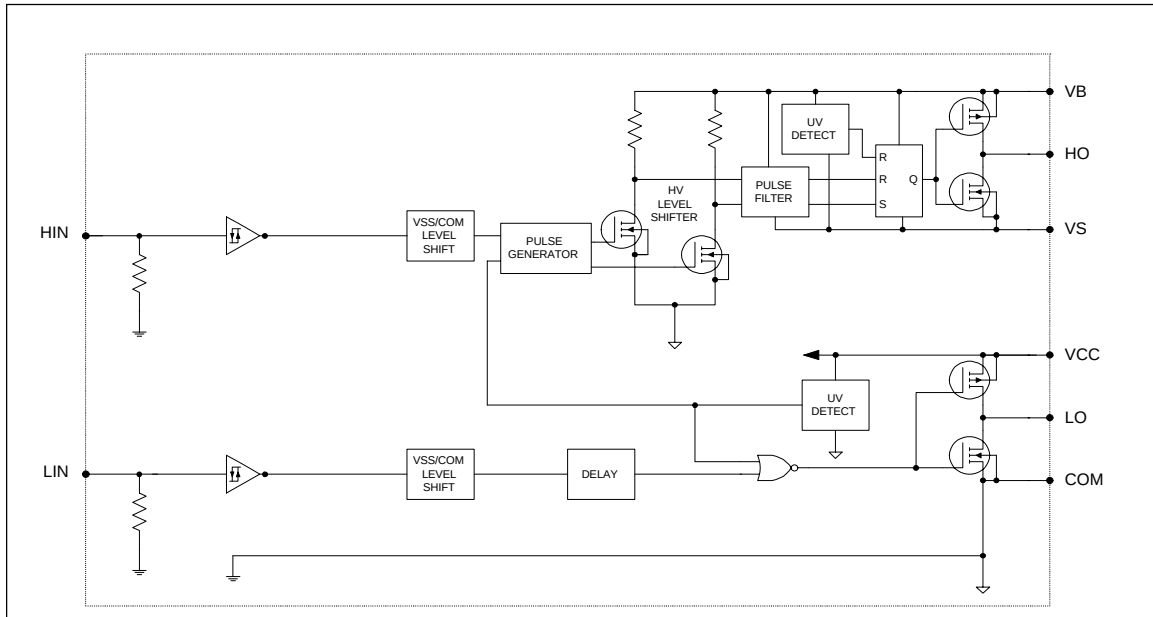
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	220	300	nsec	$V_S = 0V$
t_{off}	Turn-off propagation delay	—	200	280		$V_S = 0V$ or $600V$
MT	Delay matching, HS & LS turn-on/off	—	0	50		
t_r	Turn-on rise time	—	130	220		$V_S = 0V$
t_f	Turn-off fall time	—	50	80		$V_S = 0V$

Static Electrical Characteristics

 $V_{BIAS} (V_{CC}, V_{BS}) = 15V$, and $T_A = 25^\circ\text{C}$ unless otherwise specified. The V_{IL} , V_{IH} and I_{IN} parameters are referenced to COM and are applicable to the respective input leads. The V_O , I_O and R_{on} parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage	2.9	—	—	V	$V_{CC} = 10V$ to $20V$
V_{IL}	Logic "0" input voltage	—	—	0.8		$V_{CC} = 10V$ to $20V$
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	—	0.8	1.4		$I_O = 20\text{ mA}$
V_{OL}	Low level output voltage, V_O	—	0.3	0.6		$I_O = 20\text{ mA}$
I_{LK}	Offset supply leakage current	—	—	50	μA	$V_B = V_S = 600V$
I_{QBS}	Quiescent V_{BS} supply current	20	60	100		$V_{IN} = 0V$ or $5V$
I_{QCC}	Quiescent V_{CC} supply current	50	120	190		$V_{IN} = 0V$ or $5V$
I_{IN+}	Logic "1" input bias current	—	5	20		$V_{IN} = 5V$
I_{IN-}	Logic "0" input bias current	—	—	2		$V_{IN} = 0V$
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	3.3	4.1	5	V	
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	3	3.8	4.7		
V_{CCUVH} V_{BSUVH}	Hysteresis	0.1	0.3	—		
I_{O+}	Output high short circuit pulsed current	120	200	—	mA	$V_O = 0V$, $PW \leq 10\text{ }\mu s$
I_{O-}	Output low short circuit pulsed current	250	350	—		$V_O = 15V$, $PW \leq 10\text{ }\mu s$

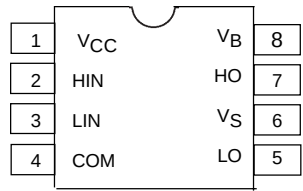
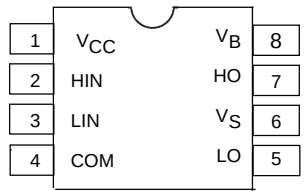
Functional Block Diagrams



Lead Definitions

Symbol	Description
HIN	Logic input for high side gate driver output (HO), in phase
LIN	Logic input for low side gate driver output (LO), in phase
VB	High side floating supply
HO	High side gate drive output
VS	High side floating supply return
VCC	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments

 8 Lead PDIP IR2301	 8 Lead SOIC IR2301S
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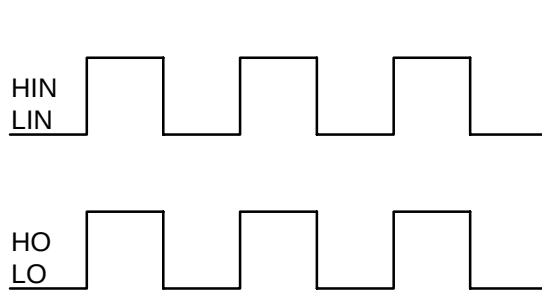


Figure 1. Input/Output Timing Diagram

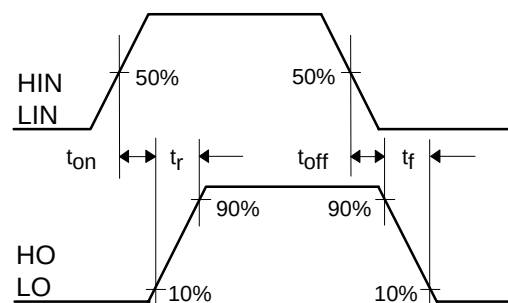


Figure 2. Switching Time Waveform Definitions

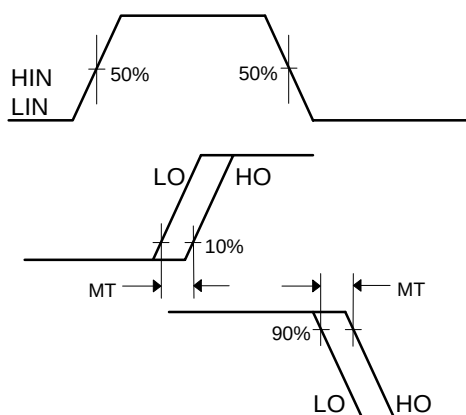


Figure 3. Delay Matching Waveform Definitions

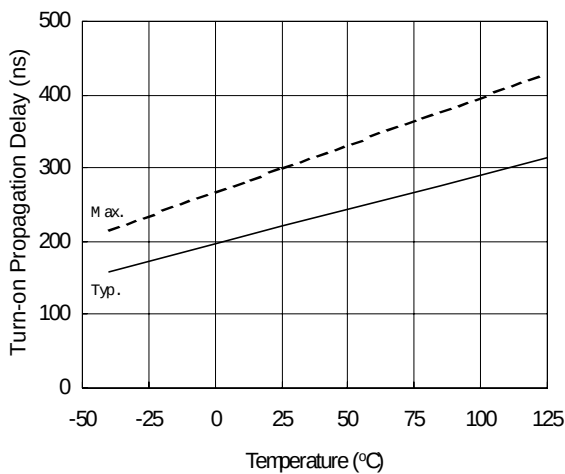


Figure 4A. Turn-on Propagation Delay vs. Temperature

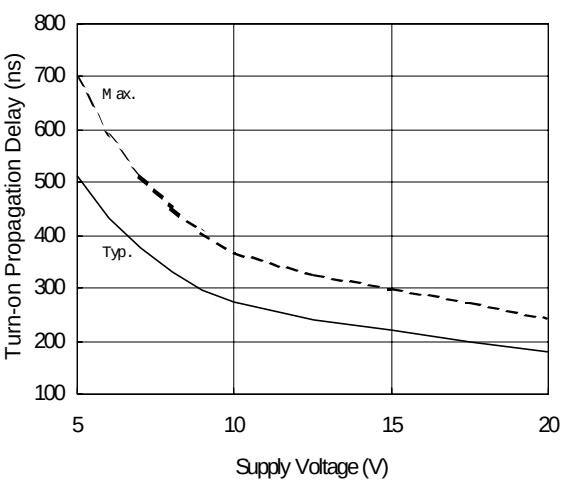


Figure 4B. Turn-on Propagation Delay vs. Supply Voltage

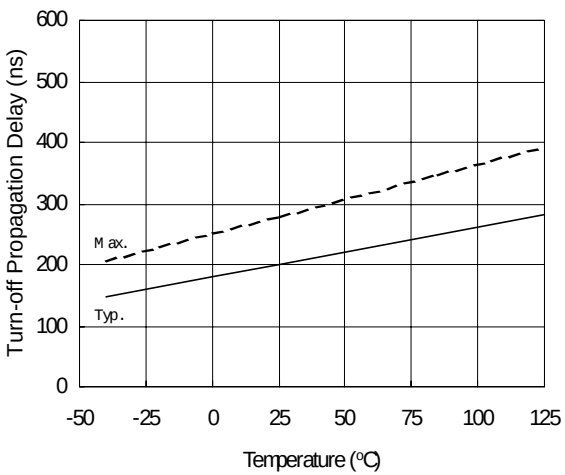


Figure 5A. Turn-off Propagation Delay vs. Temperature

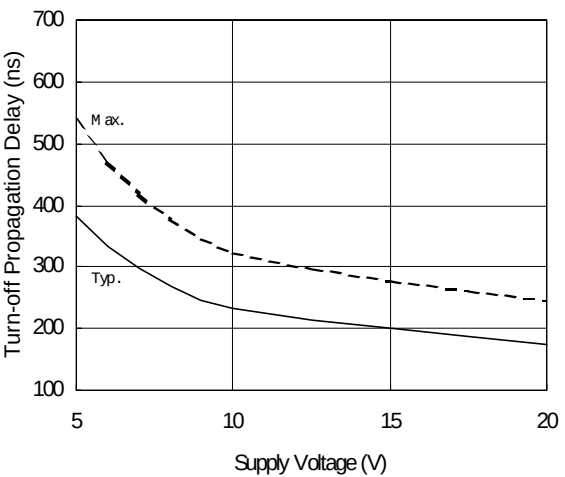


Figure 5B. Turn-off Propagation Delay vs. Supply Voltage

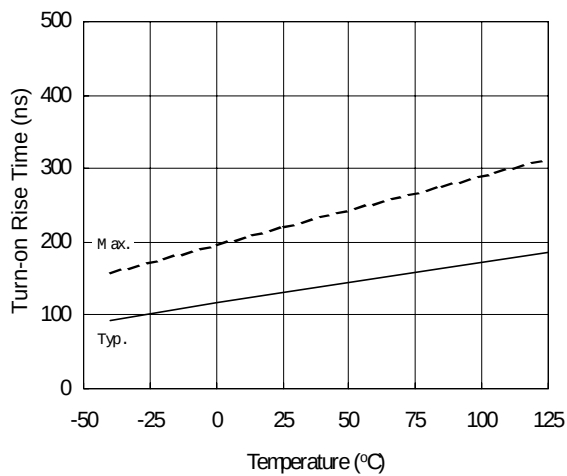


Figure 6A. Turn-on Rise Time vs. Temperature

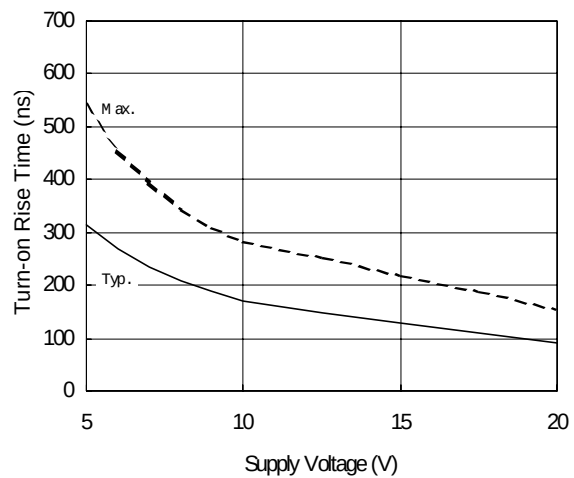


Figure 6B. Turn-on Rise Time vs. Supply Voltage

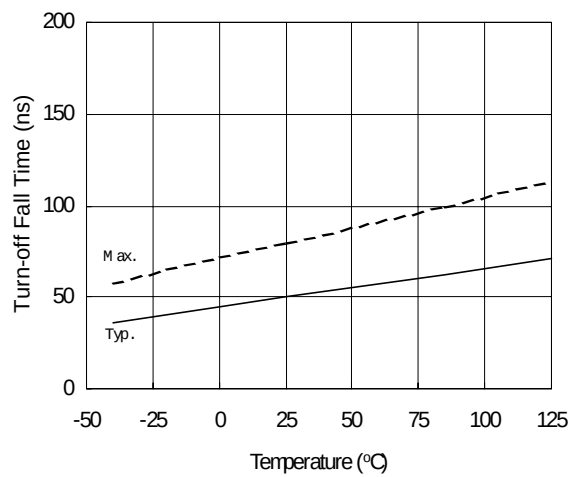


Figure 7A. Turn-off Fall Time vs. Temperature

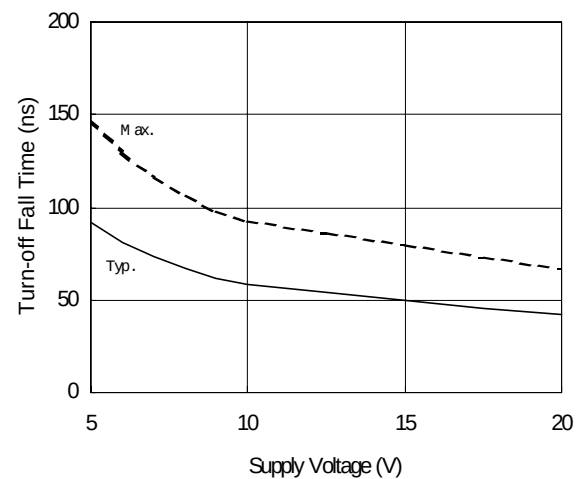


Figure 7B. Turn-off Fall Time vs. Supply Voltage

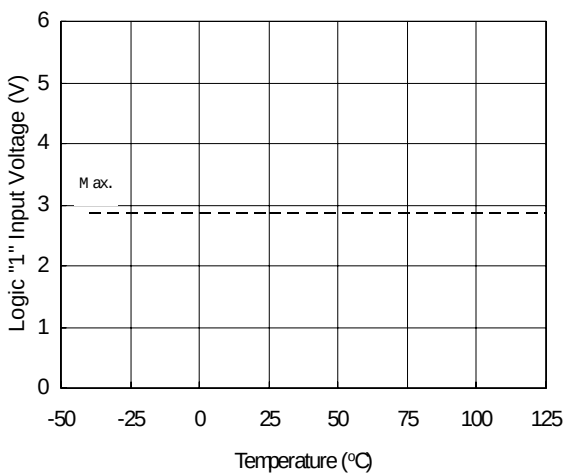


Figure 8A. Logic "1" Input Voltage vs. Temperature

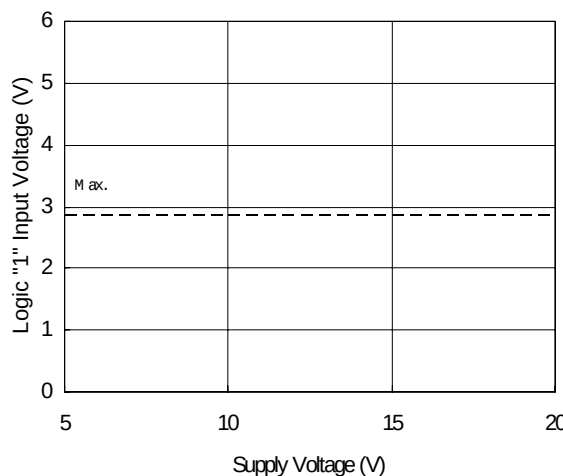


Figure 8B. Logic "1" Input Voltage vs. Supply Voltage

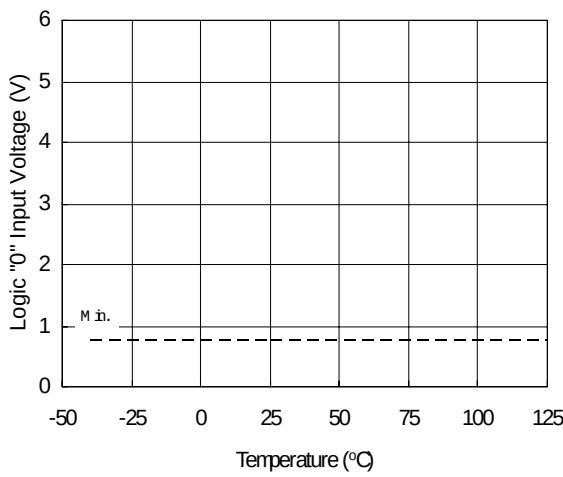


Figure 9A. Logic "0" Input Voltage vs. Temperature

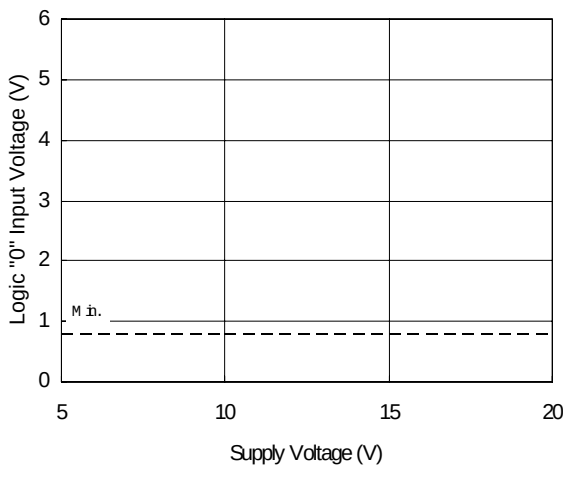


Figure 9B. Logic "0" Input Voltage vs. Supply Voltage

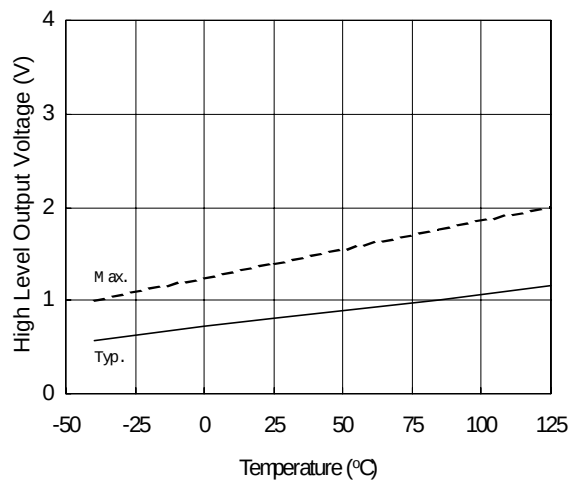


Figure 10A. High Level Output Voltage vs. Temperature

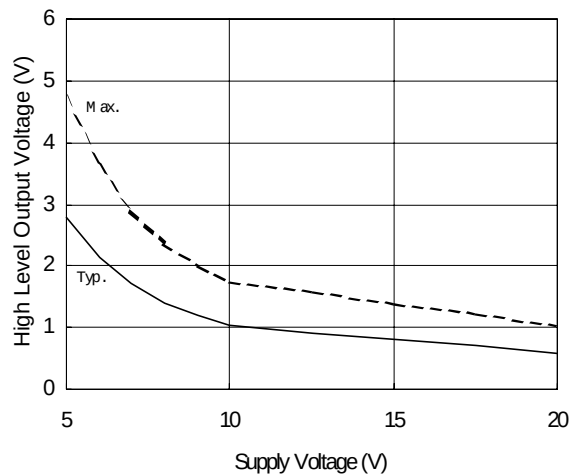


Figure 10B. High Level Output Voltage vs. Supply Voltage

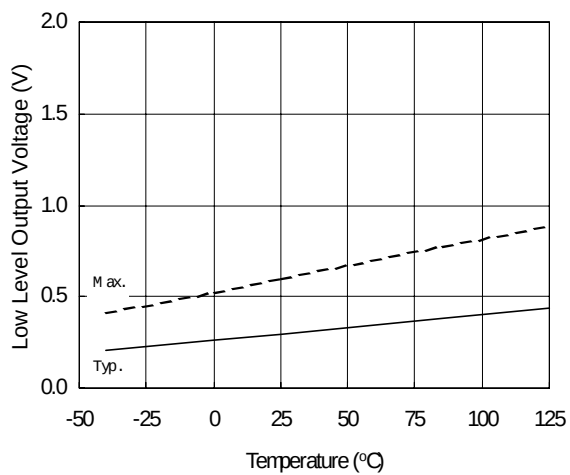


Figure 11A. Low Level Output Voltage vs. Temperature

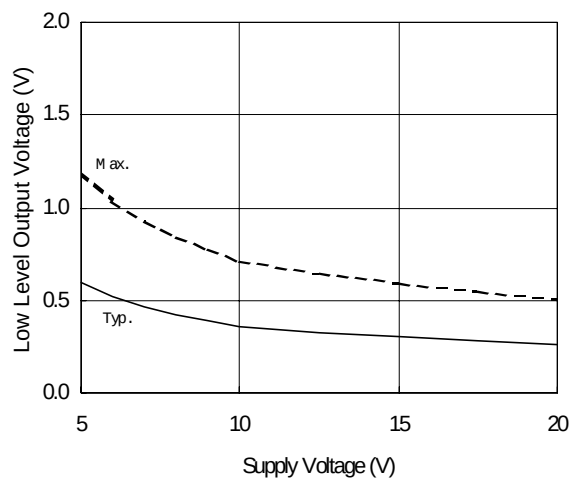


Figure 11B. Low Level Output Voltage vs. Supply Voltage

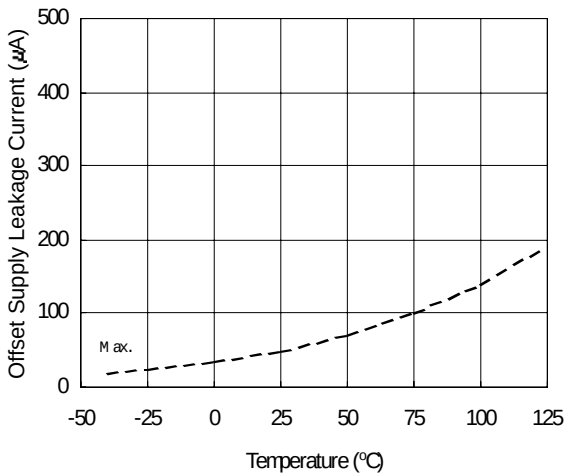


Figure 12A. Offset Supply Leakage Current vs. Temperature

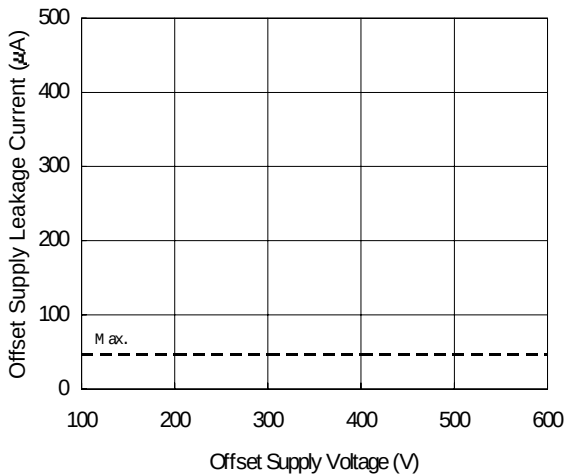


Figure 12B. Offset Supply Leakage Current vs. Supply Voltage

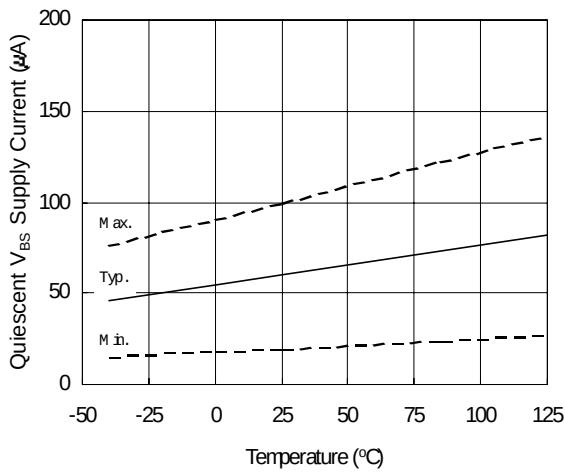


Figure 13A. Quiescent V_{BS} Supply Current vs. Temperature

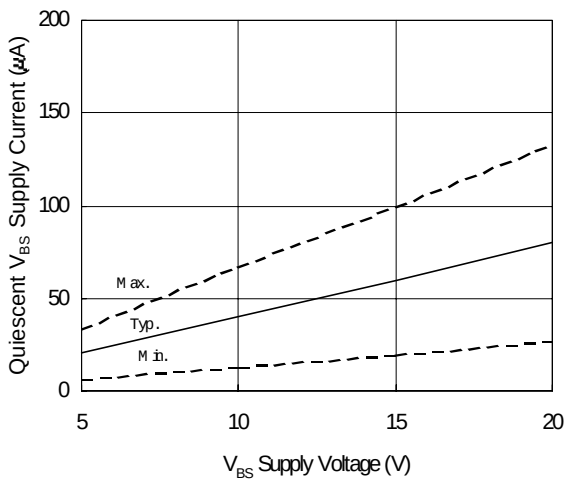


Figure 13B. Quiescent V_{BS} Supply Current vs. Supply Voltage

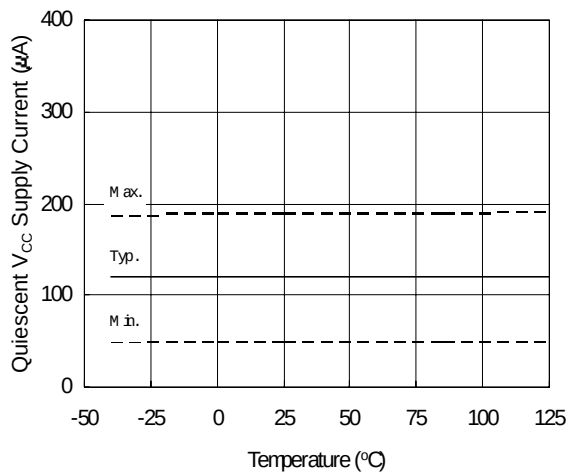


Figure 14A. Quiescent V_{CC} Supply Current vs. Temperature

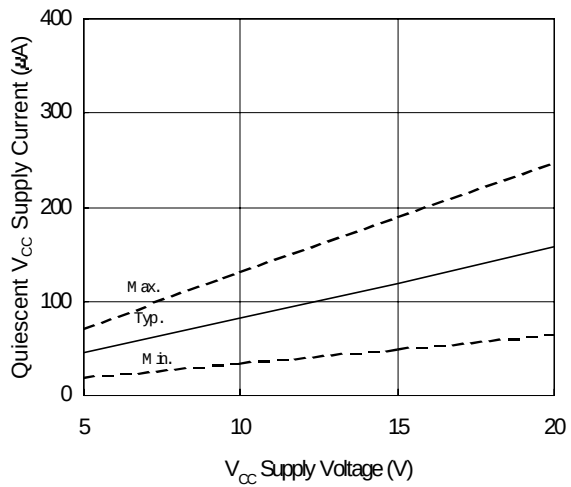


Figure 14B. Quiescent V_{CC} Supply Current vs. V_{CC} Supply Voltage

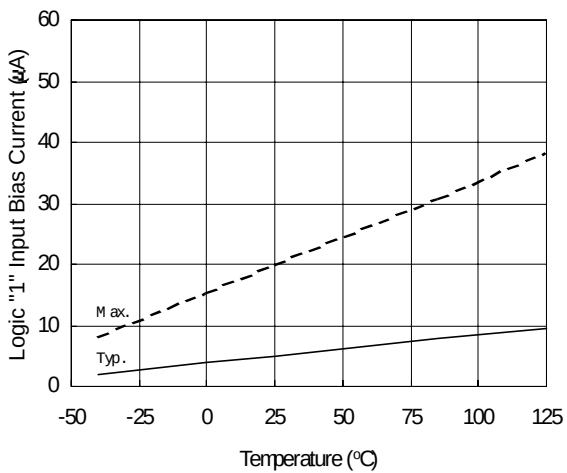


Figure 15A. Logic "1" Input Bias Current vs. Temperature

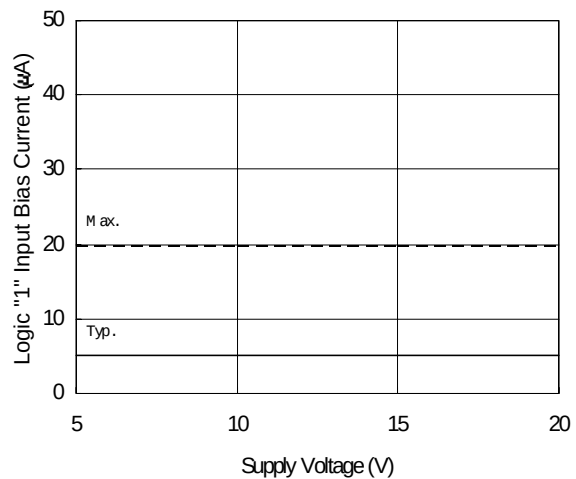


Figure 15B. Logic "1" Input Bias Current vs. Supply Voltage

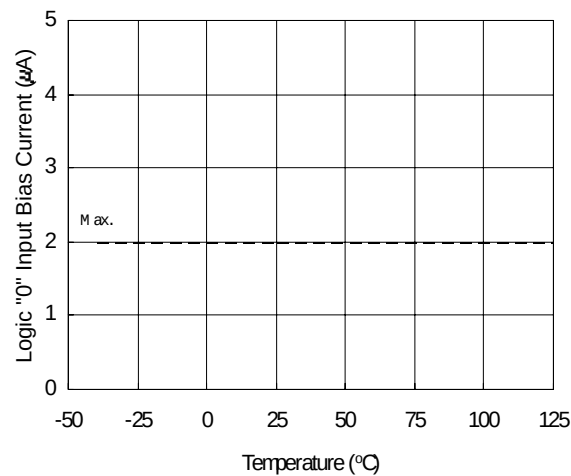


Figure 16A. Logic "0" Input Bias Current vs. Temperature

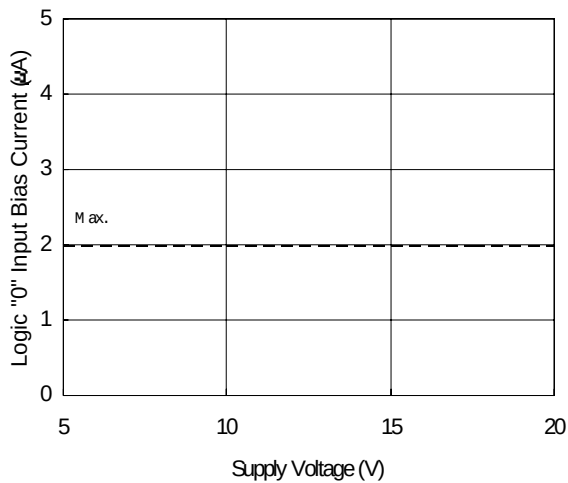


Figure 16B. Logic "0" Input Bias Current vs. Supply Voltage

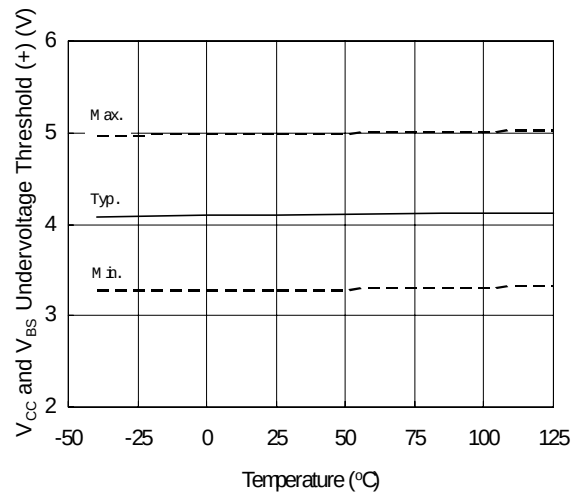


Figure 17. V_{CC} and V_{BS} Undervoltage Threshold (+) vs. Temperature

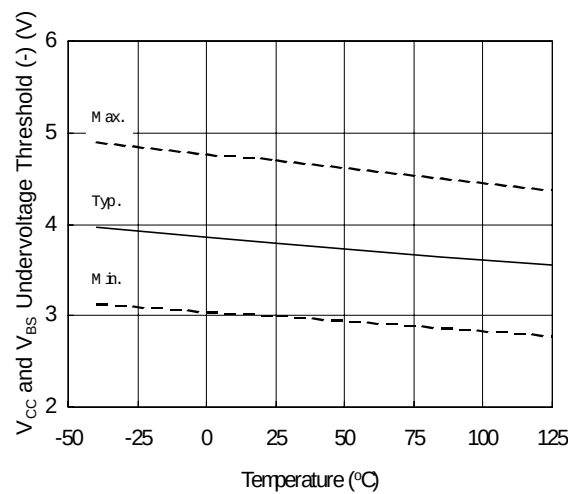


Figure 18. V_{CC} and V_{BS} Undervoltage Threshold (-) vs. Temperature

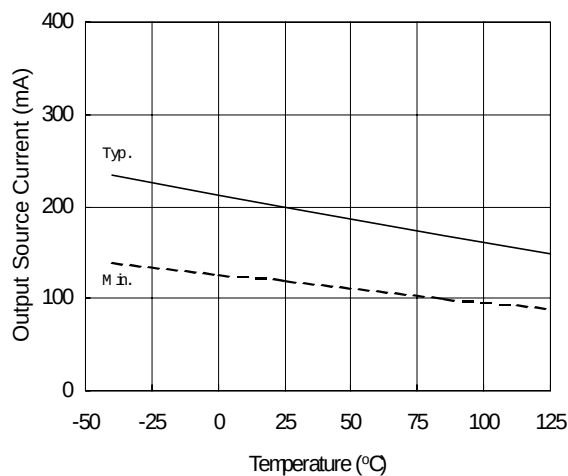


Figure 19A. Output Source Current vs. Temperature

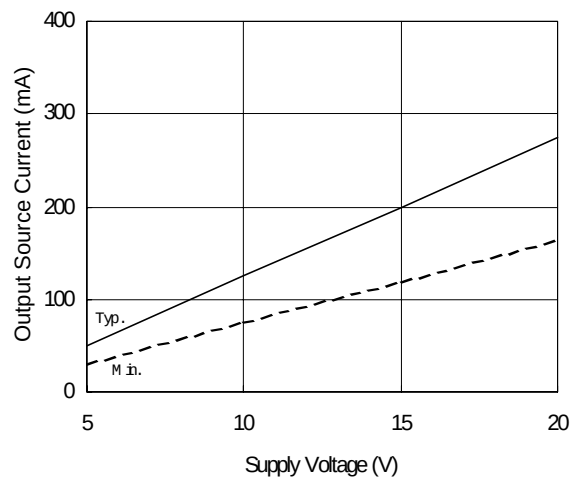


Figure 19B. Output Source Current vs. Supply Voltage

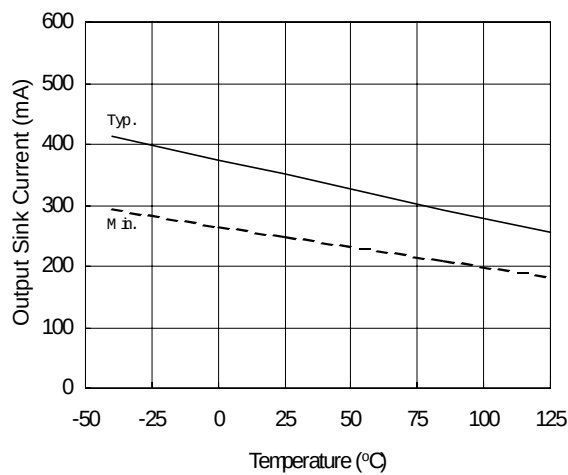


Figure 20A. Output Sink Current vs. Temperature

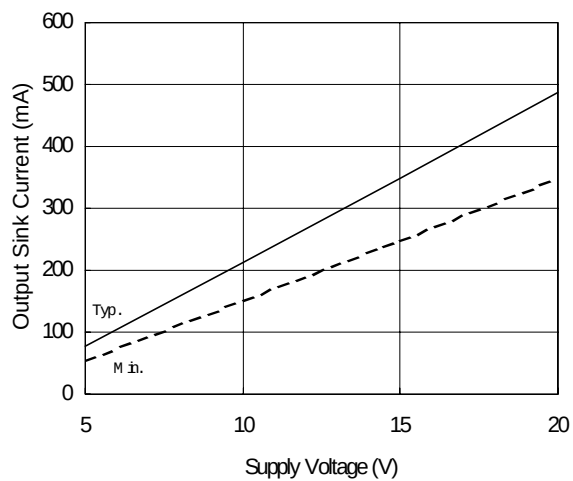


Figure 20B. Output Sink Current vs. Supply Voltage

IR2301 (S)

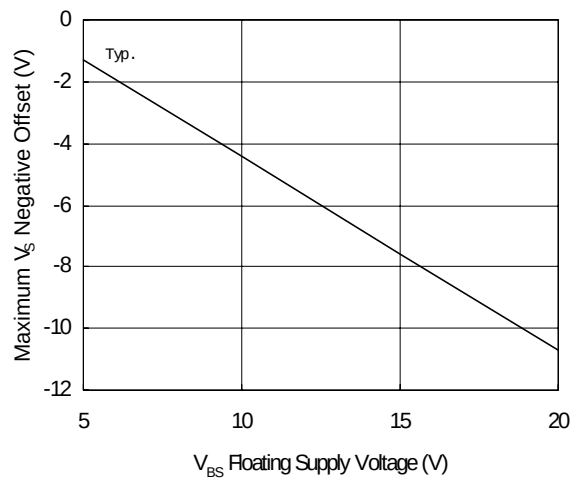


Figure 21. Maximum V_S Negative Offset vs. V_{BS} Floating Supply Voltage

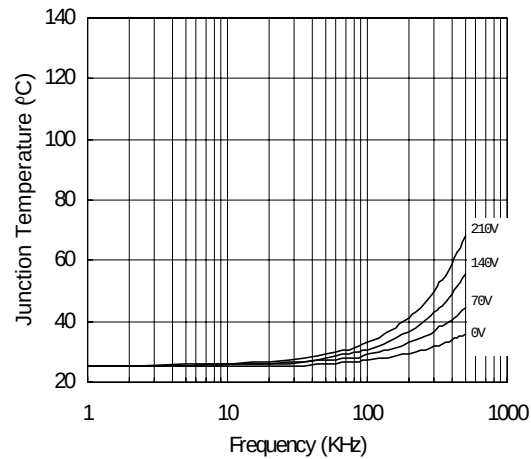


Figure 22. R2301 vs Frequency (IRFBC20)
R_{gate} = 33Ω, V_{CC} = 15V

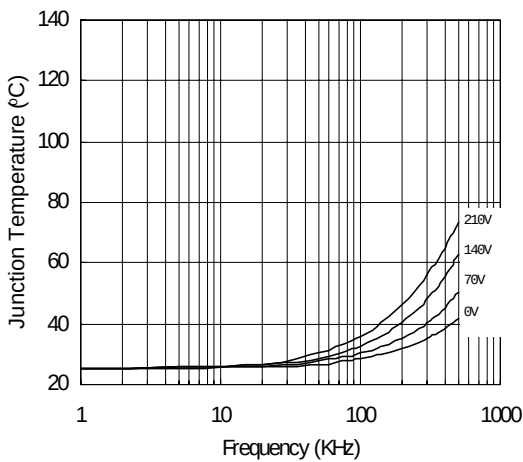


Figure 23. R2301 vs Frequency (IRFBC30)
R_{gate} = 22Ω, V_{CC} = 15V

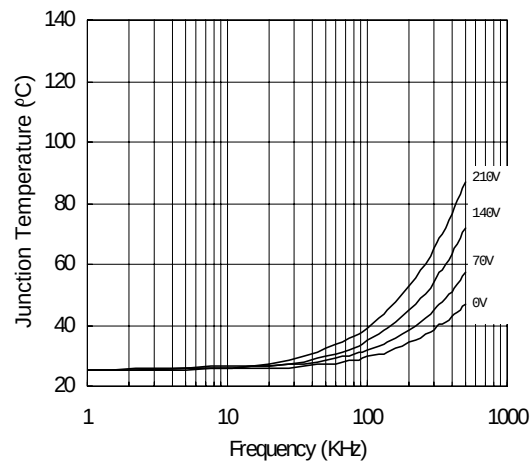


Figure 24. R2301 vs Frequency (IRFBC40)
R_{gate} = 15Ω, V_{CC} = 15V

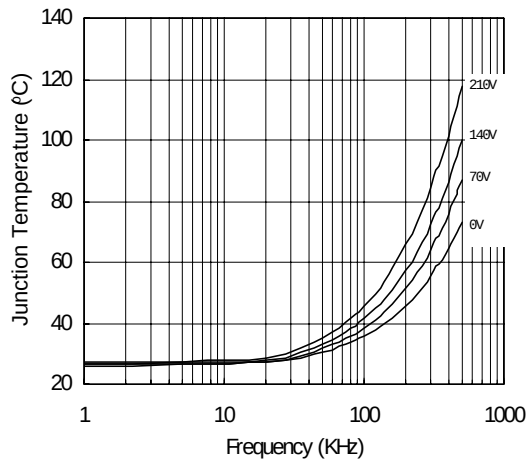


Figure 25. R2301 vs Frequency (IRFPE50)
 $R_{gate} = 10\Omega$, $V_{CC} = 15V$

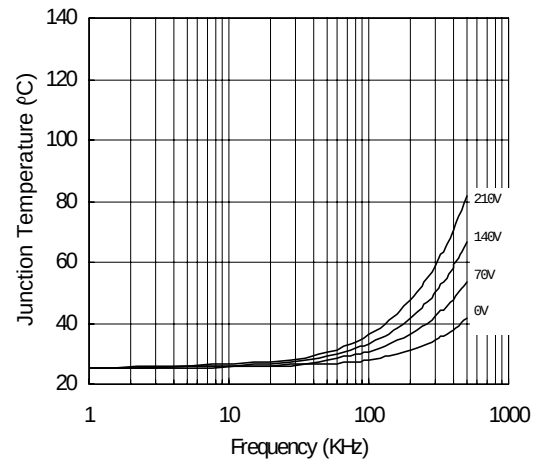


Figure 26. IR2301S vs Frequency (IRFBC20)
 $R_{gate} = 33\Omega$, $V_{CC} = 15V$

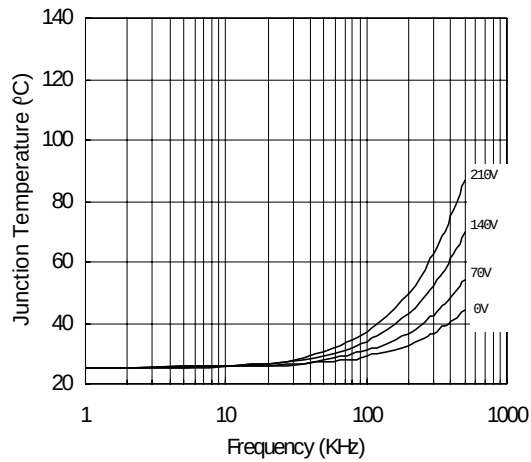


Figure 27. IR2301S vs Frequency (IRFBC30)
 $R_{gate} = 22\Omega$, $V_{CC} = 15V$

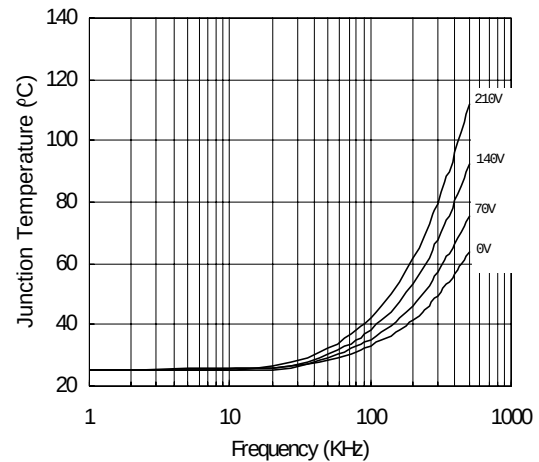


Figure 28. IR2301 vs Frequency (IRFBC40)
 $R_{gate} = 15\Omega$, $V_{CC} = 15V$

IR2301 (S)

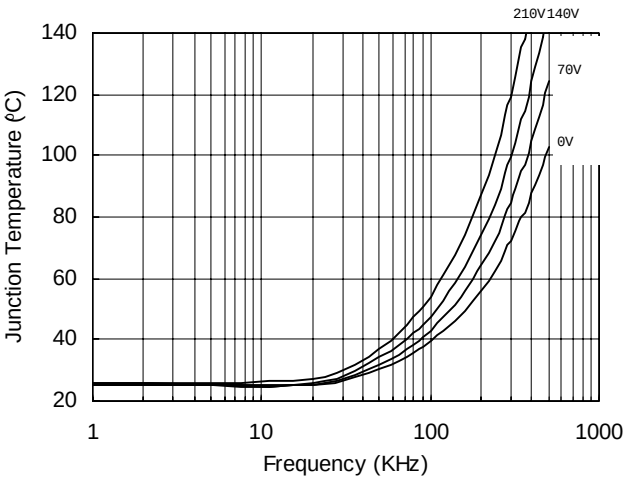


Figure 29. IR2301S vs Frequency (IRFPE50)
 $R_{gate} = 10\Omega$, $V_{CC} = 15V$

Case Outlines

