

## Product Features

- High-Performance, Phase-Locked-Loop Clock Distribution
- Allows Clock Input to have Spread Spectrum modulation for EMI reduction
- Zero Input-to-Output delay
- Low jitter: Cycle-to-Cycle jitter  $\pm 75$ ps max.
- On-chip series damping resistor at clock output drivers for low noise and EMI reduction
- Operates at 3.3V V<sub>CC</sub>
- Wide range of Clock Frequencies 80 to 134 MHz
- Package: Plastic 8-pin SOIC (W)

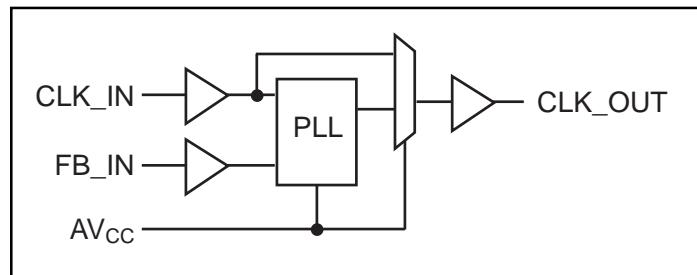
## Product Description

The PI6C2501A features a low-skew, low-jitter, phase-locked loop (PLL) clock driver. By connecting the CLK\_OUT output to the feedback FB\_IN input, the propagation delay from the CLK\_IN input to CLK\_OUT output will be nearly zero.

## Application

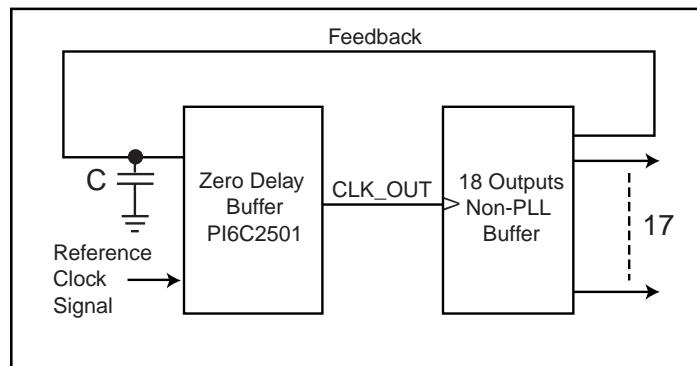
If a system designer needs more than 16 outputs with the features just described, using two or more zero-delay buffers, such as the PI6C2509Q, or PI6C2510Q, is likely to be impractical. The device-to-device skew introduced can significantly reduce the performance. Pericom recommends using a zero-delay buffer and an eighteen output non-zero-delay buffer. As shown in Figure 1, this combination produces a zero-delay buffer with all the signal characteristics of the original zero-delay buffer, but with as many outputs as the non-zero-delay buffer part. For example, when combined with an eighteen output non-zero delay buffer, a system designer can create a seventeen-output zero-delay buffer.

## Logic Block Diagram



## Product Pin Configuration

AGND	1	8	CLK_IN
GND	2	7	AVCC
CLK_OUT	3	6	GND
VCC	4	5	FB_IN



**Figure 1. This Combination Provides Zero-Delay Between the Reference Clock Signal and 17 Outputs**

## Pin Functions

Pin Name	Pin No.	Type	Description
CLK_IN	8	I	Reference Clock input. CLK_IN allows spread spectrum clock input.
FB_IN	5	I	Feedback input. FB_IN provides the feedback signal to the internal PLL.
CLK_OUT	3	O	Clock output. This output provides a low-skew copy of CLK_IN. The output has an embedded series-damping resistor.
AVCC	7	Power	Analog power supply. AVCC can be also used to bypass the PLL for test purpose. When AVCC is strapped to ground, PLL is bypassed and CLK_IN is buffered directly to the device outputs.
AGND	1	Ground	Analog ground. AGND provides the ground reference for the analog circuitry.
VCC	4	Power	Power supply.
GND	2, 6	Ground	Ground.

## DC Specifications (Absolute maximum ratings over operating free-air temperature range)

Symbol	Parameter	Min.	Max.	Units
V <sub>I</sub>	Input voltage range	-0.5	V <sub>CC</sub> + 0.5	V
V <sub>O</sub>	Output voltage range			
V <sub>I_DC</sub>	DC input voltage		3.8	
I <sub>O_DC</sub>	DC output current		100	mA
Power	Maximum power dissipation at T <sub>A</sub> = 55°C in still air		1.0	W
T <sub>STG</sub>	Storage temperature	-65	150	°C

### Note:

Stress beyond those listed under "absolute maximum ratings" may cause permanent damage to the device.

Parameter	Test Conditions	V <sub>CC</sub>	Min.	Typ.	Max.	Units
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 <sup>(1)</sup> Standby Current	3.6V			10	μA
C <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND			4		pF
C <sub>O</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3V		6		

### Note:

1. Continuous Output Current

## Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V <sub>CC</sub>	Supply voltage	3.0	3.6	V
V <sub>IH</sub>	High level input voltage	2.0		
V <sub>IL</sub>	Low level input voltage		0.8	
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	
T <sub>A</sub>	Operating free-air temperature	0	70	°C

**Electrical Characteristics** (Over Recommended Operating Free-Air Temperature Range)

 Pull Up/Down Currents of PI6C2501A,  $V_{CC} = 3.0V$ 

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH}$	Pull-up current	$V_{out} = 2.4V$		-13.6	mA
	Pull-up current	$V_{out} = 2.0V$		-22	
$I_{OL}$	Pull-down current	$V_{out} = 0.8V$	19		
	Pull-down current	$V_{out} = 0.55V$	13		

**AC Specifications**

(Timing requirements over recommended ranges of supply voltage and operating free-air temperature)

Symbol	Parameter	Min.	Max.	Units
$F_{CLK}$	Clock frequency PI6C2501A	80	134	MHz
$D_{CYI}$	Input clock duty cycle	40	60	%
	Stabilization Time after power up		1	ms

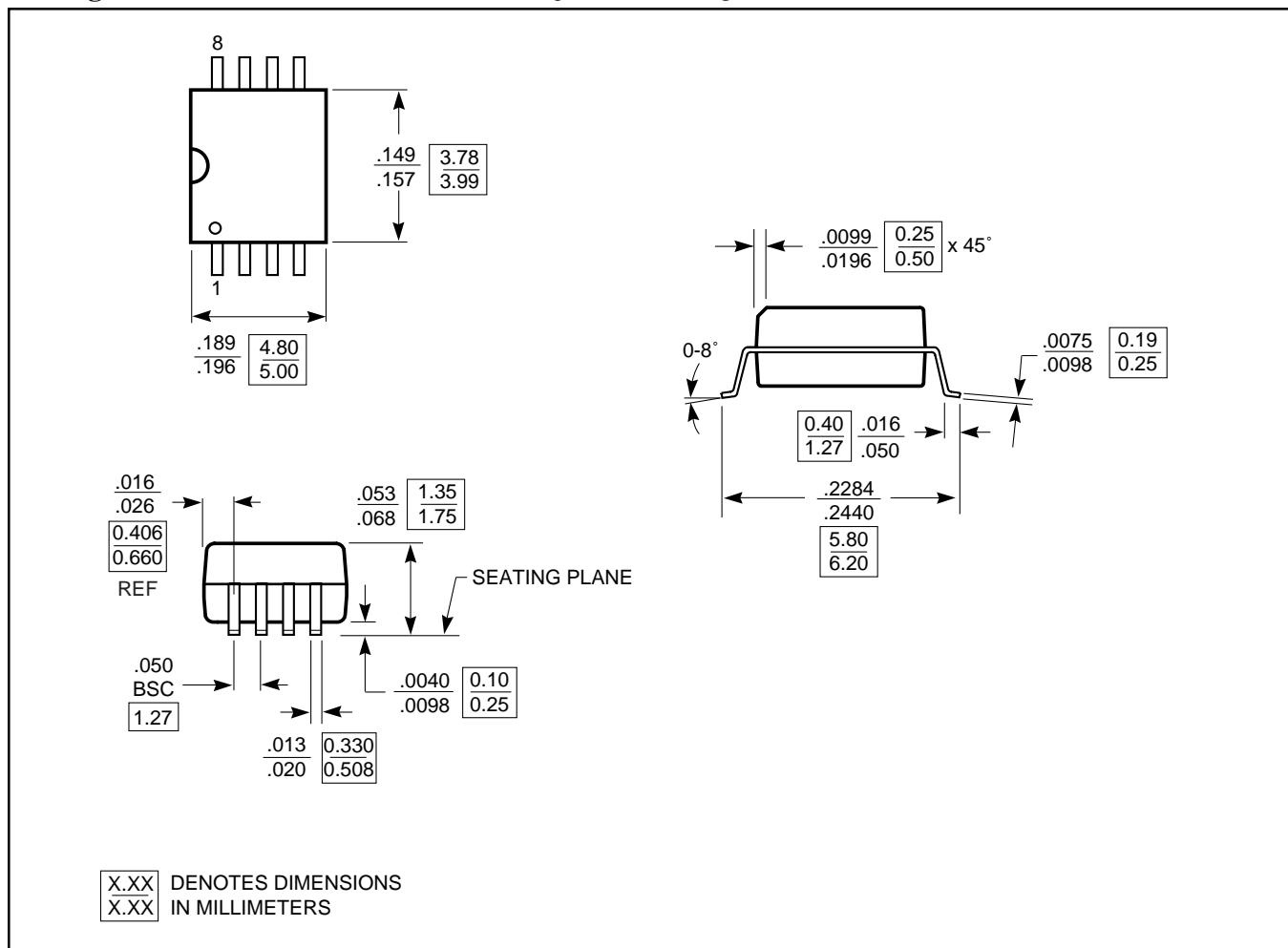
**Switching Characteristics**

 (Over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 30pF$ )

Parameter	From (Input)	To (Output)	$V_{CC} = 3.3V \pm 0.3V, 0-70^{\circ}C$			Units
			Min.	Typ.	Max.	
tphase error without jitter	$CLK\_IN \uparrow$ at 100 & 66 MHz	$FB\_IN \uparrow$	-150		+150	ps
Jitter, cycle-to-cycle	At 100 & 66 MHz		-75		+75	
Duty cycle		$CLK\_OUT$	45		55	%
$t_r$ , rise-time, 0.4V to 2.0V				1.0		
$t_f$ , fall-time, 2.0V to 0.4V				1.1		ns

**Note:**

These switching parameters are guaranteed by design.

**Package Mechanical Information:** Plastic 8-pin SOIC Package.

**Ordering Information**

Ordering Code	Package Name	Package Type	Operating Range
PI6C2501AW	W8	8-pin 150-mil SOIC	Commercial