RNA50C27AUS

CMOS System-Reset IC

REJ03D0834-0100
Preliminary
Rev.1.00
Apr 10, 2006

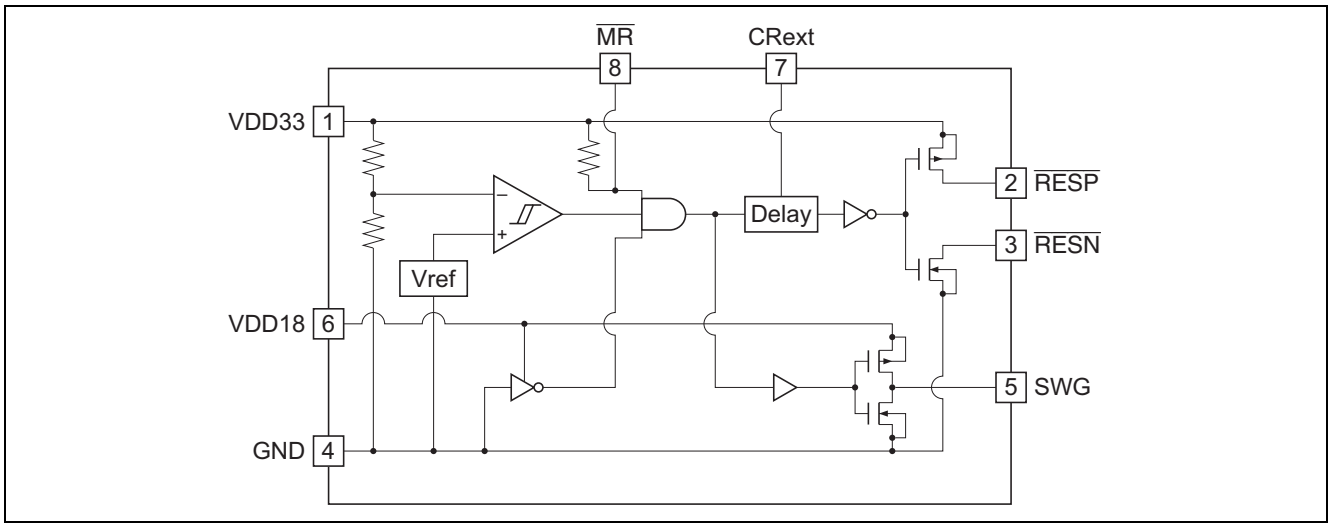
Description

This IC facilitates complicated power-on and power-monitoring resets of microcomputers that require the 3.3-V and 1.8-V dual power supplies. It also facilitates change of delay time of reset signal by externally setting resistance and capacity for delay time. By employing complementary open-drain output, desired output such as open-drain output and CMOS output can be obtained.

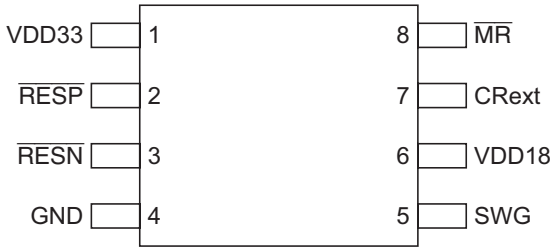
Functions

- 3.3-V detection voltage : 2.7 V
- Accuracy of 3.3-V detection voltage : ±1.0%
- Hysteresis of 3.3-V detection voltage : 5% Typ.
- Open-drain/CMOS output
- 1.8-V PMOS drive output
- Ultra-small SSOP-8 package

Block Diagram



Pin Arrangement



(Top view)

Pin Description

Pin No.	Pin Name	Function
1	VDD33	Input power supply pin for 3.3-V voltage. Recommended operating range is 2.7 to 3.6 V. Set the input voltage to 0.033 V/μs or less when starting up.
2	$\overline{\text{RESP}}$	Active-low reset signal output pin. By connecting to RESN pin, CMOS output can be used. If using open-drain, please connect pull-down resistor.
3	$\overline{\text{RESN}}$	Active-low reset signal output pin. By connecting to RESP pin, CMOS output can be used. If using open-drain, please connect pull-up resistor.
4	GND	GND pin
5	SWG	External PMOS gate control signal to be set between 1.8-V power supply and 1.8-V voltage input of microcomputer.
6	VDD18	Input power supply pin for 1.8-V voltage. Recommended operating range is 1.65 to 3.6 V.
7	CRext	Connecting pin for Rext resistance and Cext capacity that determine the delay time of reset signal. 3.3 kΩ or more is recommended for resistance. The delay time, t_{DLY}, is given by the following formula. $t_{DLY} = Cext \times Rext$ [s]
8	$\overline{\text{MR}}$	Pin to provide reset manually. MR pin is pulled-up to VDD33 through internal resistor.

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	VDD33	4.6	V
	VDD18	4.6	
Input voltage	V_I	–0.3 to VDD33+0.3	V
Output voltage	V_O	–0.3 to VDD33+0.3	V
Input current	I_I	20	mA
Output current	I_O	25	mA
Supply current	I_{DD}	25	mA
Power dissipation	P_T	273	mW
Storage temperature	Tstg	–55 to +125	°C

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit	Remarks
Supply voltage	VDD33	VTH33	—	3.6	V	
	VDD18	1.65	—	VDD33		
Input voltage	V_{MR}	0	—	VDD33	V	
Output voltage	V_O	0	—	VDD33	V	
	V_{OSWG}	0	—	VDD18		
External resistor	Rext	3.3	—	—	kΩ	VDD33 = 3.3 V
External capacitor	Cext	—	No limit	—		
Drivable capacitor	C_L	—	2200	—	pF	SWG output
Operating temperature	Ta	–40	—	85	°C	

Electrical Characteristics

DC Characteristics

(VDD33 = 3.3 V, VDD18 = 1.8 V, Ta = 25°C, CRext:R = 10 kΩ)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Quiescent supply current		IDD33	0.75	1.5	4	µA	All outputs are open
		IDD18	0.25	0.5	2		
Detection voltage		VTH33	Typ×0.99	2.7	Typ×1.01	V	
		VTH_H	1.2	—	—		
		VTH_L	—	—	0.55		
Detection voltage temperature dependency		$\frac{\Delta Vth33}{Vth \cdot \Delta Ta}$	—	±100	—	ppm/°C	
Detection voltage hysteresis		V_{HYS}	VTH33×3%	VTH33×5%	VTH33×8%	V	
MR	Low-level input voltage	V_{IL}	—	—	VTH33×0.25	V	
	High-level input voltage	V_{IH}	VTH33×0.75	—	—	V	
	internal pull-up resistance	R_{MR}	—	T.B.D.	—	kΩ	
CMOS *1	Low-level output current	I_{OL}	7.5	15	30	mA	V_O = 0.5 V
	High-level output current	I_{OH}	5	10	20		V_O = VDD33 – 0.5 V
RESP	Output leakage current	I_{LEAK}	—	—	0.1	µA	RESN off
RESN	Output leakage current	I_{LEAK}	—	—	0.1	µA	RESP off
SWG	High-level output voltage	V_{OH}	1.7	—	—	V	V_O = open
	Output source current	I_{OH}	1.5	3	6	mA	V_O = VDD33 – 0.5 V
	Low-level output voltage	V_{OL}	—	—	0.1	V	V_O = open
	Output sink current	I_{OL}	0.2	0.35	0.55	mA	V_O = 0.5 V

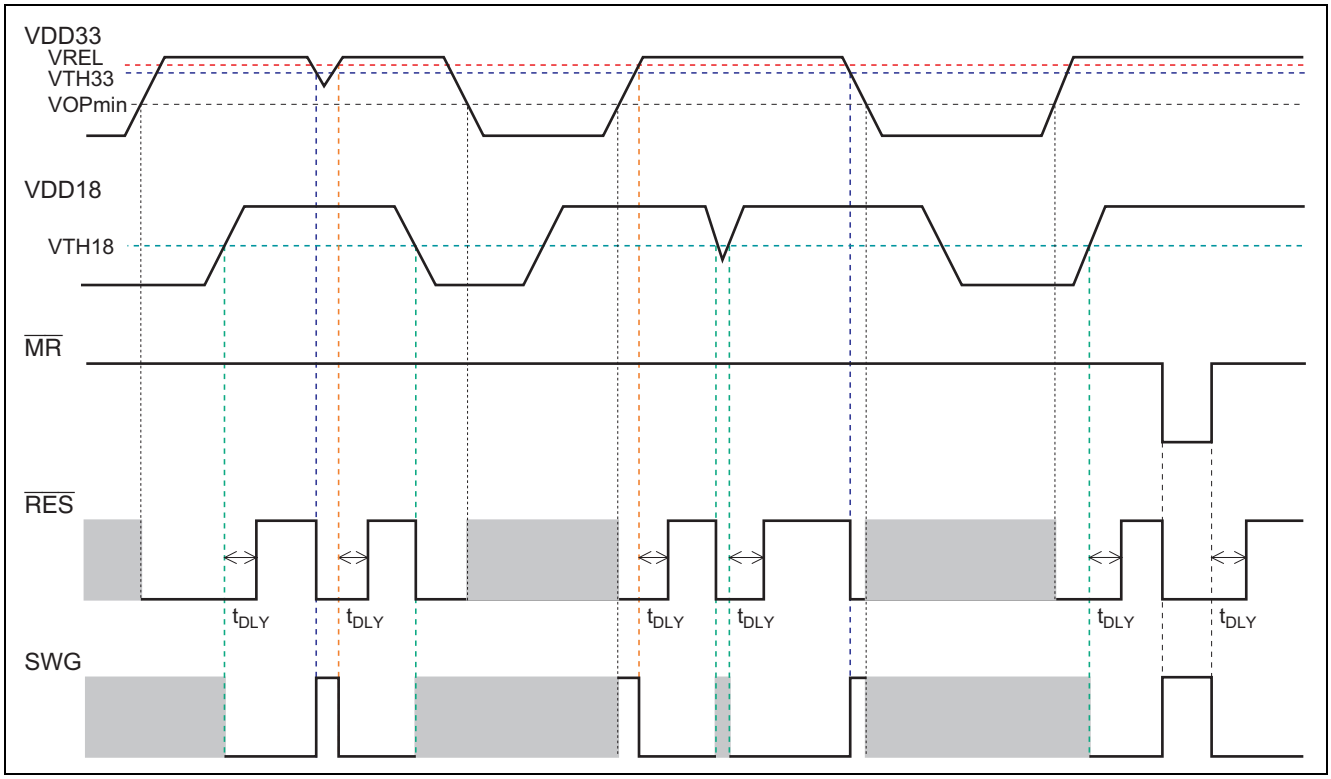
Note: When the voltage within $V_{IL} < V_{IN} < V_{IH}$ is applied to MR and VDD18 input by DC, oscillation may occur.

1. When RESP output and RESN short out and CMOS output is used.

AC Characteristics

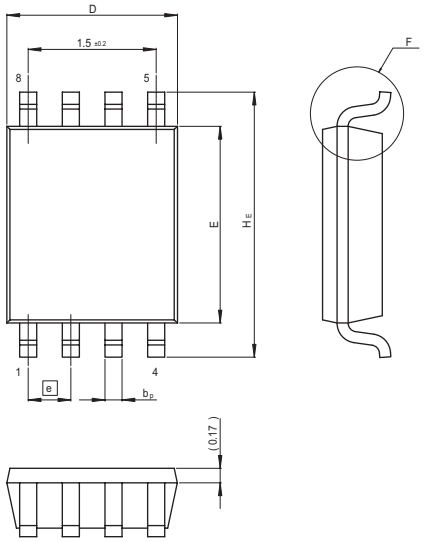
Item		Symbol	Min	Typ	Max	Unit	Test Conditions
RESP	Propagation delay time	tp_{LH}	—	50	400	µs	C_L = 15 pF, CRext:C = open
		tp_{HL}	—	5	T.B.D.		
	Response time	t_r	—	5	T.B.D.	ns	C_L = 15 pF
		t_f	—	5	T.B.D.	µs	
RESN	Propagation delay time	tp_{LH}	—	50	400	µs	C_L = 15 pF, CRext:C = open
		tp_{HL}	—	1.5	T.B.D.		
	Response time	t_r	—	5	T.B.D.	µs	C_L = 15 pF
		t_f	—	5	T.B.D.	ns	
SWG	Propagation delay time	tp_{LH}	—	50	400	µs	C_L = 2200 pF
		tp_{HL}	T.B.D.	1.5	T.B.D.		
	Response time	t_r	T.B.D.	1.0	T.B.D.	µs	
		t_f	T.B.D.	7.6	T.B.D.		
Delay time		t_{DLY}	—	93	—	ms	CRext:C = 0.1 µF, R = 1 MΩ

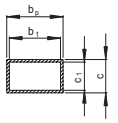
Timing Chart



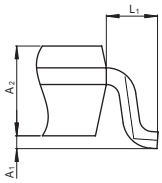
Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-VSSOP8-2.3x2-0.50	PVSP0008KA-A	TTP-8DB/TTP-8DBV	0.010g





Terminal cross section

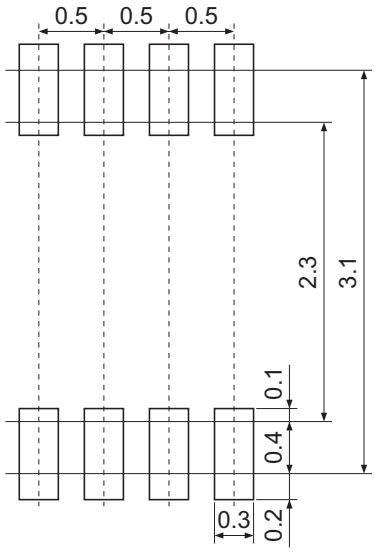


Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	1.8	2.0	2.2
E	2.2	2.3	2.4
A_2	0.6	0.7	0.8
A_1	0	—	0.1
A	—	—	—
b_p	0.15	0.22	0.3
b_1	—	0.20	—
c	0.08	0.13	0.23
c_1	—	0.11	—
θ	—	—	—
H_E	2.8	3.1	3.4
e	—	(0.5)	—
x	—	—	—
y	—	—	—
Z	—	—	—
L	—	—	—
L_1	—	(0.4)	—

Footprint

Unit: mm



SSOP-8 Footprint Example

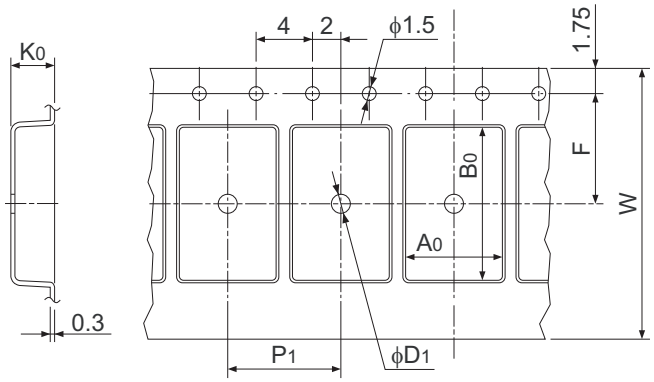
Note: These numbers on the diagram are reference values.
Please adjust size, space, and other area of footprint as needed.

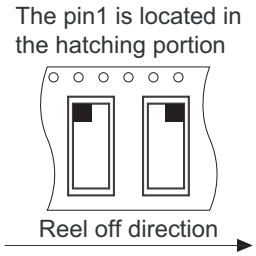
Taping and Reel Specifications

[Taping]

Unit: mm

W	P_1	A_0	B_0	K_0	F	D_1	Maximum Storage No.	Reel Type	Packing Form
8	4	2.25	3.4	1.0	3.5	1.05	3,000 IC/Reel	C	Non dry pack

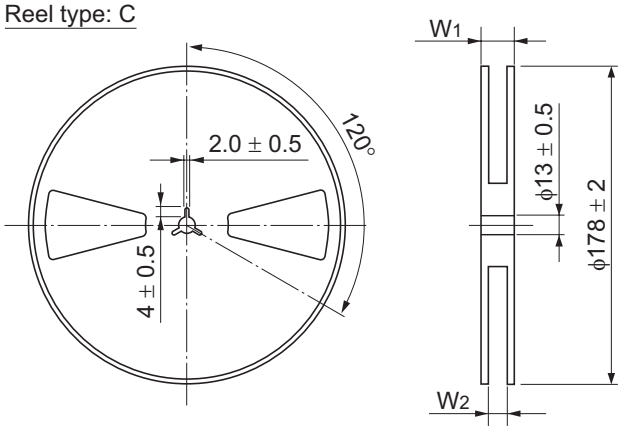




[Reel]

Tape width: W	W_1	W_2
8	13.0	9.0

Reel type: C



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