Power MOSFET

25 V, 85 A, Single N-Channel, DPAK

Features

- Low R_{DS(on)} to Minimize Conduction Losses
- Optimized Gate Charge to Minimize Switching Losses
- Pb-Free Packages are Available

Applications

- VCORE Applications
- DC-DC Converters
- Optimized for Low Side Switching

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

TIPATITO (1) = 23 0 unicas outerwise noted)					
Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	25	٧
Gate-to-Source Voltag	е		V _{GS}	±20	>
Continuous Drain		$T_A = 25^{\circ}C$	I _D	14.7	A
Current (R _{θJA}) (Note 1)		T _A = 85°C		11.4	
Power Dissipation (R _{θJA}) (Note 1)		T _A = 25°C	P _D	2.3	W
Continuous Drain		$T_A = 25^{\circ}C$	P	11.3	Α
Current (R _{θJA}) (Note 2)	Steady	T _A = 85°C		8.8	(5)
Power Dissipation (R _{0.IA}) (Note 2)	State	T _A = 25°C	P _D	1.4	W
Continuous Drain		T _C = 25°C	I _D	85	А
Current (R _{θJC})	X	T _C = 85°C		66	
Power Dissipation (R ₀ JC)		T _C = 25°C	PD	76.9	W
Pulsed Drain Current t _p = 10 μs			I _{DM}	98	Α
Current Limited by Pack	age	T _A = 25°C	I _{DmaxPkg}	32	Α
Operating Junction and	T _J , T _{stg}	-55 to 175	°C		
Source Current (Body Diode)			Is	77	Α
Drain to Source dV/dt	dV/dt	8.0	V/ns		
Single Pulse Drain-to-S Energy (V _{DD} = 24 V, V _G L = 5.0 mH, I _L (pk) = 5.5	E _{AS}	75	mJ		
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T _L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

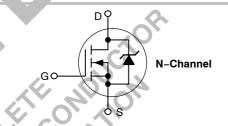
- 1. Surface-mounted on FR4 board using 1 in sq pad size, 1 oz Cu.
- 2. Surface-mounted on FR4 board using the minimum recommended pad size.



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V _{(BR)DSS}	R _{DS(on)} TYP	I _D MAX
25 V	5.0 @ 11.5 V	85 A
25 V	7.5 @ 4.5 V	05 A







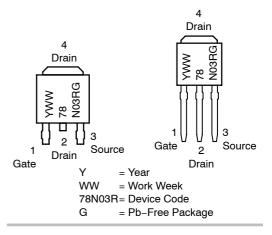


CASE 369C DPAK (Bend Lead) STYLE 2

CASE 369D DPAK (Straight Lead) STYLE 2

CASE 369AC 3 IPAK (Straight Lead)

MARKING DIAGRAMS & PIN ASSIGNMENTS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{ heta JC}$	1.95	°C/W
Junction-to-Ambient - Steady State (Note 3)	$R_{ heta JA}$	65	
Junction-to-Ambient - Steady State (Note 4)	$R_{\theta JA}$	110	

Parameter	Symbol	Test Cor	ndition	Min	Тур	Max	Unit
OFF CHARACTERISTICS		<u>I</u>					
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _[_O = 250 μA	25			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J			_	10		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 20 V	$T_{J} = 25^{\circ}C$ $T_{J} = 125^{\circ}C$			1.5 10	μΑ
Gate-to-Source Leakage Current	I _{GSS}	$V_{DS} = 0 V, V_{C}$	_			± 100	nA
ON CHARACTERISTICS (Note 5)				<u> </u>	1	0,	
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}$, I	_D = 250 μA	1.0	1.7	3.0	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J			4.	-5.3		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} =	I _D = 30 A	1	5.0	5.8	mΩ
		10V to 11.5 V	I _D = 15 A	(0)	4.9	5.7	
		V _{GS} = 4.5 V	I _D = 30 A		7.5	9.0	
			l _D = 15 A		7.2	8.5	
Forward Transconductance	gFS	$V_{DS} = 15 V_{r}$	I _D = 10 A		23		S
CHARGES, CAPACITANCES AND GATE RE	SISTANCE	, 10	0, 12	7,			
Input Capacitance	C _{iss}	CV Q	1		1794		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 12 V			882		
Reverse Transfer Capacitance	C _{rss}				373		
Total Gate Charge	Q _{G(TOT)}	7			19.4	24	nC
Threshold Gate Charge	Q _{G(TH)}	V _{GS} = 4.5 V,	V _{DS} = 20 V,		0.8		
Gate-to-Source Charge	Q_GS	I _D = 2	.0 A		2.9		
Gate-to-Drain Charge	Q_{GD}				12.4		
SWITCHING CHARACTERISTICS (Note 6)	0 03)					
Turn-On Delay Time	t _{d(on)}				11		ns
Rise Time	t _r	V _{GS} = 4.5 V,	V _{DS} = 20 V,		75		
Turn-Off Delay Time	t _{d(off)}	$I_D = 20 \text{ A}, R_G = 2.5 \Omega$			18		
Fall Time	t _f				17		
PRAIN-SOURCE DIODE CHARACTERISTIC	cs						
Forward Diode Voltage	V _{SD}	$V_{GS} = 0 \text{ V},$ $I_{S} = 30 \text{ A}$	T _J = 25°C		8.0	1.0	V
Reverse Recovery Time	t _{RR}				38		ns
Charge Time	ta	$V_{GS} = 0 \text{ V, } dls/d_t = 100 \text{ A/}\mu s,$ $l_S = 20 \text{ A}$			16.5		1
Discharge Time	tb				22		1
Reverse Recovery Time	Q _{RR}				31		nC

- Surface–mounted on FR4 board using 1 in sq pad size, 1 oz Cu.
 Surface–mounted on FR4 board using the minimum recommended pad size.
 Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
 Switching characteristics are independent of operating junction temperatures.

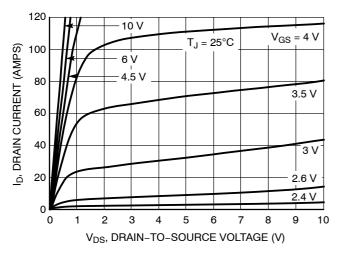


Figure 1. On-Region Characteristics

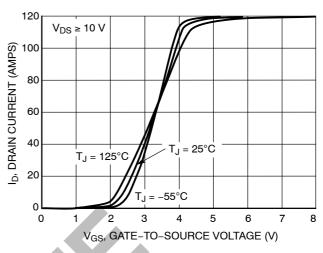


Figure 2. Transfer Characteristics

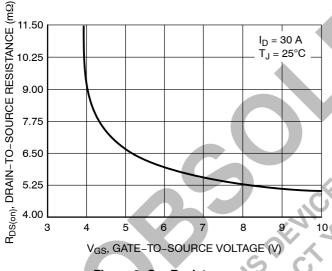


Figure 3. On-Resistance versus Gate-to-Source Voltage

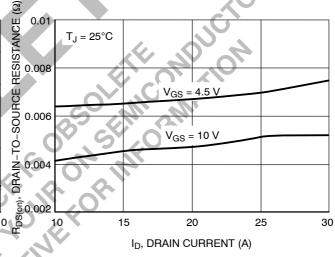


Figure 4. On-Resistance versus Drain Current and Gate Voltage

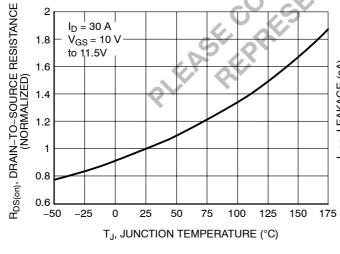


Figure 5. On–Resistance Variation with Temperature

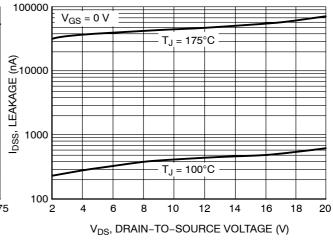
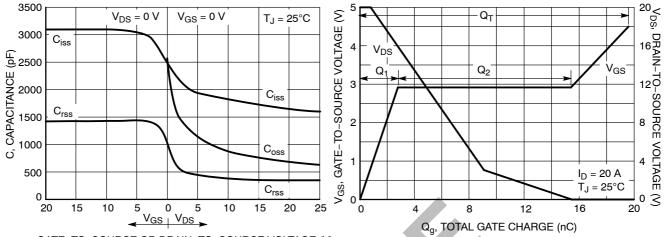
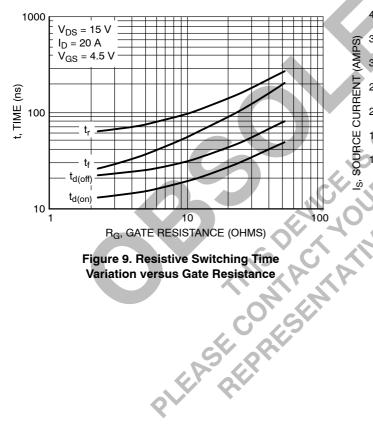


Figure 6. Drain-To-Source Leakage Current versus Voltage



GATE-TO-SOURCE OR DRAIN-TO-SOURCE VOLTAGE (V) Figure 7. Capacitance Variation

Figure 8. Gate-to-Source and **Drain-to-Source Voltage versus Total Charge**



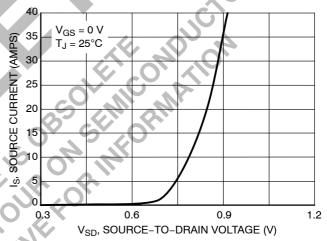
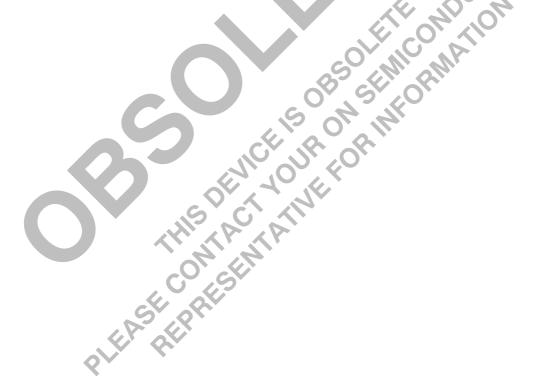


Figure 10. Diode Forward Voltage versus Current

ORDERING INFORMATION

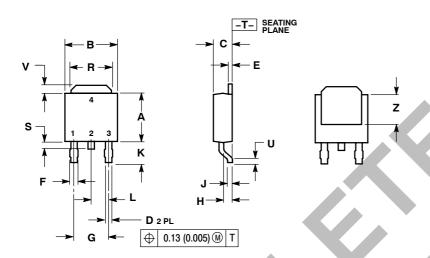
Order Number	Package	Shipping [†]
NTD78N03R	DPAK	
NTD78N03RG	DPAK (Pb-Free)	75 Units/Rail
NTD78N03RT4	DPAK	
NTD78N03RT4G	DPAK (Pb-Free)	2500 Tape & Reel
NTD78N03R-1	DPAK Straight Lead	
NTD78N03R-1G	DPAK Straight Lead (Pb-Free)	
NTD78N03R-35	DPAK Straight Lead (3.5 ± 0.15 mm)	75 Units/Rail
NTD78N03R-35G	DPAK Straight Lead (3.5 ± 0.15 mm) (Pb-Free)	

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



PACKAGE DIMENSIONS

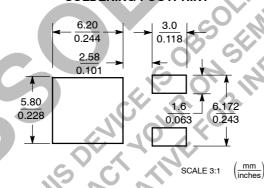
DPAK CASE 369C-01 ISSUE O



- NOTES: 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: INCH.

	INC	HES	MILLIMETERS		
DIM	MIN MAX		MIN	MAX	
Α	0.235	0.245	5.97	6.22	
В	0.250	0.265	6.35	6.73	
С	0.086	0.094	2.19	2.38	
D	0.027	0.035	0.69	0.88	
E	0.018	0.023	0.46	0.58	
F	0.037	0.045	0.94	1.14	
G	0.180	BSC	4.58 BSC		
Н	0.034	0.040	0.87	1.01	
J	0.018	0.023	0.46	0.58	
K	0.102	0.114	2.60	2.89	
L	0.090 BSC		2.29 BSC		
R	0.180	0.215	4.57	5.45	
S	0.025	0.040	0.63	1.01	
U	0.020		0.51		
٧	0.035	0.050	0.89	1.27	
Z	0.155	U	3.93		

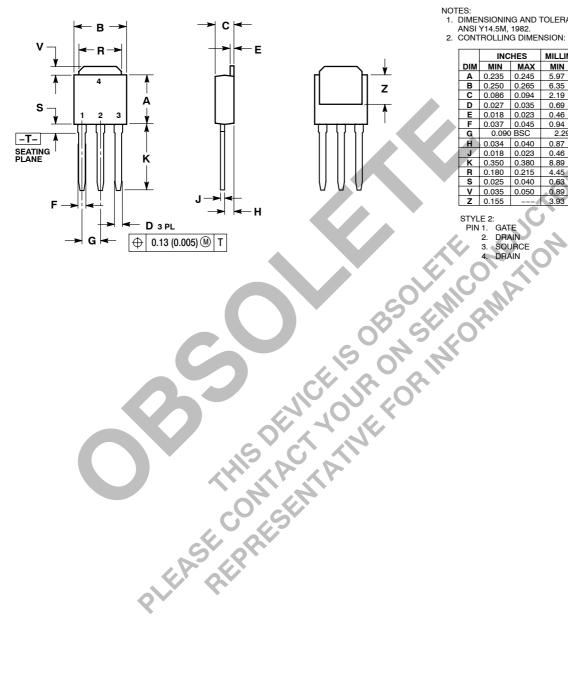
SOLDERING FOOTPRINT*

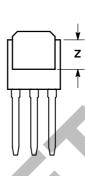


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

DPAK CASE 369D-01 **ISSUE B**





- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

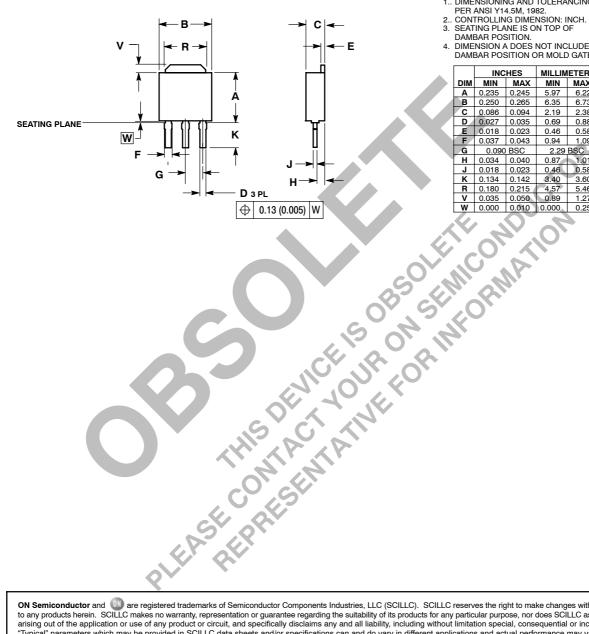
	INCHES		MILLIMETERS		
DIM	MIN MAX		MIN	MAX	
Α	0.235	0.245	5.97	6.35	
В	0.250	0.265	6.35	6.73	
С	0.086	0.094	2.19	2.38	
D	0.027	0.035	0.69	0.88	
Е	0.018	0.023	0.46	0.58	
F	0.037	0.045	0.94	1.14	
G	0.090 BSC		2.29 BSC		
H	0.034	0.040	0.87	1.01	
J	0.018	0.023	0.46	0.58	
Κ	0.350	0.380	8.89	9.65	
R	0.180	0.215	4.45	5.45	
S	0.025	0.040	0.63	1.01	
٧	0.035	0.050	0.89	1.27	
Z	0.155		3.93		

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PACKAGE DIMENSIONS

3 IPAK, STRAIGHT LEAD

CASE 369AC-01 ISSUE O



NOTES:

- DIMENSIONING AND TOLERANCING
 PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH. SEATING PLANE IS ON TOP OF
- 3. DAMBAR POSITION.
 DIMENSION A DOES NOT INCLUDE
- DAMBAR POSITION OR MOLD GATE.

	INCHES		MILLIMETERS		
DIM	MIN	MAX	MIN	MAX	
Α	0.235	0.245	5.97	6.22	
В	0.250	0.265	6.35	6.73	
C	0.086	0.094	2.19	2.38	
D	0.027	0.035	0.69	0.88	
E	0.018	0.023	0.46	0.58	
F	0.037	0.043	0.94	1.09	
G	0.090	BSC	2.29 BSC		
Н	0.034	0.040	0.87	1.01	
J	0.018	0.023	0.46	0.58	
K	0.134	0.142	3.40	3.60	
R	0.180	0.215	4.57	5.46	
٧	0.035	0.050	0.89	1.27	
W	0.000	0.010	0.000	0.25	
#					

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