PI6C2510A

Phase-Lock Loop Clock Driver with 10-Clock Outputs

Features

- High-Performance Phase-Lock Loop Clock Distribution that meets 100/134 MHz Registered DIMM Synchronous DRAM modules for server/workstation/PC applications
- Allows Clock Input to have Spread Spectrum modulation for EMI reduction
- Zero Input-to-Output delay: Distribute One Clock Input to one bank of ten outputs, with an output enable.
- Same pinout as TI CDC2510/2510A
- Low jitter: Cycle-to-Cycle jitter ±100ps max.
- On-chip series damping resistor at clock output drivers for low noise and EMI reduction
- Operates at 3.3V V_{CC}
- Wide Clock Frequency Range:
- Packaging
  -24-pin TSSOP (L)

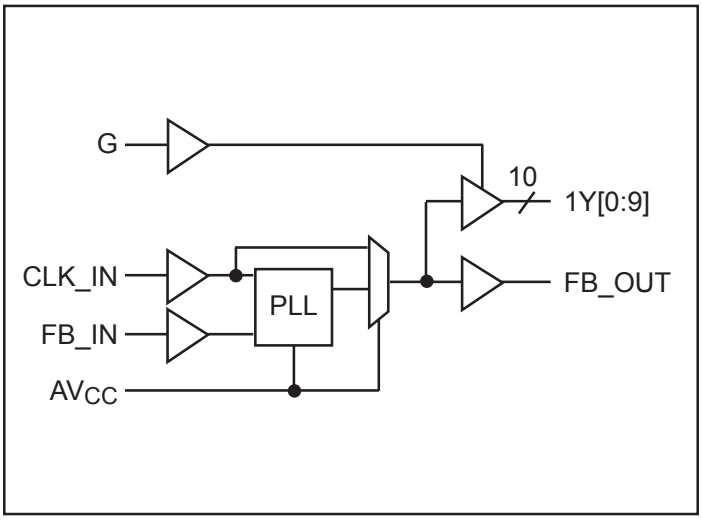
Description

The PI6C2510A family is a low-skew, low-jitter, phase-lock loop (PLL) clock driver, distributing high-frequency clock signals for SDRAM and server applications. By connecting the feedback FB_OUT output to the feedback FB_IN input, the propagation delay from the CLK_IN input to any clock output will be nearly zero. This zero-delay feature allows the CLK_IN input clock to be distributed, providing one clock input to one bank of ten outputs, with an output enable.

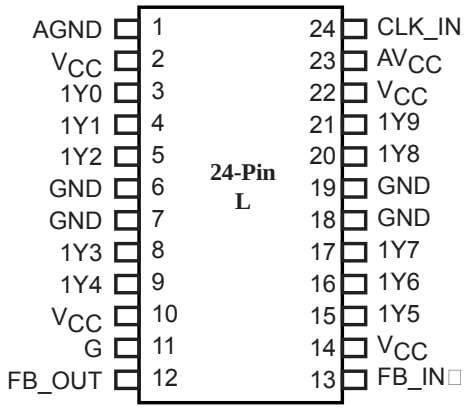
The PI6C2510A is designed to meet PC100 SDRAM Registered DIMM Specification, for heavy load applications. For test purposes, the PLL can be bypassed by strapping AV_{CC} to ground.

The PI6C2510A family has the same pinouts as TI's CDC2510A/2510B, with enhanced rise/fall times, and allowing a Spread Spectrum clock input.

Logic Block Diagram



Product Pin Configuration



Functional Table

Inputs		Outputs	
G	**CLK_IN**	**1Y[0:9]**	**FB_OUT**
X	L	L	L
L	H	L	H
H	H	H	H

Pin Functions

Pin Name	Pin No.	Type	Description
CLK_IN	24	I	Reference Clock input. CLK_IN allows spread spectrum of 0.5% underspread.
FB_IN	13	I	Feedback input. FB_IN provides the feedback signal to the internal PLL
G	11	I	Output bank enable. When G is LOW, outputs 1Y[09] are disabled to a logic low state. When G is HIGH, all outputs 1Y[0:9] are enabled.
FB_OUT	12	O	Feedback output. FB_OUT is dedicated for external feedback. FB_OUT has an embedded series-damping resistor of the same value as the clock outputs 1Yx, 2Yx.
1Y[0:9]	3,4,5,8,9,15 16,17,20,21	O	Clock outputs. These outputs provide low-skew copies of CLK_IN. Each output has an embedded series-damping resistor.
AV_{CC}	23	Power	Analog power supply. AV_{CC} can be also used to bypass the PLL for test purposes. When AV_{CC} is strapped to ground, PLL is bypassed and CLK_IN is buffered directly to the device outputs.
AGND	1	Ground	Analog ground. AGND provides the ground reference for the analog circuitry.
V_{CC}	2,10,14,22	Power	Power supply.
GND	6,7,18,19	Ground	Ground

DC Specifications

Absolute maximum ratings over operating free-air temperature range.

Symbol	Parameter	Min.	Max.	Units
V_I	Input voltage range	–0.5	V_{CC} +0.5	V
V_O	Output voltage range			
V_{I_DC}	DC input voltage		+5.0	
I_{O_DC}	DC output current		100	mA
Power	Maximum power dissipation at T_A =55°C in still air		1.0	W
T_{STG}	Storage temperature	–65	150	°C

Stress beyond those listed under “absolute maximum ratings” may cause permanent damage to the device.

Parameter	Test Conditions	V_{CC}	Min.	Typ.	Max.	Units
I_{CC}	V_I = V_{CC} or GND; I_O = 0	3.6V				mA
C_I	V_I = V_{CC} or GND	3.3V		4		pF
C_O	V_O = V_{CC} or GND			6		

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply voltage	3	3.6	V
V_{IH}	High level input voltage	2		
V_{IL}	Low level input voltage		0.8	
V_I	Input voltage	0	V_{CC}	
T_A	Operating free-air temperature	0	70	°C

Electrical characteristics over recommended operating free-air temperature range.

Pull Up/Down Currents of PI6C2510A/PI2510A-134, V_{CC} = 3.0V:

Symbol	Parameter	Condition	Min.	Max.	Units
I_{OH}	Pull-up current	V_{OUT} = 2.4V		–19	mA
	Pull-up current	V_{OUT} = 2.0V		–32	
I_{OL}	Pull-down current	V_{OUT} = 0.8V	28		
	Pull-down current	V_{OUT} = 0.55V	19		

AC Specifications

Timing requirements over recommended ranges of supply voltage and operating free-air temperature.

Symbol	Parameter	Min.	Max.	Units
Fclock	Clock frequency (PI6C2510A)	25	125	MHz
Fclock	Clock frequency (PI6C2510A-134)	25	134	
D_{CYI}	Input clock duty cycle	40	60	%
	Stabilization Time after power up		1	ms

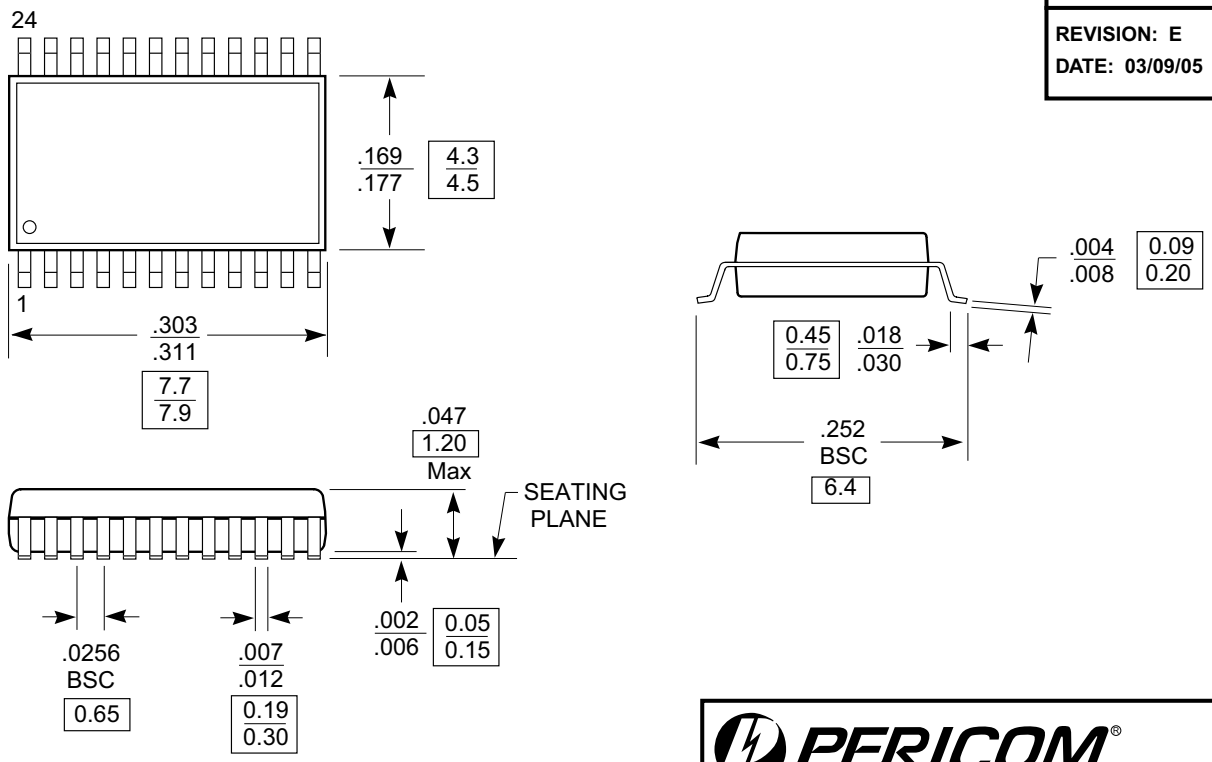
Switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L=30pF

Parameter	From (Input)	To (Output)	V_{CC} = 3.3V ±0.30V, 0-70°C			Units
			Min.	Typ.	Max.	
tphase error, with and without 0.5% spread spectrum	CLK_IN↑ at 100 MHz and 66 MHz	FB_IN↑	–150		+150	ps
Jitter, cycle-to-cycle, with and without 0.5% spread spectrum	Any Output or FB_OUT in CLKn, at 100 MHz and 66 MHz	Output or FB_OUT in CLKn+1	–100		+100	
Skew, at 100 MHz and 66 MHz	Any Y or FB_OUT	Any Y or FB_OUT			200	
Duty cycle			45		55	%
t_R, rise-time, 0.4V to 2.0V				1.0		ns
t_F, fall-time, 2.0V to 0.4V				1.1		

Note: These switching parameters are guaranteed, but not production tested.

Package Mechanical Information:

Plastic 24-pin Thin Shrink Small-Outline Package (L package).



DOCUMENT CONTROL NO.
PD - 1312

REVISION: E
DATE: 03/09/05

Note:
1. Package Outline Exclusive of Mold Flash and Metal Burr
2. Controlling dimentions in millimeters
3. Ref: JEDEC MO-153F/AD

Pericom Semiconductor Corporation
3545 N. 1st Street, San Jose, CA 95134
1-800-435-2335 • www.pericom.com

DESCRIPTION: 24-Pin, 173-Mil Wide, TSSOP

PACKAGE CODE: L

Ordering Information

Order Code	Package Code	Package Description
PI6C2510ALE	L	Pb-free & Green, 24-pin TSSOP

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/

2. Number of transistors = TBD

3. E = Pb-free and Green