

DATA SHEET

PDTA115E series

PNP resistor-equipped transistors;

R1 = 100 k Ω , R2 = 100 k Ω

Product specification
Supersedes data of 2004 May 05

2004 Jul 30

PNP resistor-equipped transistors; R1 = 100 k Ω , R2 = 100 k Ω

PDTA115E series

FEATURES

- Built-in bias resistors
- Simplified circuit design
- Reduction of component count
- Reduced pick and place costs.

APPLICATIONS

- General purpose switching and amplification
- Inverter and interface circuits
- Circuit driver.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V _{CEO}	collector-emitter voltage	–	–50	V
I _O	output current (DC)	–	–20	mA
R1	bias resistor	100	–	k Ω
R2	bias resistor	100	–	k Ω

DESCRIPTION

PNP resistor-equipped transistor (see “Simplified outline, symbol and pinning” for package details).

PRODUCT OVERVIEW

TYPE NUMBER	PACKAGE		MARKING CODE	NPN COMPLEMENT
	PHILIPS	EIAJ		
PDTA115EE	SOT416	SC-75	5E	PDTC115EE
PDTA115EEF	SOT490	SC-89	6B	PDTC115EEF
PDTA115EK	SOT346	SC-59	62	PDTC115EK
PDTA115EM	SOT883	SC-101	F6	PDTC115EM
PDTA115ES	SOT54 (TO-92)	SC-43	TA115E	PDTC115ES
PDTA115ET	SOT23	–	*AB ⁽¹⁾	PDTC115ET
PDTA115EU	SOT323	SC-70	*7C ⁽¹⁾	PDTC115EU

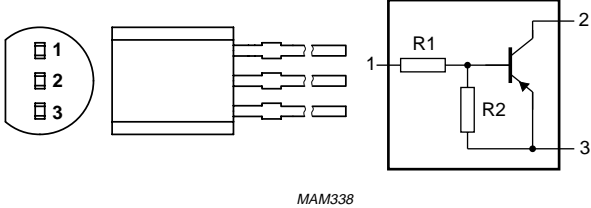
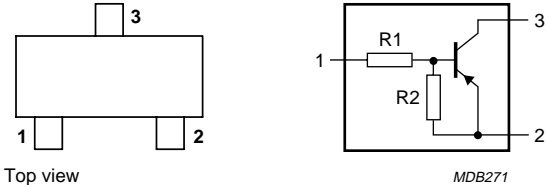
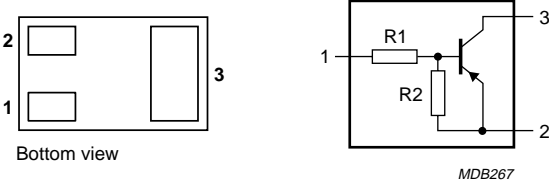
Note

- * = p: Made in Hong Kong.
* = t: Made in Malaysia.
* = W: Made in China.

PNP resistor-equipped transistors;
R1 = 100 kΩ, R2 = 100 kΩ

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SIMPLIFIED OUTLINE, SYMBOL AND PINNING

TYPE NUMBER	SIMPLIFIED OUTLINE AND SYMBOL	PINNING	
		PIN	DESCRIPTION
PDTA115ES		1 2 3	base collector emitter
PDTA115EE PDTA115EEF PDTA115EK PDTA115ET PDTA115EU		1 2 3	base emitter collector
PDTA115EM		1 2 3	base emitter collector

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ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PDTA115EE	–	plastic surface mounted package; 3 leads	SOT416
PDTA115EEF	–	plastic surface mounted package; 3 leads	SOT490
PDTA115EK	–	plastic surface mounted package; 3 leads	SOT346
PDTA115EM	–	leadless ultra small plastic package; 3 solder lands; body 1.0 × 0.6 × 0.5 mm	SOT883
PDTA115ES	–	plastic single-ended leaded (through hole) package; 3 leads	SOT54
PDTA115ET	–	plastic surface mounted package; 3 leads	SOT23
PDTA115EU	–	plastic surface mounted package; 3 leads	SOT323

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CBO}	collector-base voltage	open emitter	–	–50	V
V _{CEO}	collector-emitter voltage	open base	–	–50	V
V _{EBO}	emitter-base voltage	open collector	–	–10	V
V _I	input voltage				
	positive		–	+10	V
	negative		–	–40	V
I _O	output current (DC)		–	–20	mA
I _{CM}	peak collector current		–	–100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C			
	SOT23	note 1	–	250	mW
	SOT54	note 1	–	500	mW
	SOT323	note 1	–	200	mW
	SOT346	note 1	–	250	mW
	SOT416	note 1	–	150	mW
	SOT490	notes 1 and 2	–	250	mW
	SOT883	notes 2 and 3	–	250	mW
T _{stg}	storage temperature		–65	+150	°C
T _j	junction temperature		–	150	°C
T _{amb}	operating ambient temperature		–65	+150	°C

Notes

1. Refer to standard mounting conditions.
2. Reflow soldering is the only recommended soldering method.
3. Refer to SOT883 standard mounting conditions; FR4 with 60 μ m copper strip line.

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th(j-a)}	thermal resistance from junction to ambient	T _{amb} ≤ 25 °C		
	SOT23	note 1	500	K/W
	SOT54	note 1	250	K/W
	SOT323	note 1	625	K/W
	SOT346	note 1	500	K/W
	SOT416	note 1	833	K/W
	SOT490	notes 1 and 2	500	K/W
	SOT883	notes 2 and 3	500	K/W

Notes

1. Refer to standard mounting conditions.
2. Reflow soldering is the only recommended soldering method.
3. Refer to SOT883 standard mounting conditions; FR4 with 60 μ m copper strip line.

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I _{CBO}	collector-base cut-off current	V _{CB} = -50 V; I _E = 0 A	–	–	-100	nA
I _{CEO}	collector-emitter cut-off current	V _{CE} = -30 V; I _B = 0 A	–	–	-1	μ A
		V _{CE} = -30 V; I _B = 0 A; T _j = 150 °C	–	–	-50	μ A
I _{EBO}	emitter-base cut-off current	V _{EB} = -5 V; I _C = 0 A	–	–	-50	μ A
h _{FE}	DC current gain	V _{CE} = -5 V; I _C = -5 mA	80	–	–	
V _{CEsat}	collector-emitter saturation voltage	I _C = -5 mA; I _B = -0.25 mA	–	–	-150	mV
V _{i(off)}	input-off voltage	I _C = -100 μ A; V _{CE} = -5 V	–	-1.2	-0.5	V
V _{i(on)}	input-on voltage	I _C = -1 mA; V _{CE} = -0.3 V	-3	-1.6	–	V
R1	input resistor		70	100	130	k Ω
$\frac{R2}{R1}$	resistor ratio		0.8	1	1.2	
C _c	collector capacitance	I _E = i _e = 0 A; V _{CB} = -10 V; f = 1 MHz	–	–	3	pF

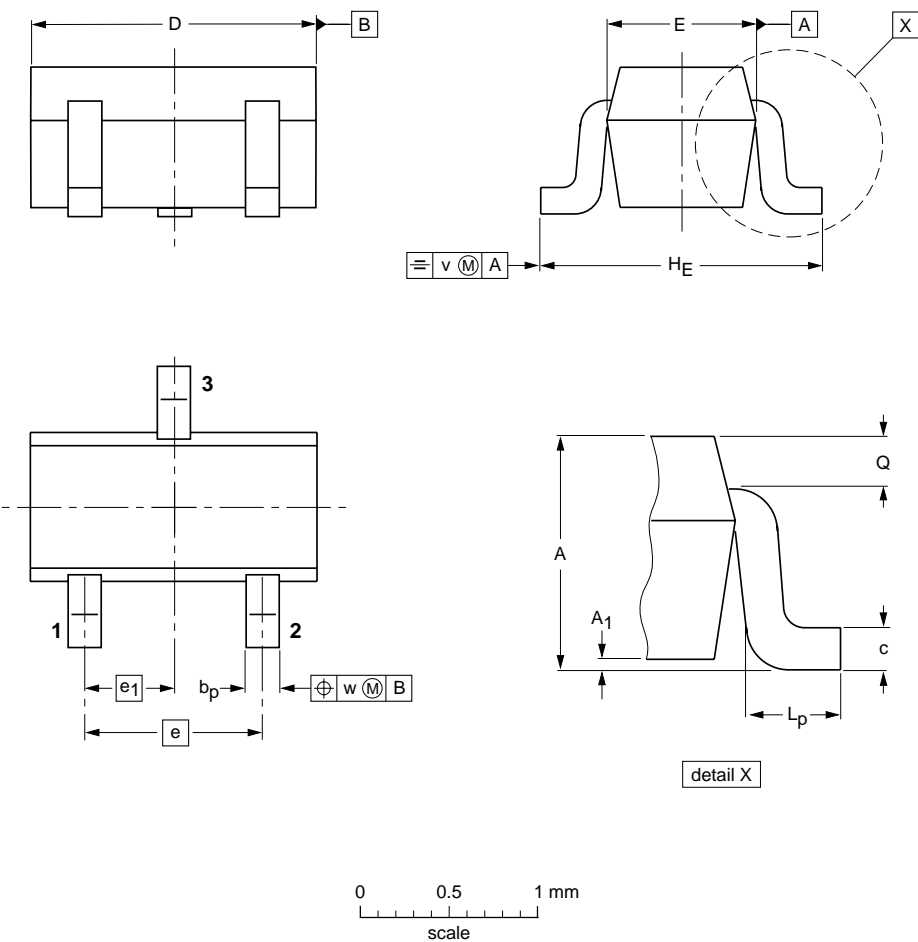
PNP resistor-equipped transistors;
R1 = 100 kΩ, R2 = 100 kΩ

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PACKAGE OUTLINES


Plastic surface mounted package; 3 leads

SOT416



DIMENSIONS (mm are the original dimensions)

UNIT	A	A1 max	bp	c	D	E	e	e1	HE	Lp	Q	v	w
mm	0.95 0.60	0.1	0.30 0.15	0.25 0.10	1.8 1.4	0.9 0.7	1	0.5	1.75 1.45	0.45 0.15	0.23 0.13	0.2	0.2

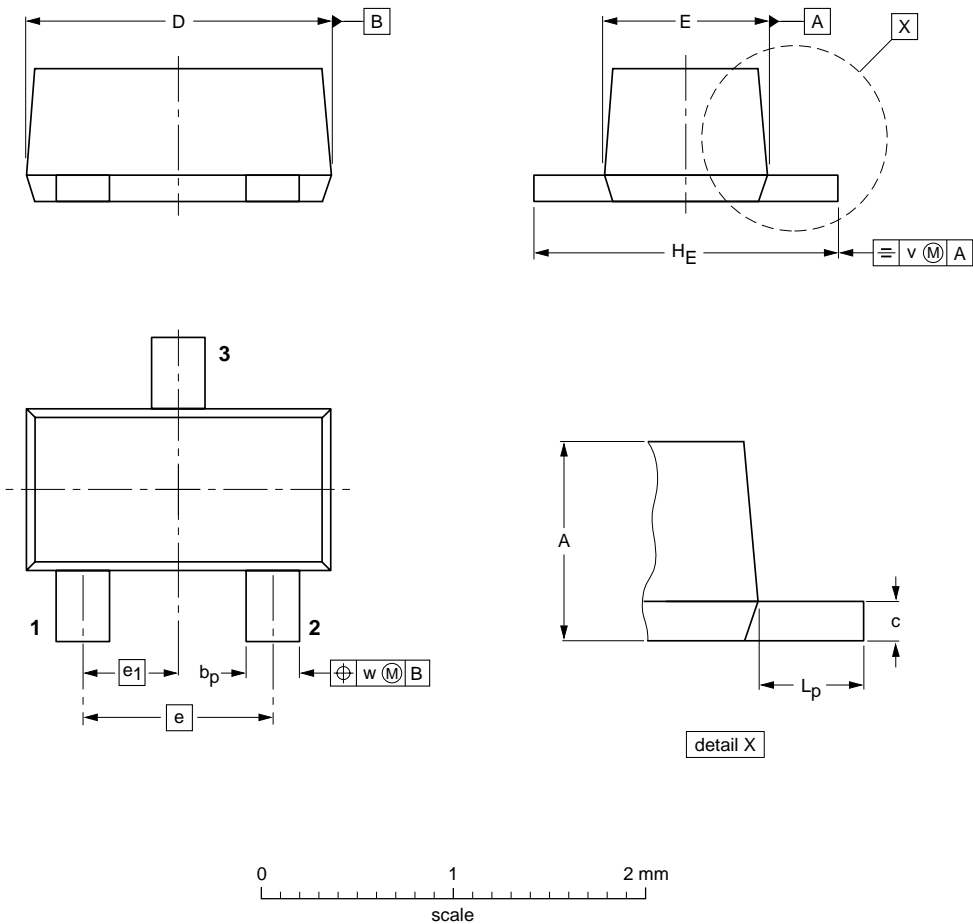
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT416			SC-75			97-02-28

PNP resistor-equipped transistors;
R1 = 100 kΩ, R2 = 100 kΩ

PDTA115E series

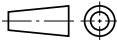
Plastic surface mounted package; 3 leads

SOT490



DIMENSIONS (mm are the original dimensions)

UNIT	A	b _p	c	D	E	e	e ₁	H _E	L _p	v	w
mm	0.8 0.6	0.33 0.23	0.2 0.1	1.7 1.5	0.95 0.75	1.0	0.5	1.7 1.5	0.5 0.3	0.1	0.1

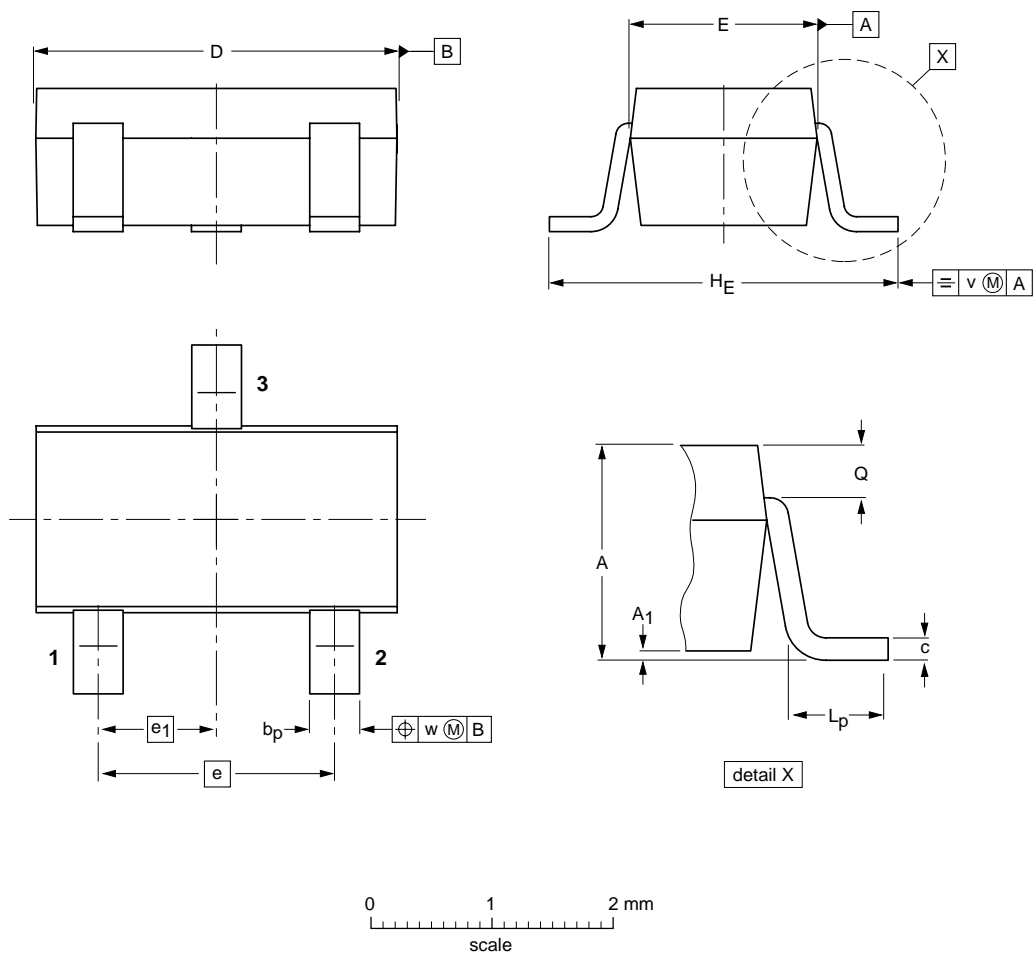
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	IEC	JEDEC	EIAJ			
SOT490			SC-89			98-10-23

PNP resistor-equipped transistors;
R1 = 100 kΩ, R2 = 100 kΩ

PDTA115E series

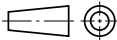
Plastic surface mounted package; 3 leads

SOT346



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b _p	c	D	E	e	e ₁	H _E	L _p	Q	v	w
mm	1.3 1.0	0.1 0.013	0.50 0.35	0.26 0.10	3.1 2.7	1.7 1.3	1.9	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2

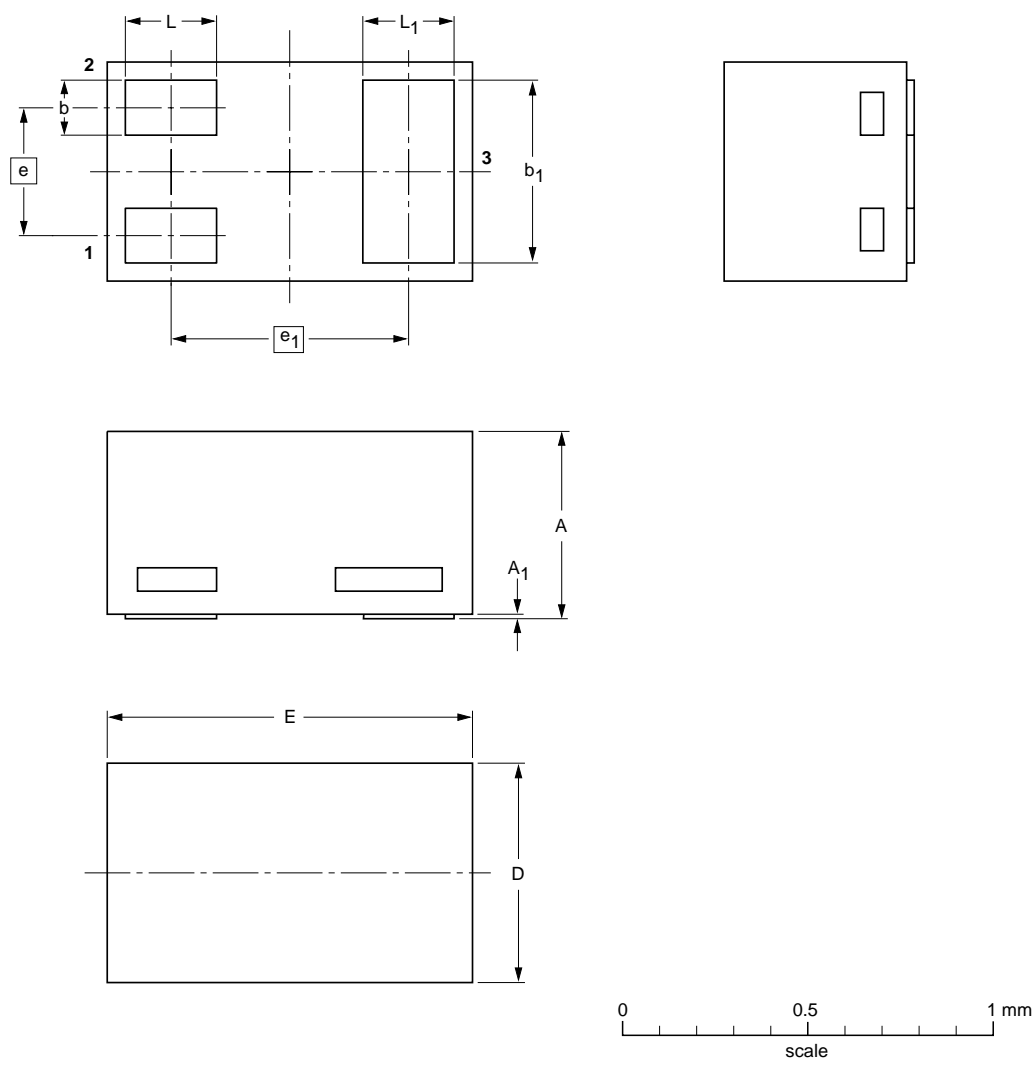
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT346		TO-236	SC-59			98-07-17

PNP resistor-equipped transistors;
R1 = 100 kΩ, R2 = 100 kΩ

PDTA115E series

Leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.5 mm

SOT883



DIMENSIONS (mm are the original dimensions)

UNIT	A ⁽¹⁾	A ₁ max.	b	b ₁	D	E	e	e ₁	L	L ₁
mm	0.50 0.46	0.03	0.20 0.12	0.55 0.47	0.62 0.55	1.02 0.95	0.35	0.65	0.30 0.22	0.30 0.22

Note
1. Including plating thickness

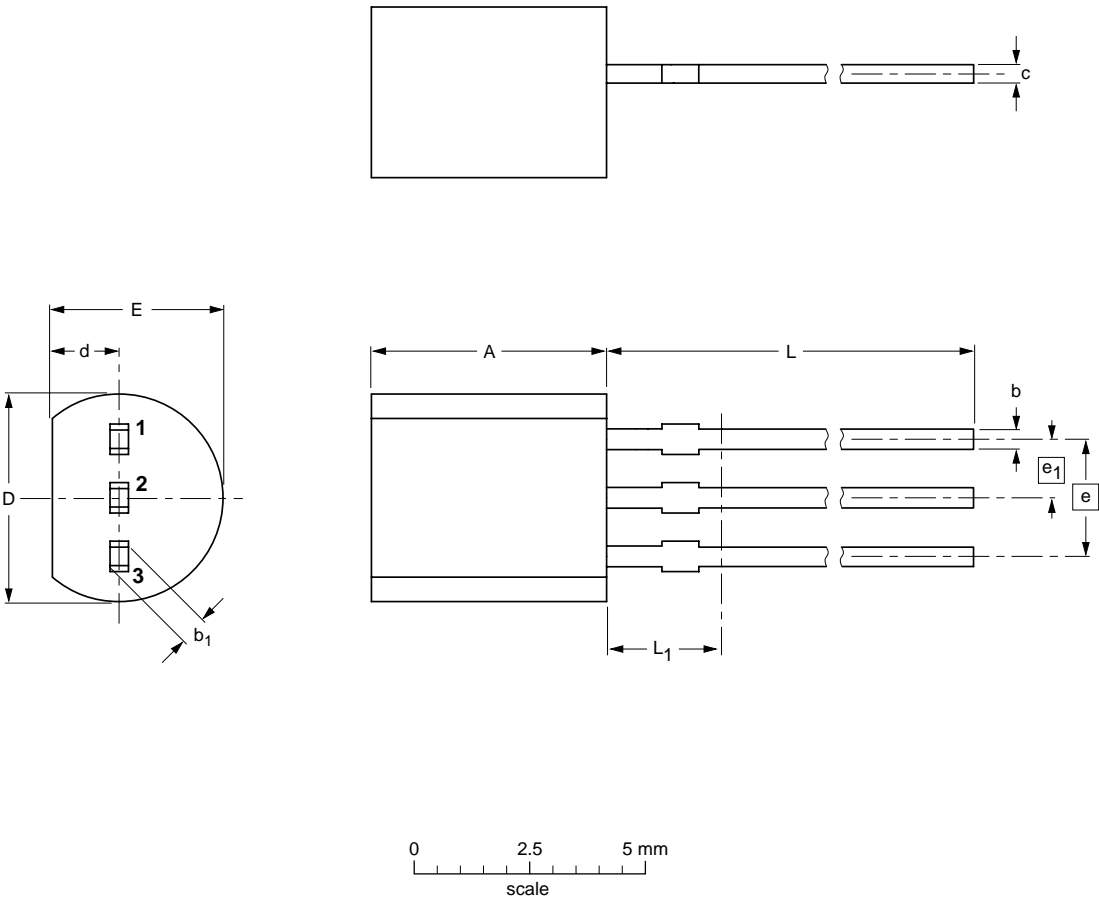
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	IEC	JEDEC	JEITA			
SOT883			SC-101			03-02-05 03-04-03

PNP resistor-equipped transistors;
R1 = 100 kΩ, R2 = 100 kΩ

PDTA115E series

Plastic single-ended leaded (through hole) package; 3 leads

SOT54



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b ₁	c	D	d	E	e	e ₁	L	L ₁ ⁽¹⁾ max.
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.38	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note
1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

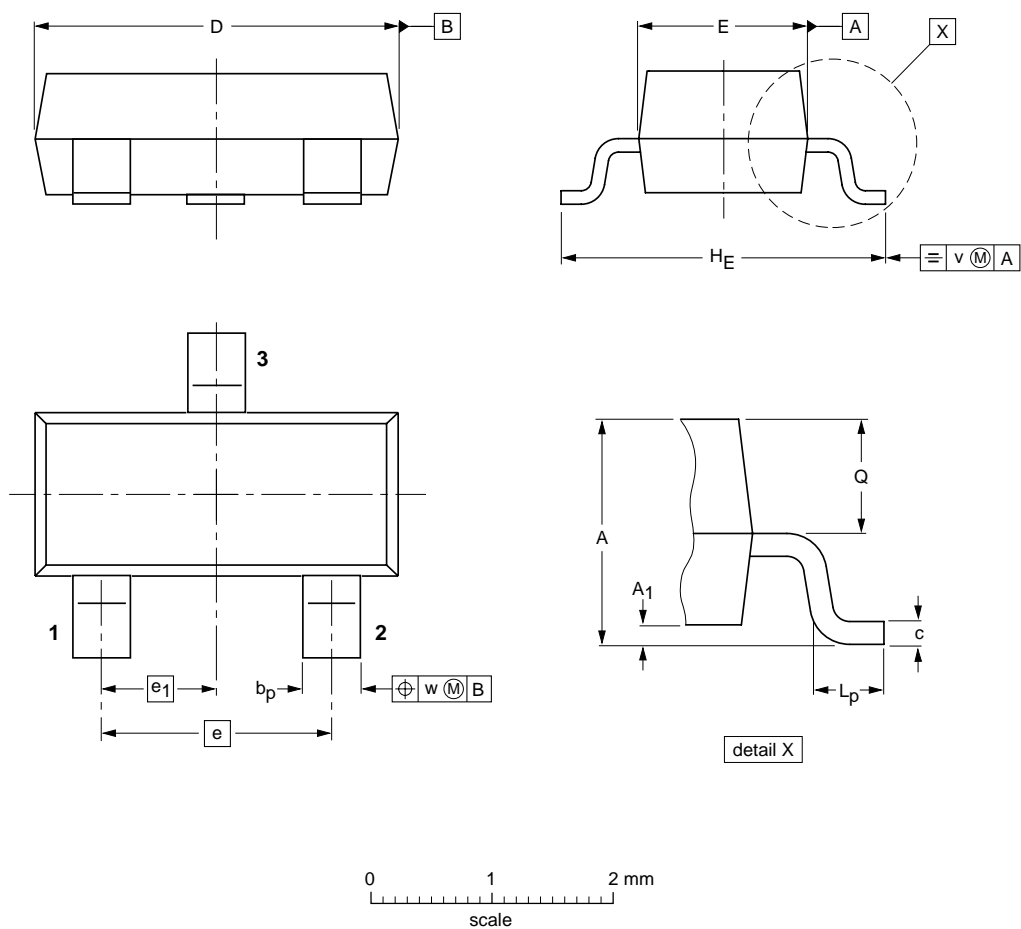
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	IEC	JEDEC	JEITA			
SOT54		TO-92	SC-43A			97-02-28 04-06-28

PNP resistor-equipped transistors;
R1 = 100 kΩ, R2 = 100 kΩ

PDTA115E series

Plastic surface mounted package; 3 leads

SOT23



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max.	b _P	c	D	E	e	e ₁	H _E	L _P	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

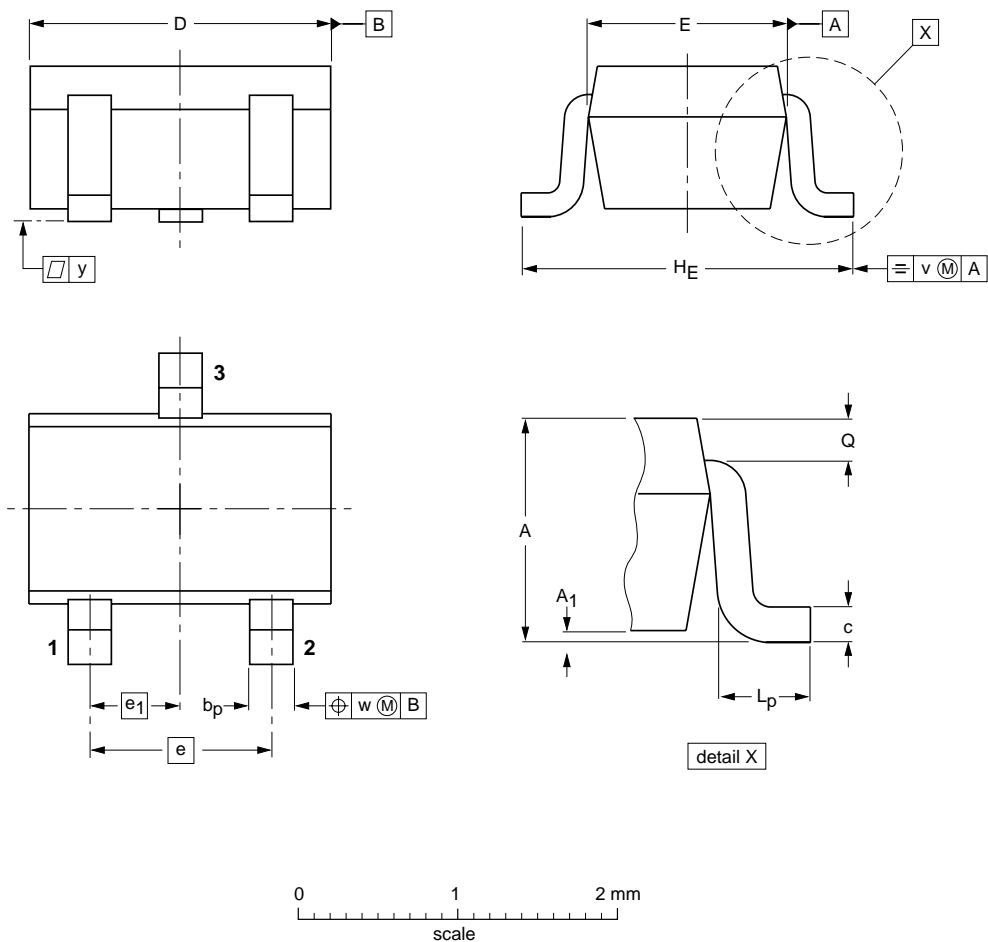
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT23		TO-236AB				97-02-28 99-09-13

PNP resistor-equipped transistors;
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PDTA115E series

Plastic surface mounted package; 3 leads

SOT323



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	c	D	E	e	e ₁	H _E	L _p	Q	v	w
mm	1.1 0.8	0.1	0.4 0.3	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT323			SC-70			97-02-28

PNP resistor-equipped transistors;
R1 = 100 k Ω , R2 = 100 k Ω

PDTA115E series

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Contact information

For additional information please visit **<http://www.semiconductors.philips.com>**. Fax: **+31 40 27 24825**

For sales offices addresses send e-mail to: **sales.addresses@www.semiconductors.philips.com**.

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Printed in The Netherlands

R75/03/pp14

Date of release: 2004 Jul 30

Document order number: 9397 750 13648

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