

Preliminary

TOSHIBA CMOS Digital Integrated Circuit
Silicon Monolithic

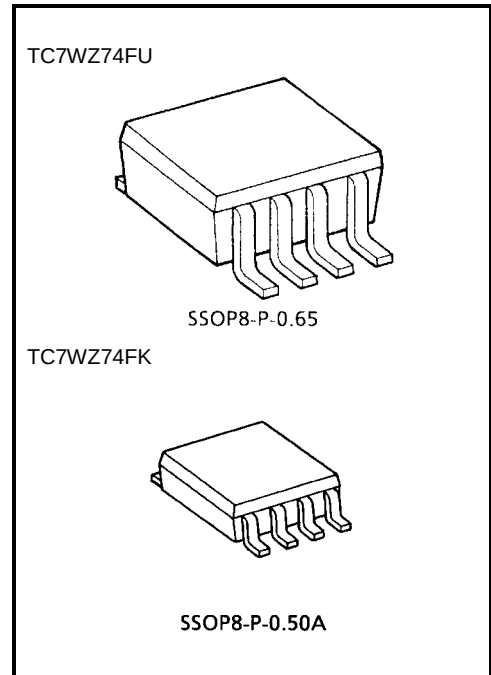
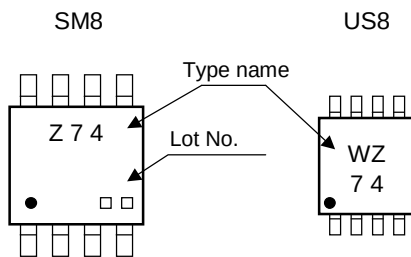
TC7WZ74FU, TC7WZ74FK

D-Type Flip Flop with Preset and Clear

Features

- High output current: ± 24 mA (min) @ $V_{CC} = 3$ V
- Propagation delay time: t_{pd} 2.8 ns (typ.) @ $V_{CC} = 3$ V, 50 pF
- Operating voltage range: $V_{CC} (opr) = 1.65 \sim 5.5$ V
- High latch-up immunity: ± 500 mA or more
- High ESD: ± 200 V or more (JEITA)
 ± 2000 V or more (MIL)
- Power down protection is provided on all inputs.
- Electrical characteristics when $V_{CC} = 3.3$ V is the same as TC74LCX series.

Marking

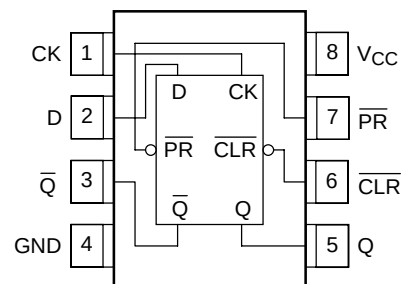


Weight
SSOP8-P-0.65 : 0.02 g (typ.)
SSOP8-P-0.50A : 0.01 g (typ.)

Maximum Ratings ($T_a = 25^\circ\text{C}$)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	$-0.5 \sim 6$	V
DC input voltage	V_{IN}	$-0.5 \sim 6$	V
DC output voltage	V_{OUT}	$-0.5 \sim 6$	V
Input diode current	I_{IK}	-20	mA
Output diode current	I_{OK}	-20	mA
DC output current	I_{OUT}	± 50	mA
DC V_{CC} /ground current	I_{CC}	± 50	mA
Power dissipation	P_D	300 (SM8) 200 (US8)	mW
Storage temperature	T_{stg}	$-65 \sim 150$	$^\circ\text{C}$
Lead temperature (10s)	T_L	260	$^\circ\text{C}$

Pin Assignment (top view)

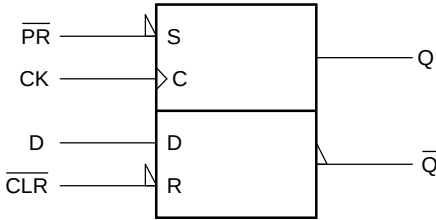


Truth Table

Inputs				Outputs		Function
$\overline{\text{CLR}}$	$\overline{\text{PR}}$	D	CK	Q	$\overline{\text{Q}}$	
L	H	X	X	L	H	Clear
H	L	X	X	H	L	Preset
L	L	X	X	H	H	—
H	H	L	$\uparrow$	L	H	—
H	H	H	$\uparrow$	H	L	—
H	H	X	$\downarrow$	Qn	Qn	No Change

X: Don't care

Logic Diagram



Recommended Operating Conditions

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	1.65~5.5	V
		1.5~5.5 (Note 1)	
Input voltage	V_{IN}	0~5.5	V
Output voltage	V_{OUT}	0~5.5 (Note 2)	V
		0~ V_{CC} (Note 3)	
Operating temperature	T_{opr}	-40~85	°C
Input rise and fall time	dt/dv	0~20 ($V_{\text{CC}} = 1.8 \text{ V} \pm 0.15 \text{ V}$, 2.5 V $\pm 0.2 \text{ V}$)	ns/V
		0~10 ($V_{\text{CC}} = 3.3 \text{ V} \pm 0.3 \text{ V}$)	
		0~5 ($V_{\text{CC}} = 5.5 \text{ V} \pm 0.5 \text{ V}$)	

Note 1: Data retention only

Note 2: $V_{\text{CC}} = 0 \text{ V}$

Note 3: High or low

Electrical Characteristics
DC Characteristics

Characteristics		Symbol	Test Condition		Ta = 25°C				Ta = -40~85°C		Unit
					V _{CC} (V)	Min	Typ.	Max	Min	Max	
Input voltage	High level	V _{IH}	—	1.65~1.8	0.75 × V _{CC}	—	—	0.75 × V _{CC}	—	V	
				2.3~5.5	0.7 × V _{CC}	—	—	0.7 × V _{CC}	—		
	Low level	V _{IL}	—	1.65~1.8	—	—	0.25 × V _{CC}	—	0.25 × V _{CC}		
				2.3~5.5	—	—	0.3 × V _{CC}	—	0.3 × V _{CC}		
Output voltage	High level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = -100 μA	1.65	1.55	1.65	—	1.55	—	V
					2.3	2.2	2.3	—	2.2	—	
					3.0	2.9	3.0	—	2.9	—	
					4.5	4.4	4.5	—	4.4	—	
				I _{OL} = -4 mA	1.65	1.29	1.52	—	1.29	—	
				I _{OL} = -8 mA	2.3	1.9	2.15	—	1.9	—	
				I _{OL} = -16 mA	3.0	2.4	2.8	—	2.4	—	
				I _{OL} = -24 mA	3.0	2.3	2.68	—	2.3	—	
				I _{OL} = -32 mA	4.5	3.8	4.2	—	3.8	—	
	Low level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100 μA	1.8	—	0	0.1	—	0.1	V
					2.3	—	0	0.1	—	0.1	
					3.0	—	0	0.1		0.1	
					4.5	—	0	0.1	—	0.1	
				I _{OL} = 4 mA	1.65	—	0.08	0.24	—	0.24	
				I _{OL} = 8 mA	2.3	—	0.1	0.3		0.3	
				I _{OL} = 16 mA	3.0	—	0.15	0.4		0.4	
				I _{OL} = 24 mA	3.0	—	0.22	0.55		0.55	
				I _{OL} = 32 mA	4.5	—	0.22	0.55	—	0.55	
Input leakage current		I _{IN}	V _{IN} = 5.5 V or GND	0~5.5	—	—	±1	—	±10	μA	
Power OFF leak current		I _{OFF}	V _{IN} or V _{OUT} = 5.5 V	0.0	—	—	1	—	10	μA	
Quiescent supply current		I _{CC}	V _{IN} = 5.5 V or GND	1.65~5.5	—	—	1	—	10	μA	

AC Characteristics (unless otherwise specified, Input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40~85°C		Unit
			V _{CC} (V)	Min	Typ.	Max	Min	Max	
Maximum clock frequency	f _{MAX}	C _L = 50 pF, R _L = 500 Ω	1.8 ± 0.15	51	—	—	38	—	MHz
			2.5 ± 0.2	130	—	—	100	—	
			3.3 ± 0.3	200	—	—	150	—	
			5.0 ± 0.5	200	—	—	180	—	
Propagation delay time (CK-Q, $\overline{Q}$)	t _{pLH} t _{pHL}	C _L = 15 pF, R _L = 1 MΩ	1.8 ± 0.15	2.5	10.0	18.0	2.1	23.0	ns
			2.5 ± 0.2	2.0	4.9	7.5	1.7	9.0	
			3.3 ± 0.3	1.5	3.3	4.8	1.3	5.6	
			5.0 ± 0.5	1.0	2.4	3.5	1.0	3.9	
		C _L = 50 pF, R _L = 500 Ω	3.3 ± 0.3	2.0	4.3	5.7	1.5	7.0	
			5.0 ± 0.5	1.5	2.8	4.0	1.3	4.4	
Propagation delay time ($\overline{CLR}$, $\overline{PR}$ -Q, $\overline{Q}$)	t _{pLH} t _{pHL}	C _L = 15 pF, R _L = 1 MΩ	1.8 ± 0.15	2.5	10.0	17.0	2.1	21.0	ns
			2.5 ± 0.2	2.0	5.0	7.3	1.7	8.8	
			3.3 ± 0.3	1.5	3.4	4.8	1.3	5.6	
			5.0 ± 0.5	1.5	2.2	3.5	1.0	3.9	
		C _L = 50 pF, R _L = 500 Ω	3.3 ± 0.3	2.0	4.3	5.7	1.5	7.0	
			5.0 ± 0.5	1.0	3.1	3.9	1.0	4.3	
Minimum setup time	t _s	C _L = 50 pF, R _L = 500 Ω	2.5 ± 0.2	3.4	—	—	4.1	—	ns
			3.3 ± 0.3	2.1	—	—	2.5	—	
			5.0 ± 0.5	1.5	—	—	1.7	—	
Minimum hold time	t _h	C _L = 50 pF, R _L = 500 Ω	2.5 ± 0.2	2.4	—	—	2.9	—	ns
			3.3 ± 0.3	1.4	—	—	1.5	—	
			5.0 ± 0.5	1.0	—	—	1.1	—	
Minimum pulse width (CK)	t _W (L) t _W (H)	C _L = 50 pF, R _L = 500 Ω	2.5 ± 0.2	3.0	—	—	3.6	—	ns
			3.3 ± 0.3	3.0	—	—	3.3	—	
			5.0 ± 0.5	3.0	—	—	3.2	—	
Minimum pulse width ($\overline{CLR}$, $\overline{PR}$)	t _W (L)	C _L = 50 pF, R _L = 500 Ω	2.5 ± 0.2	3.0	—	—	3.6	—	ns
			3.3 ± 0.3	3.0	—	—	3.3	—	
			5.0 ± 0.5	3.0	—	—	3.2	—	
Minimum removal time	t _{rem}	C _L = 50 pF, R _L = 500 Ω	2.5 ± 0.2	3.6	—	—	4.4	—	ns
			3.3 ± 0.3	2.2	—	—	2.5	—	
			5.0 ± 0.5	1.3	—	—	1.4	—	
Input capacitance	C _{IN}	—	0~0.5	—	3.0	—	—	—	pF
Output capacitance	C _{OUT}	—	0~0.5	—	5.0	—	—	—	pF
Power dissipation capacitance	C _{PD}	(Note 4)	3.3	—	30	—	—	—	pF
			5.5	—	47	—	—	—	

Note 4: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

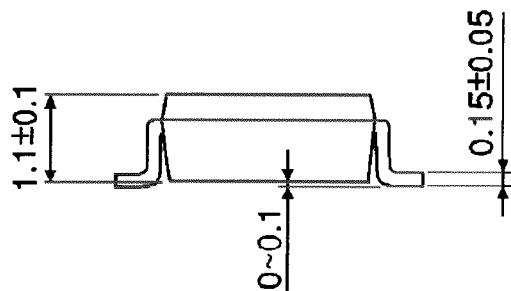
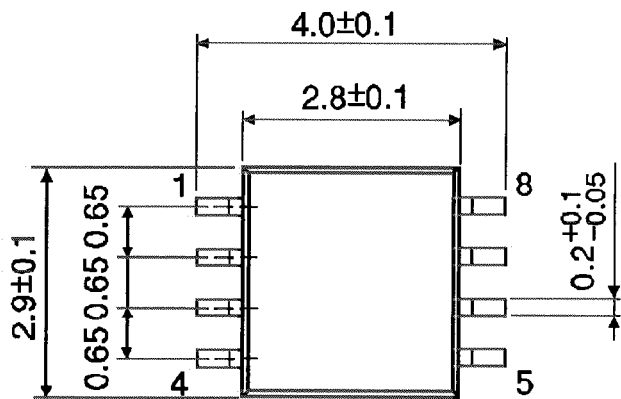
Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

Package Dimensions

SSOP8-P-0.65

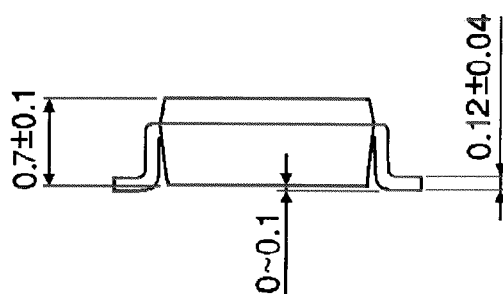
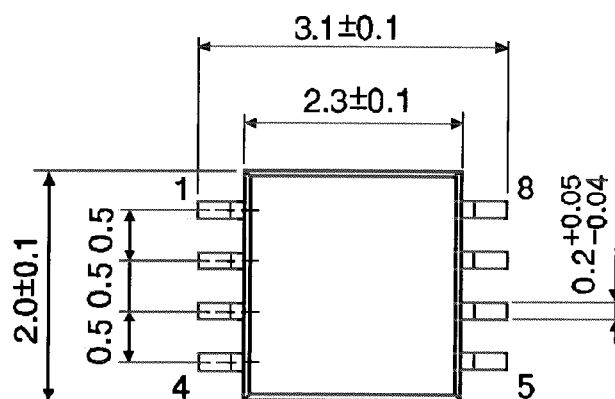
Unit : mm



Weight: 0.02 g (typ.)

SSOP8-P-0.50A

Unit : mm



Weight: 0.01 g (typ.)

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