

Product Summary

V _{BR} (min)	I _{PP} (max)	C _T (typ)
6V	5.5A	0.55pF

Description

The DT1240V3-04LP-7 is a high-performance device suitable for protecting four high speed I/Os. These devices are assembled in DFN2510-10 packages and have high ESD surge capability and low capacitance.

Applications

Typically used at high-speed ports such as USB 2.0, IEEE1394 (Firewire®, iLink™), Serial ATA, DVI, HDMI, PCI.

Features

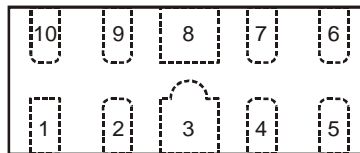
- Clamping Voltage: 8.8V at 10A 100ns, TLP 9V at 5.5A 8μs/20μs
- IEC 61000-4-2 (ESD): Air — ±16kV, Contact — ±14kV
- IEC 61000-4-5 (Lightning): ±5.5A (8/20μs)
- 4 Channels of ESD protection
- Low Channel Input Capacitance of 0.55pF Typical
- TLP Dynamic Resistance: 0.3Ω
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- Halogen and Antimony Free. "Green" Device (Note 3)**

Mechanical Data

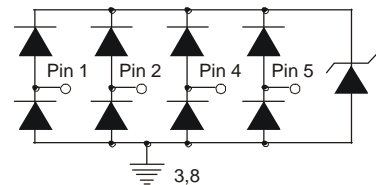
- Case: U-DFN2510-10
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Schematic
- Terminals: Finish – NiPdAu, Solderable per MIL-STD-202, Method 208 (e4)
- Weight: 0.038 grams (Approximate)

U-DFN2510-10

Pin #	Description
1, 2, 4, 5	I/O
6, 7, 9, 10	No Connection
3, 8	V _{SS}



Pin Description (Top View)



Device Schematic

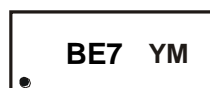
Ordering Information (Note 4)

Product	Compliance	Marking	Reel Size (inches)	Tape Width (mm)	Quantity per Reel
DT1240V3-04LP-7	Standard	BE7	7	8	3,000/Tape & Reel

- Notes:
- No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
 - See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 - Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 - For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information

U-DFN2510-10



BE7 = Product Type Marking Code
 YM = Date Code Marking
 Y = Year (ex: A = 2013)
 M = Month (ex: 9 = September)

Date Code Key

Year	2013	2014	2015	2016	2017	2018
Code	A	B	C	D	E	F

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit	Conditions
Peak Pulse Current, per IEC 61000-4-5	I _{PP}	5.5	A	I/O to V _{SS} , 8/20μs
Peak Pulse Power, per IEC 61000-4-5	P _{PP}	60	W	I/O to V _{SS} , 8/20μs
ESD Protection – Contact Discharge, per IEC 61000-4-2	V _{ESD_Contact}	±14	kV	I/O to V _{SS}
ESD Protection – Air Discharge, per IEC 61000-4-2	V _{ESD_Air}	±16	kV	I/O to V _{SS}
Operating Temperature	T _{OP}	-55 to +85	°C	—
Storage Temperature	T _{STG}	-55 to +150	°C	—

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Power Dissipation Typical (Note 5)	P _D	350	mW
Thermal Resistance, Junction to Ambient Typical (Note 5)	R _{θJA}	360	°C/W

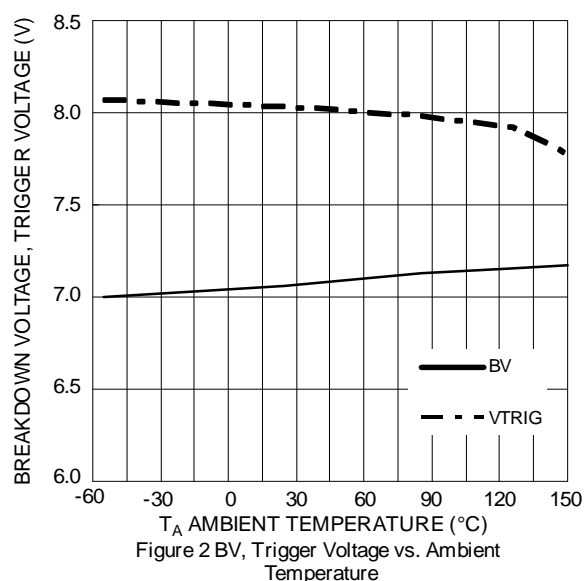
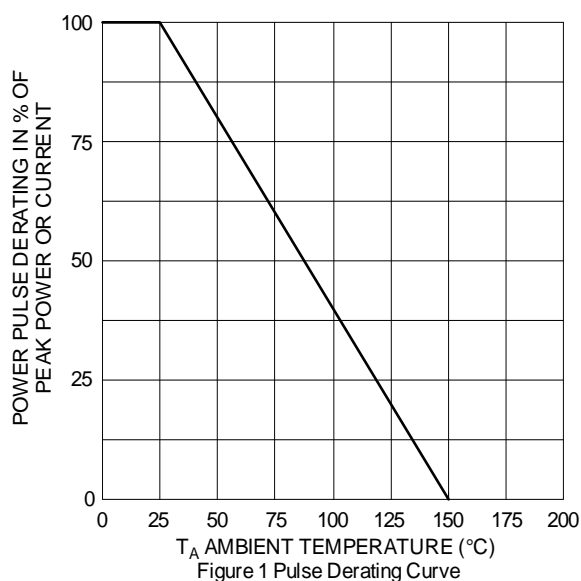
Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

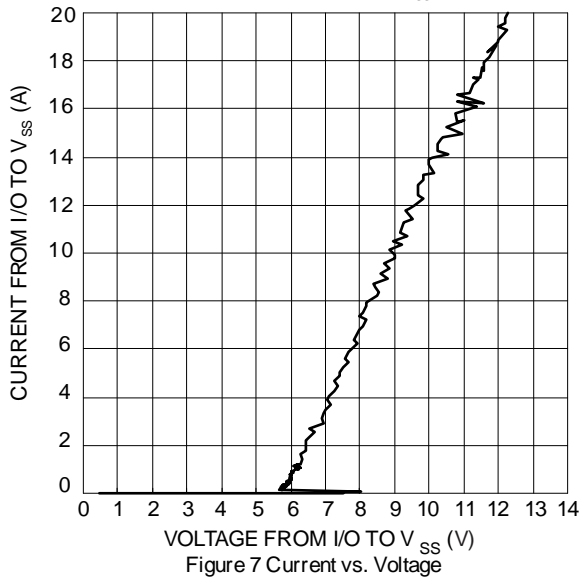
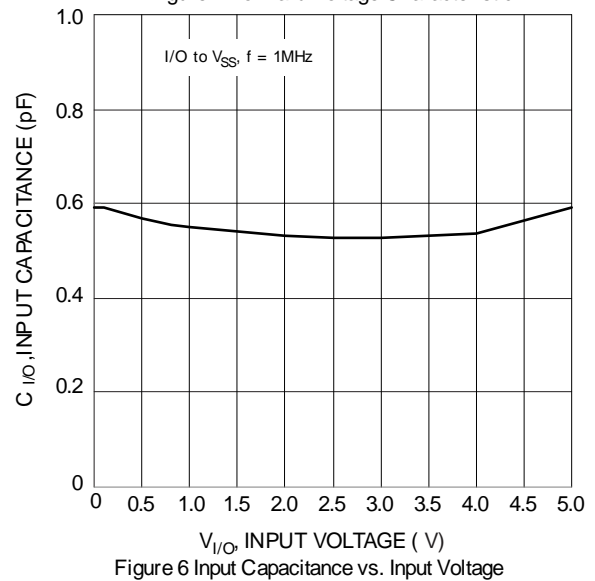
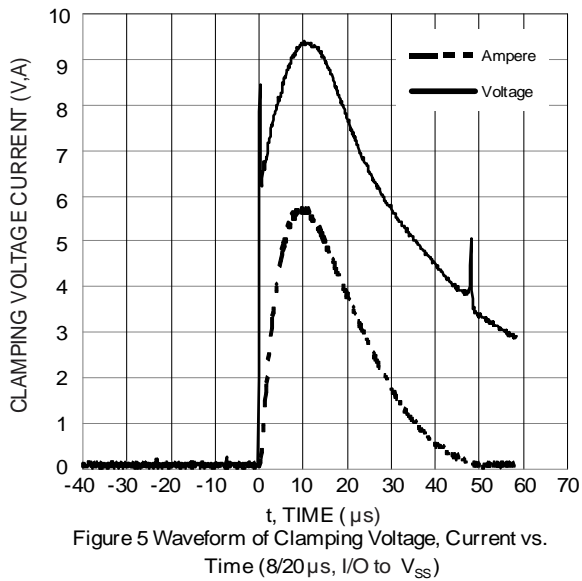
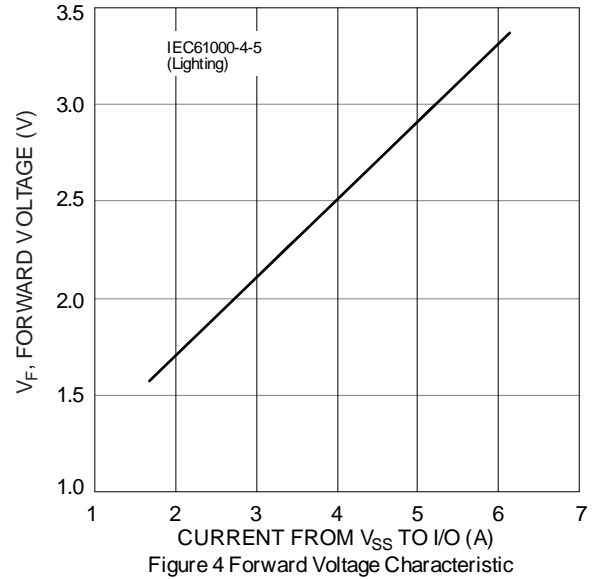
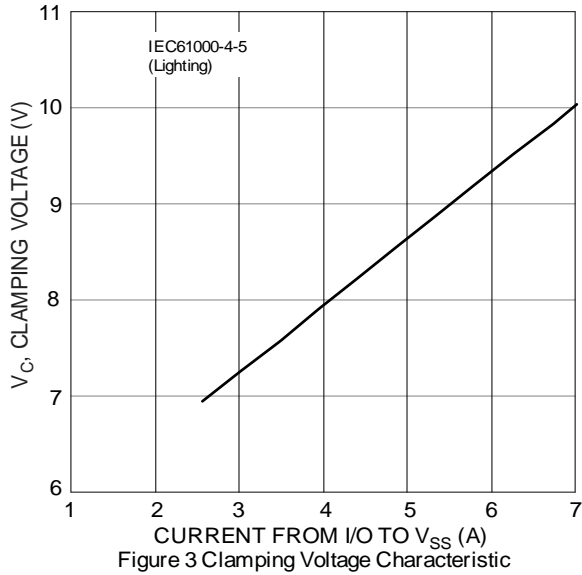
Characteristic	Symbol	Min	Typ	Max	Unit	Test Conditions
Reverse Working Voltage	V _{RWM}	—	—	3.3	V	I _R =1mA, , I/O to V _{SS}
Reverse Current	I _R	—	—	0.5	μA	V _R = 3.3V, I/O to V _{SS}
Reverse Breakdown Voltage	V _{BR}	6	—	—	V	I _R = 1mA, I/O to V _{SS}
Forward Clamping Voltage	V _F	-1.0	-0.85	—	V	I _F = -15mA, I/O to V _{SS}
Reverse Clamping Voltage (Note 6)	V _C	—	9	11	V	I _{PP} = 5.5A, I/O to V _{SS} , 8/20μs
Trigger Voltage	V _{TRIG}	—	—	9.5	V	—
ESD Clamping Voltage	V _{ESD}	—	8.8	—	V	TLP, 10A, tp = 100 ns, I/O to V _{SS}
Dynamic Reverse Resistance	R _{DIF-R}	—	0.3	—	Ω	TLP, 10A, tp = 100 ns, I/O to V _{SS}
Dynamic Forward Resistance	R _{DIF-F}	—	0.25	—	Ω	TLP, 10A, tp = 100 ns, V _{SS} to I/O
Channel Input Capacitance (Note7)	C _{I/O}	—	0.55	0.65	pF	V _{I/O} = 2.5V, V _{SS} = 0V, f = 1MHz
Delta C _{I/O}	C _{I/OMAX} -C _{I/OMIN}	—	0.04	—	pF	C _{I/OMAX} -C _{I/OMIN}

Notes: 5. Device mounted on FR-4 PCB pad layout (2oz copper) as shown on Diodes, Inc. suggested pad layout AP02001, which can be found on our website at <http://www.diodes.com>.

6. Clamping voltage value is based on an 8x20μs peak pulse current (I_{PP}) waveform.

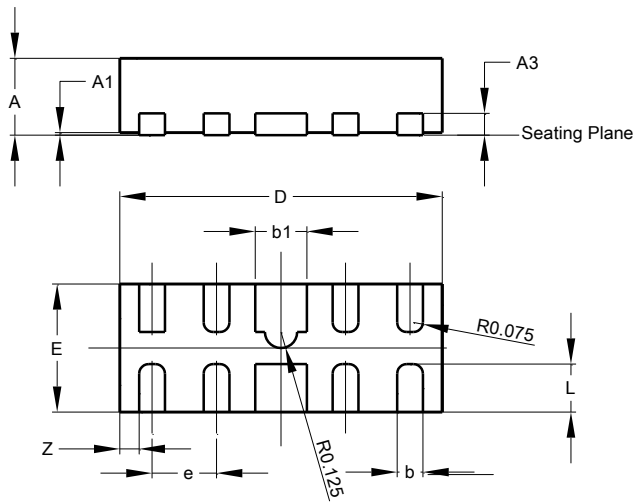
7. C_{I/O1}=C_{PIN1}+C_{PIN10}, C_{I/O2}=C_{PIN2}+C_{PIN9}, C_{I/O3}=C_{PIN4}+C_{PIN7}, C_{I/O4}=C_{PIN5}+C_{PIN6}.





Package Outline Dimensions

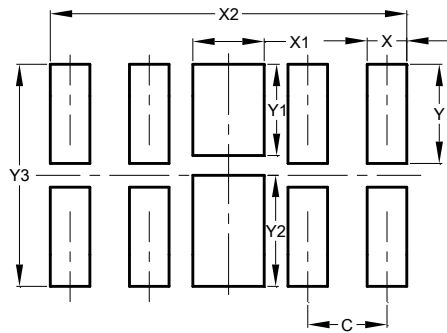
Please see AP02001 at http://www.diodes.com/_files/datasheets/ap02001.pdf for the latest version.



U-DFN2510-10			
Dim	Min	Max	Typ
A	0.545	0.605	0.575
A1	0	0.05	0.03
A3	-	-	0.13
b	0.15	0.25	0.20
b1	0.35	0.45	0.40
D	2.450	2.575	2.500
e	-	-	0.50
E	0.950	1.075	1.000
L	0.325	0.425	0.375
Z	-	-	0.150
All Dimensions in mm			

Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/_files/datasheets/ap02001.pdf for the latest version.



Dimensions	Value (in mm)
C	0.500
X	0.250
X1	0.450
X2	2.250
Y	0.625
Y1	0.575
Y2	0.700
Y3	1.400

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