TIP30C

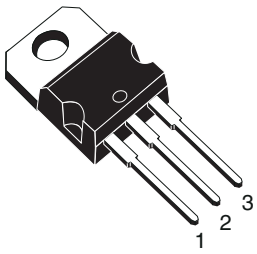
Low voltage PNP power transistor

Application

- General purpose switching and amplifier

Description

The device is manufactured in planar technology with “Base Island” layout. The resulting transistor shows exceptional high gain performance coupled with very low saturation voltage. The NPN type is TIP29C.



TO-220

Figure 1. Internal schematic diagram

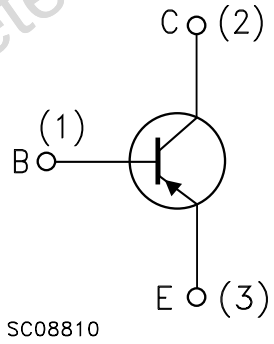


Table 1. Device summary

Order code	Marking	Package	Packaging
TIP30C	TIP30C	TO-220	Tube

1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-base voltage (I_E = 0)	-100	V
V_{CEO}	Collector-emitter voltage (I_B = 0)	-100	V
V_{EBO}	Emitte-base voltage (I_C = 0)	-5	V
I_C	Collector current	-1	A
I_{CM}	Collector peak current (t_P < 5ms)	-3	A
I_B	Base current	-0.4	A
P_{TOT}	Total dissipation at T_{case} = 25°C T_{amb} = 25°C	30 2	W W
T_{stg}	Storage temperature	-65 to 150	°C
T_J	Max. operating junction temperature	150	°C

2 Electrical characteristics

(T_{case} = 25°C; unless otherwise specified)

Table 3. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CEO}	Collector cut-off current (I_B = 0)	V_{CE} = -60 V			-0.3	mA
I_{CES}	Collector cut-off current (V_{BE} = 0)	V_{CE} =-100 V			-0.2	mA
I_{EBO}	Emitter cut-off current (I_C = 0)	V_{EB} = -5 V			-1	mA
$V_{CEO(sus)}$ (1)	Collector-emitter sustaining voltage (I_B = 0)	I_C = -30 mA	-100			V
$V_{CE(sat)}$ (1)	Collector-emitter saturation voltage	I_C = -1 A I_B = -125 mA			-0.7	V
$V_{BE(on)}$ (1)	Base-emitter voltage	I_C = -1 A V_{CE} = -4 V			-1.3	V
h_{FE} (1)	DC current gain	I_C = -200 mA V_{CE} = -4V I_C = -1 A V_{CE} = -4V	40 15		 75	

1. Pulsed duration = 300 ms, duty cycle ≥1.5%.

2.1 Typical characteristic (curves)

Figure 2. DC current gain

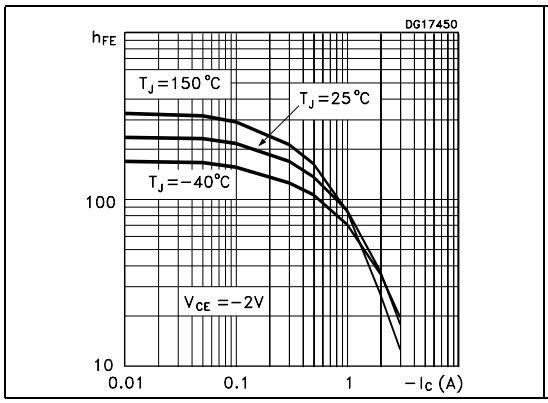


Figure 3. DC current gain

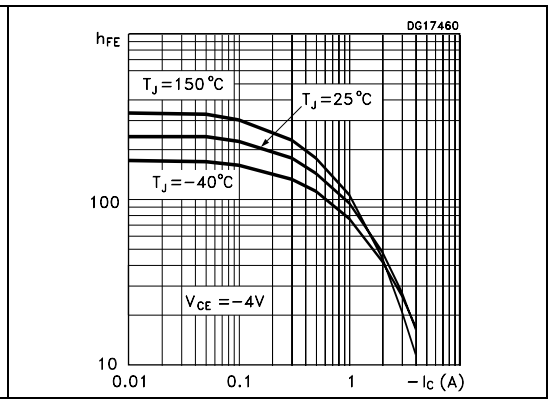


Figure 4. Collector-emitter saturation voltage

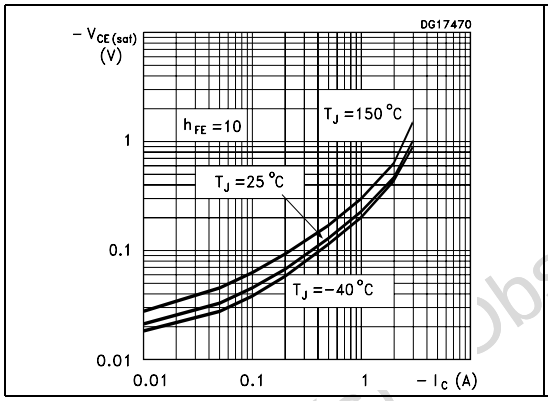


Figure 5. Base-emitter saturation voltage

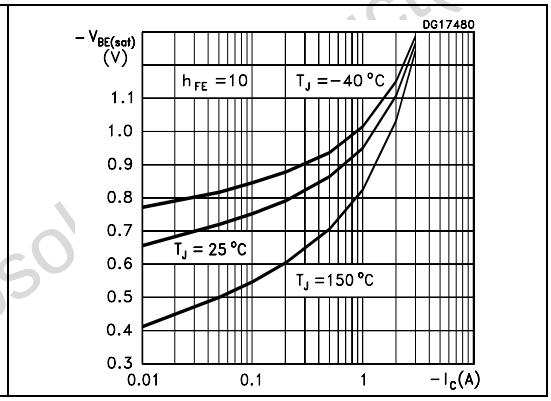


Figure 6. Resistive load switching time

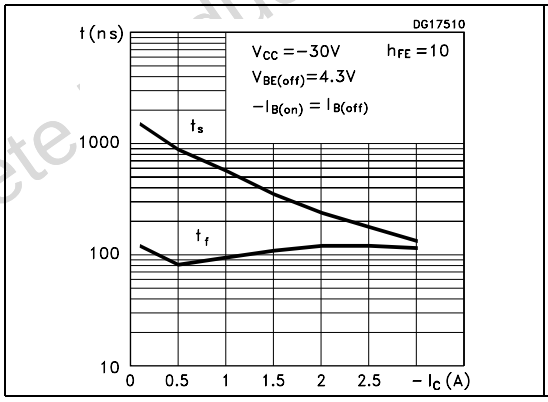


Figure 7. Resistive load switching time

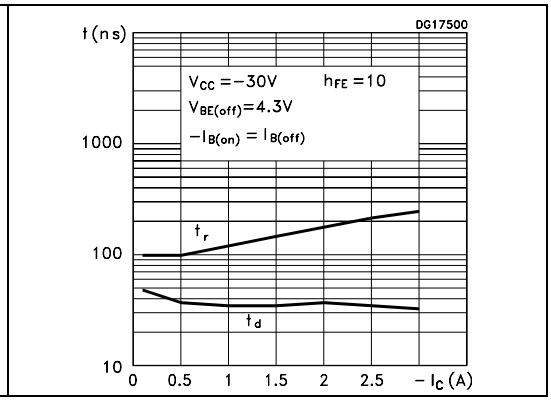
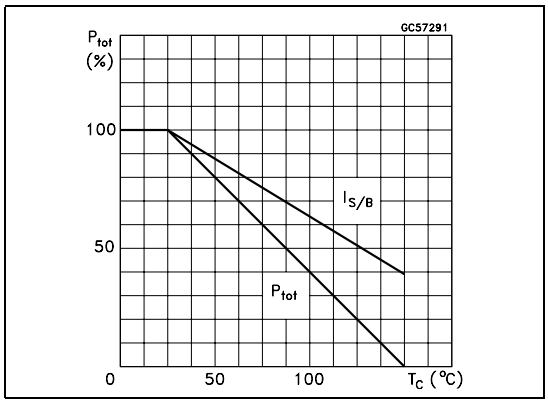
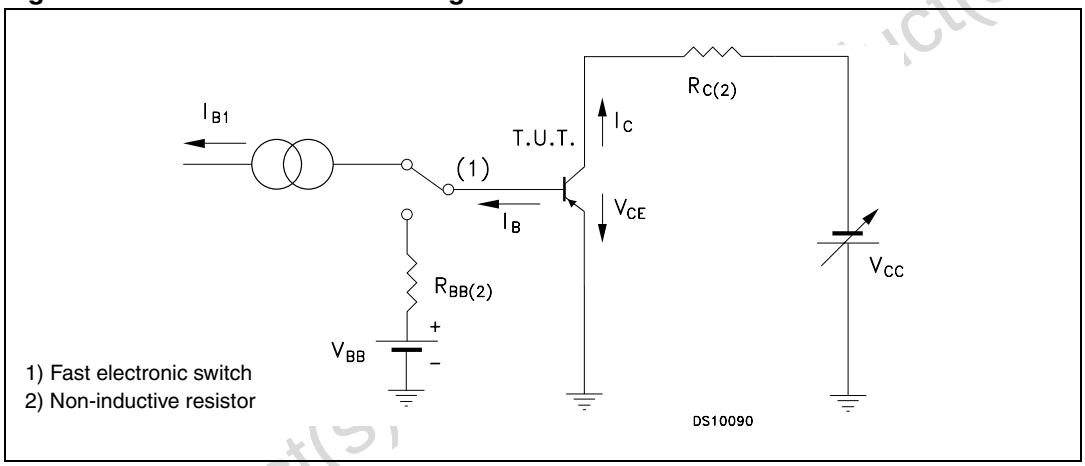


Figure 8. Derating curve



2.2 Test circuits

Figure 9. Resistive load switching test circuit

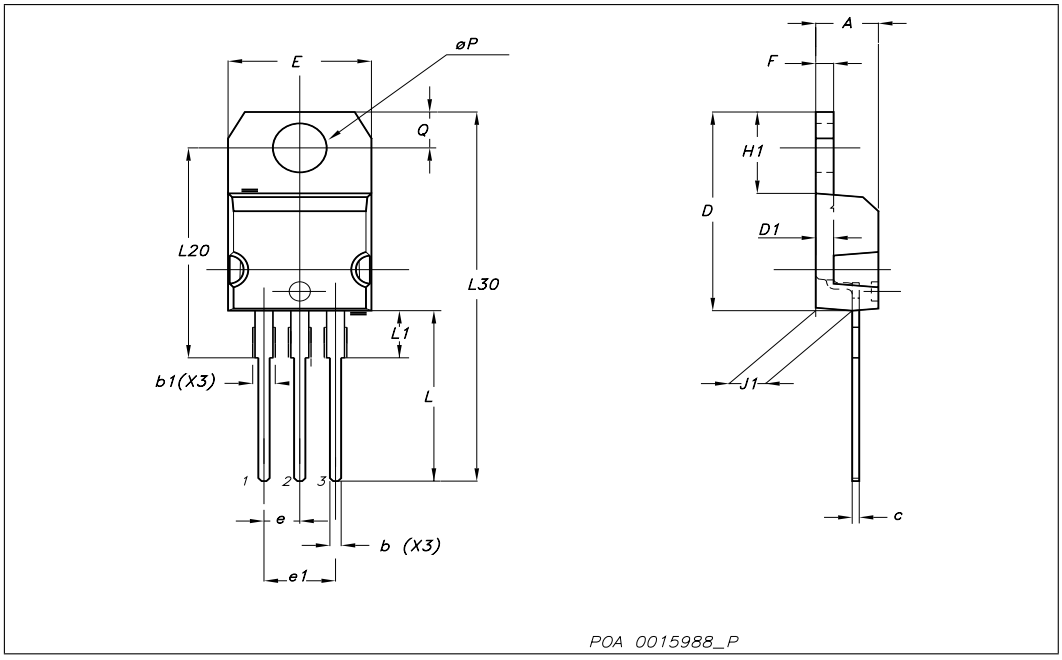


3 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TO-220 mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.6		0.62
D1		1.27			0.050	
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.051
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
∅P	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



4 Revision history

Table 4. Document revision history

Date	Revision	Changes
11-Oct-2007	1	Initial release

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