

MC10124

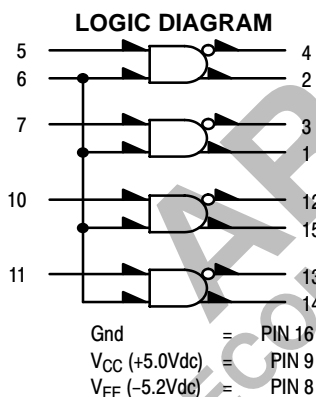
Quad TTL to MECL Translator

The MC10124 is a quad translator for interfacing data and control signals between a saturated logic section and the MECL section of digital systems. The MC10124 has TTL compatible inputs, and MECL complementary open-emitter outputs that allow use as an inverting/ non-inverting translator or as a differential line driver. When the common strobe input is at the low logic level, it forces all true outputs to a MECL low logic state and all inverting outputs to a MECL high logic state.

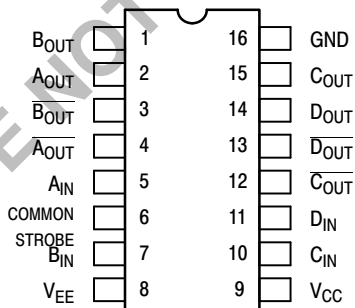
Power supply requirements are ground, +5.0 Volts, and -5.2 Volts. Propagation delay of the MC10124 is typically 3.5 ns. The dc levels are standard or Schottky TTL in, MECL 10,000 out.

An advantage of this device is that TTL level information can be transmitted differentially, via balanced twisted pair lines, to the MECL equipment, where the signal can be received by the MC10115 or MC10116 differential line receivers. The MC10124 is useful in computers, instrumentation, peripheral controllers, test equipment, and digital communications systems.

- $P_D = 380 \text{ mW typ/pkg (No Load)}$
- $t_{pd} = 3.5 \text{ ns typ (+ 1.5 Vdc in to 50% out)}$
- $t_r, t_f = 2.5 \text{ ns typ (20%–80%)}$



DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-Line Package.

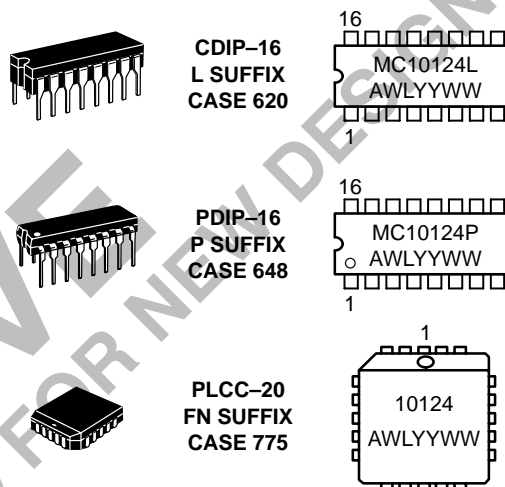
For PLCC pin assignment, see the Pin Conversion Tables on page 18 of the ON Semiconductor MECL Data Book (DL122/D).



ON Semiconductor

<http://onsemi.com>

MARKING DIAGRAMS



A = Assembly Location
 WL = Wafer Lot
 YY = Year
 WW = Work Week

ORDERING INFORMATION

| Device | Package | Shipping |
|-----------|---------|-----------------|
| MC10124L | CDIP-16 | 25 Units / Rail |
| MC10124P | PDIP-16 | 25 Units / Rail |
| MC10124FN | PLCC-20 | 46 Units / Rail |

ELECTRICAL CHARACTERISTICS

| Characteristic | Symbol | Pin Under Test | Test Limits | | | | | | | Unit |
|---|-------------------|----------------|------------------|------------------|------------------|-----|------------------|------------------|------------------|------|
| | | | −30°C | | +25°C | | | +85°C | | |
| | | | Min | Max | Min | Typ | Max | Min | Max | |
| Negative Power Supply Drain Current | I _E | 8 | | 72 | | | 66 | | 72 | mAdc |
| Positive Power Supply Drain Current | I _{CCH} | 9 | | 16 | | | 16 | | 18 | mAdc |
| | I _{CCL} | 9 | | 25 | | | 25 | | 25 | mAdc |
| Reverse Current | I _R | 6 7 | | 200 50 | | | 200 50 | | 200 50 | μAdc |
| Forward Current | I _F | 6 7 | | −12.8 −3.2 | | | −12.8 −3.2 | | −12.8 −3.2 | mAdc |
| Input Breakdown Voltage | BV _{in} | 6 7 | 5.5 5.5 | | 5.5 5.5 | | | 5.5 5.5 | | Vdc |
| Clamp Input Voltage | V _I | 6 7 | | −1.5 −1.5 | | | −1.5 −1.5 | | −1.5 −1.5 | Vdc |
| High Output Voltage | V _{OH} | 1 3 | −1.060 −1.060 | −0.890 −0.890 | −0.960 −0.960 | | −0.810 −0.810 | −0.890 −0.890 | −0.700 −0.700 | Vdc |
| Low Output Voltage | V _{OL} | 1 3 | −1.890 −1.890 | −1.675 −1.675 | −1.850 −1.850 | | −1.650 −1.650 | −1.825 −1.825 | −1.615 −1.615 | Vdc |
| High Threshold Voltage | V _{OHA} | 1 3 | −1.080 −1.080 | | −0.980 −0.980 | | | −0.910 −0.910 | | Vdc |
| Low Threshold Voltage | V _{OLA} | 1 3 | | −1.655 −1.655 | | | −1.630 −1.630 | | −1.595 −1.595 | Vdc |
| Switching Times (50Ω Load) | | | | | | | | | | ns |
| Propagation Delay (+3.5Vdc to 50%) ¹ | t ₆₊₁₊ | 1 | 1.5 | 6.8 | 1.0 | 3.5 | 6.0 | 1.0 | 6.0 | |
| | t _{6−1−} | 1 | 1.0 | 6.0 | 1.0 | 3.5 | 6.0 | 1.5 | 6.8 | |
| | t ₇₊₁₊ | 1 | 1.5 | 6.8 | 1.0 | 3.5 | 6.0 | 1.0 | 6.0 | |
| | t _{7−1−} | 1 | 1.0 | 6.0 | 1.0 | 3.5 | 6.0 | 1.5 | 6.8 | |
| | t _{7+3−} | 3 | 1.5 | 6.8 | 1.0 | 3.5 | 6.0 | 1.0 | 6.0 | |
| | t _{7−3+} | 3 | 1.0 | 6.0 | 1.0 | 3.5 | 6.0 | 1.5 | 6.8 | |
| Rise Time (20 to 80%) | t ₁₊ | 1 | 1.0 | 4.2 | 1.1 | 2.5 | 3.9 | 1.1 | 4.3 | |
| Fall Time (20 to 80%) | t _{1−} | 1 | 1.0 | 4.2 | 1.1 | 2.5 | 3.9 | 1.1 | 4.3 | |

1. See switching time test circuit. Propagation delay for this circuit is specified from +1.5Vdc in to the 50% point on the output waveform. The +3.5Vdc is shown here because all logic and supply levels are shifted 2 volts positive.

ELECTRICAL CHARACTERISTICS (continued)

| @ Test Temperature | | | TEST VOLTAGE VALUES (Volts) | | | | | Gnd |
|--|-------------------|----------------|---|--------------------|-------------------|-------------------|----------------|----------------------|
| | | | V _{IH} | V _{ILmax} | V _{IHA'} | V _{ILA'} | V _F | |
| | | | -30°C | +4.0 | +0.40 | +2.00 | +1.10 | +0.40 |
| | | | +25°C | +4.0 | +0.40 | +1.80 | +1.10 | +0.40 |
| | | | +85°C | +4.0 | +0.40 | +1.80 | +0.90 | +0.40 |
| Characteristic | Symbol | Pin Under Test | TEST VOLTAGE APPLIED TO PINS LISTED BELOW | | | | | Gnd |
| | | | V _{IH} | V _{ILmax} | V _{IHA'} | V _{ILA'} | V _F | |
| Negative Power Supply Drain Current | I _E | 8 | | | | | | 16 |
| Positive Power Supply Drain Current | I _{CCH} | 9 | 5,6,7,10,11 | | | | | 16 |
| | I _{CCL} | 9 | | | | | | 5,6,7,10,11,16 |
| Reverse Current | I _R | 6 7 | | | | | 5,7,10,11 6 | 16 16 |
| Forward Current | I _F | 6 7 | 5,7,10,11 6 | | | | 6 7 | 16 16 |
| Input Breakdown Voltage | BV _{in} | 6 7 | | | | | | 5,7,10,11,16 6,16 |
| Clamp Input Voltage | V _I | 6 7 | | | | | | 16 16 |
| High Output Voltage | V _{OH} | 1 3 | 6,7 | 6,7 | | | | 16 16 |
| Low Output Voltage | V _{OL} | 1 3 | 6,7 | 6,7 | | | | 16 16 |
| High Threshold Voltage | V _{OHA} | 1 3 | 6 6 | | 7 | 7 | | 16 16 |
| Low Threshold Voltage | V _{OLA} | 1 3 | 6 6 | | 7 | 7 | | 16 16 |
| Switching Times (50Ω Load) | | | +6.0 V | Pulse In | Pulse Out | | | +2.0 V |
| Propagation Delay (+3.5Vdc to 50%) ¹ | t ₆₊₁₊ | 1 | 7 | 6 | 1 | | | 16 |
| | t ₆₋₁₋ | 1 | 7 | 6 | 1 | | | 16 |
| | t ₇₊₁₊ | 1 | 6 | 7 | 1 | | | 16 |
| | t ₇₋₁₋ | 1 | 6 | 7 | 1 | | | 16 |
| | t ₇₊₃₋ | 3 | 6 | 7 | 3 | | | 16 |
| | t ₇₋₃₊ | 3 | 6 | 7 | 3 | | | 16 |
| Rise Time (20 to 80%) | t ₁₊ | 1 | 6 | 7 | 1 | | | 16 |
| Fall Time (20 to 80%) | t ₁₋ | 1 | 6 | 7 | 1 | | | 16 |

1. See switching time test circuit. Propagation delay for this circuit is specified from +1.5Vdc in to the 50% point on the output waveform. The +3.5Vdc is shown here because all logic and supply levels are shifted 2 volts positive.

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ELECTRICAL CHARACTERISTICS (continued)

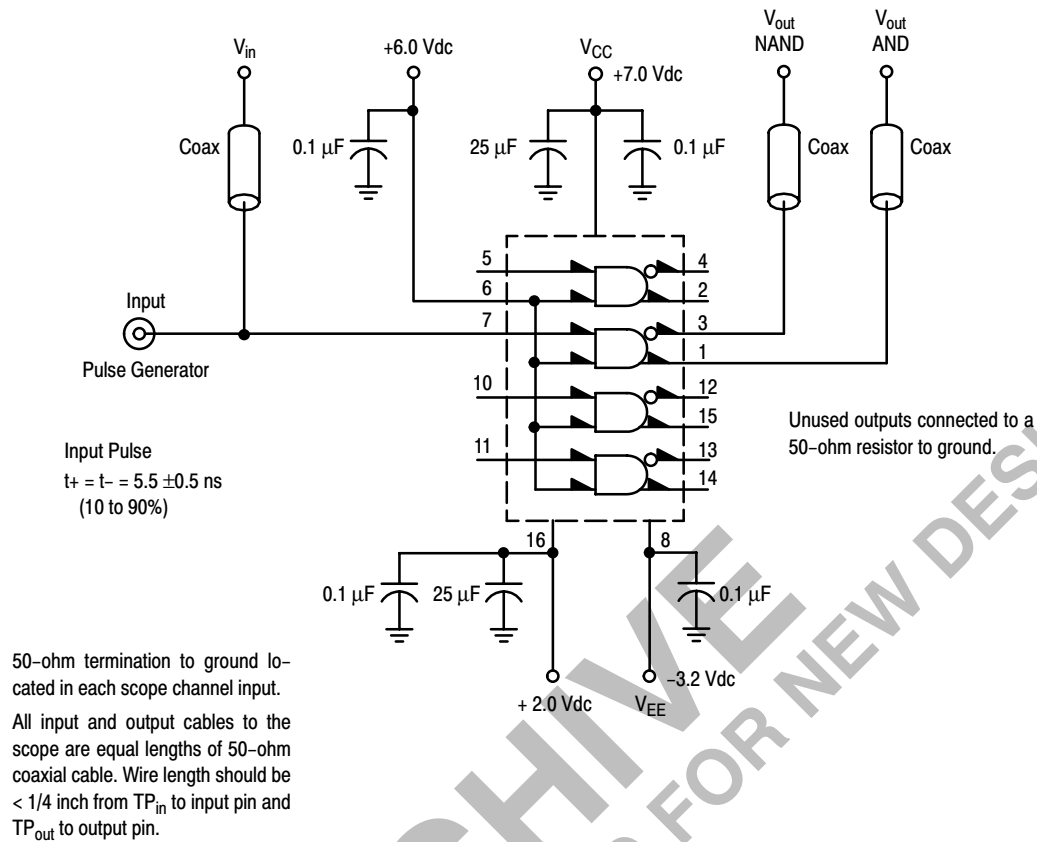
| @ Test Temperature | | | TEST VOLTAGE VALUES (Volts) | | | (mA) | | |
|--|-------------------|----------------|---|-----------------|-----------------|----------------|-----------------|----------------|
| | | | V _R | V _{CC} | V _{EE} | I _I | I _{in} | |
| | | | −30°C | +2.40 | +5.00 | −5.2 | −10 | +1.0 |
| | | | +25°C | +2.40 | +5.00 | −5.2 | −10 | +1.0 |
| | | | +85°C | +2.40 | +5.00 | −5.2 | −10 | +1.0 |
| Characteristic | Symbol | Pin Under Test | TEST VOLTAGE APPLIED TO PINS LISTED BELOW | | | | | Gnd |
| | | | V _R | V _{CC} | V _{EE} | I _I | I _{in} | |
| Negative Power Supply Drain Current | I _E | 8 | | 9 | 8 | | | 16 |
| Positive Power Supply Drain Current | I _{CCH} | 9 | | 9 | 8 | | | 16 |
| | I _{CCL} | 9 | | 9 | 8 | | | 5,6,7,10,11,16 |
| Reverse Current | I _R | 6 | 6 | 9 | 8 | | | 16 |
| | | 7 | 7 | 9 | 8 | | | 16 |
| Forward Current | I _F | 6 | | 9 | 8 | | | 16 |
| | | 7 | | 9 | 8 | | | 16 |
| Input Breakdown Voltage | BV _{in} | 6 | | 9 | 8 | | 6 | 5,7,10,11,16 |
| | | 7 | | 9 | 8 | | 7 | 6,16 |
| Clamp Input Voltage | V _I | 6 | | 9 | 8 | 6 | | 16 |
| | | 7 | | 9 | 8 | 7 | | 16 |
| High Output Voltage | V _{OH} | 1 | | 9 | 8 | | | 16 |
| | | 3 | | 9 | 8 | | | 16 |
| Low Output Voltage | V _{OL} | 1 | | 9 | 8 | | | 16 |
| | | 3 | | 9 | 8 | | | 16 |
| High Threshold Voltage | V _{OHA} | 1 | | 9 | 8 | | | 16 |
| | | 3 | | 9 | 8 | | | 16 |
| Low Threshold Voltage | V _{OLA} | 1 | | 9 | 8 | | | 16 |
| | | 3 | | 9 | 8 | | | 16 |
| Switching Times (50Ω Load) | | | | +7.0 V | −3.2 V | | | +2.0 V |
| Propagation Delay (+3.5Vdc to 50%) ¹ | t ₆₊₁₊ | 1 | | 9 | 8 | | | 16 |
| | t _{6−1−} | 1 | | 9 | 8 | | | 16 |
| | t ₇₊₁₊ | 1 | | 9 | 8 | | | 16 |
| | t _{7−1−} | 1 | | 9 | 8 | | | 16 |
| | t _{7+3−} | 3 | | 9 | 8 | | | 16 |
| | t _{7−3+} | 3 | | 9 | 8 | | | 16 |
| Rise Time (20 to 80%) | t ₁₊ | 1 | | 9 | 8 | | | 16 |
| Fall Time (20 to 80%) | t _{1−} | 1 | | 9 | 8 | | | 16 |

1. See switching time test circuit. Propagation delay for this circuit is specified from +1.5Vdc in to the 50% point on the output waveform. The +3.5Vdc is shown here because all logic and supply levels are shifted 2 volts positive.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

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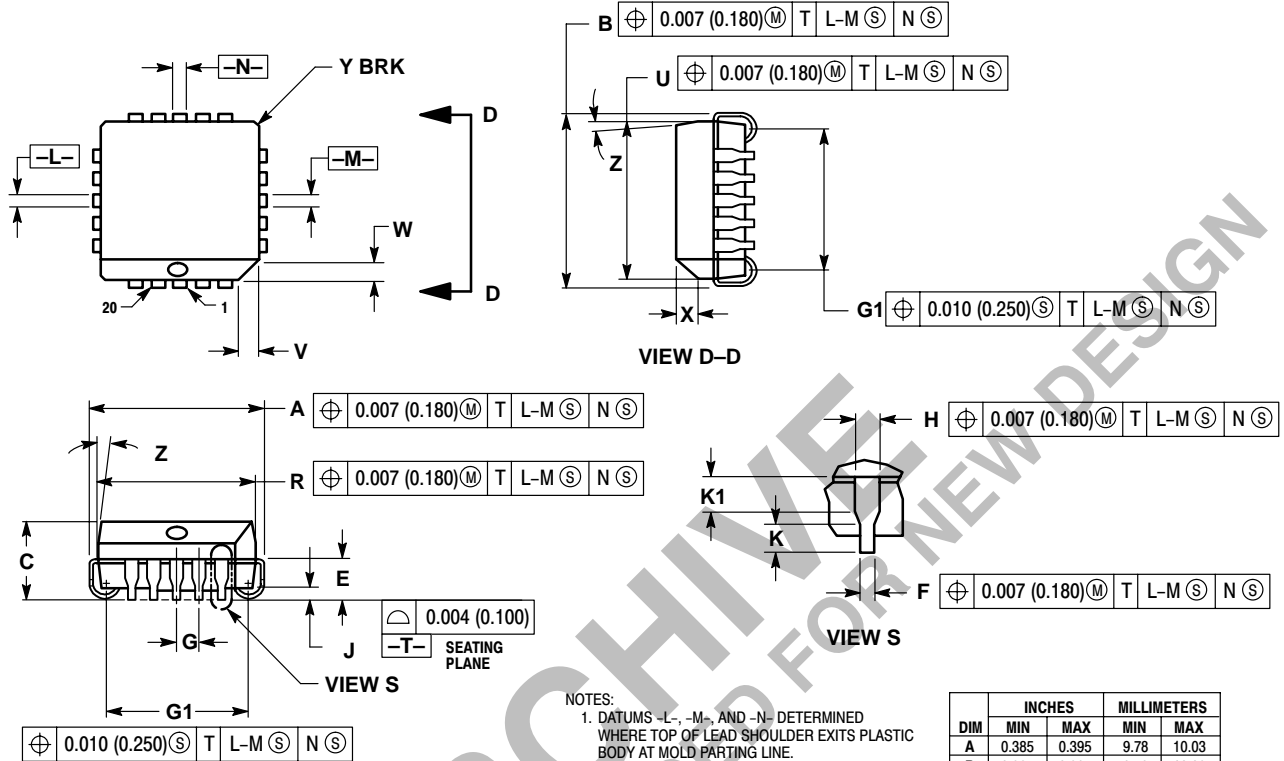
SWITCHING TIME TEST CIRCUIT



MC10124

PACKAGE DIMENSIONS

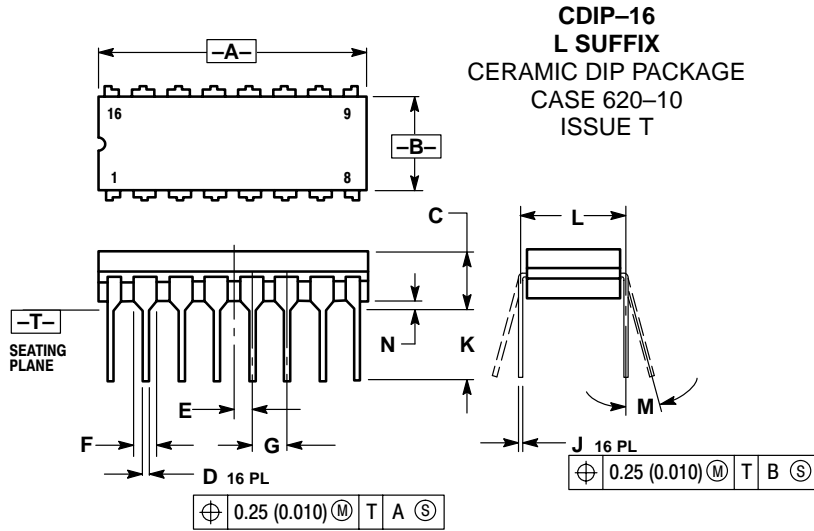
PLCC-20
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 775-02
ISSUE C



| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.385 | 0.395 | 9.78 | 10.03 |
| B | 0.385 | 0.395 | 9.78 | 10.03 |
| C | 0.165 | 0.180 | 4.20 | 4.57 |
| E | 0.090 | 0.110 | 2.29 | 2.79 |
| F | 0.013 | 0.019 | 0.33 | 0.48 |
| G | 0.050 BSC | | 1.27 BSC | |
| H | 0.026 | 0.032 | 0.66 | 0.81 |
| J | 0.020 | --- | 0.51 | --- |
| K | 0.025 | --- | 0.64 | --- |
| R | 0.350 | 0.356 | 8.89 | 9.04 |
| U | 0.350 | 0.356 | 8.89 | 9.04 |
| V | 0.042 | 0.048 | 1.07 | 1.21 |
| W | 0.042 | 0.048 | 1.07 | 1.21 |
| X | 0.042 | 0.056 | 1.07 | 1.42 |
| Y | --- | 0.020 | --- | 0.50 |
| Z | 2 ° | 10 ° | 2 ° | 10 ° |
| G1 | 0.310 | 0.330 | 7.88 | 8.38 |
| K1 | 0.040 | --- | 1.02 | --- |

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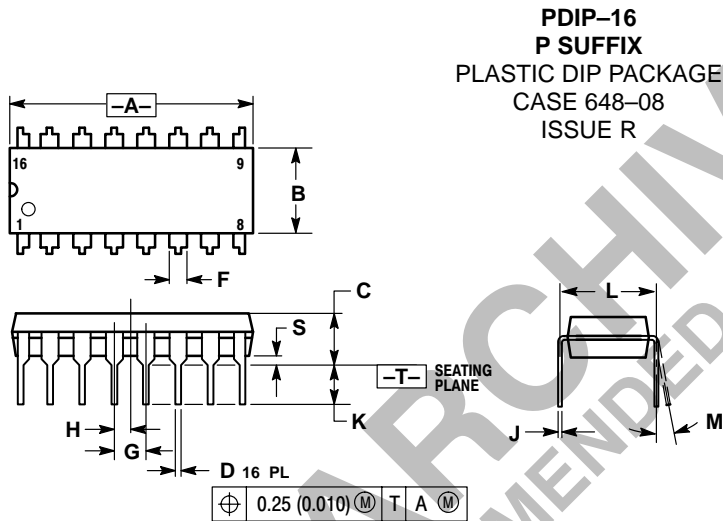
PACKAGE DIMENSIONS



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.750 | 0.785 | 19.05 | 19.93 |
| B | 0.240 | 0.295 | 6.10 | 7.49 |
| C | --- | 0.200 | --- | 5.08 |
| D | 0.015 | 0.020 | 0.39 | 0.50 |
| E | 0.050 BSC | | 1.27 BSC | |
| F | 0.055 | 0.065 | 1.40 | 1.65 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.125 | 0.170 | 3.18 | 4.31 |
| L | 0.300 BSC | | 7.62 BSC | |
| M | 0° | 15° | 0° | 15° |
| N | 0.020 | 0.040 | 0.51 | 1.01 |



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.740 | 0.770 | 18.80 | 19.55 |
| B | 0.250 | 0.270 | 6.35 | 6.85 |
| C | 0.145 | 0.175 | 3.69 | 4.44 |
| D | 0.015 | 0.021 | 0.39 | 0.53 |
| F | 0.040 | 0.70 | 1.02 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.050 BSC | | 1.27 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.130 | 2.80 | 3.30 |
| L | 0.295 | 0.305 | 7.50 | 7.74 |
| M | 0° | 10° | 0° | 10° |
| S | 0.020 | 0.040 | 0.51 | 1.01 |

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