

1. General description

Planar passivated four quadrant triac in a SOT223 surface-mountable plastic package intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance.

2. Features and benefits

- High blocking voltage capability
- High noise immunity suitable for noisy applications
- Planar passivated for voltage ruggedness and reliability
- Surface-mountable package
- Triggering in all four quadrants

3. Applications

- General purpose low power motor control
- General purpose switching and phase control

4. Quick reference data

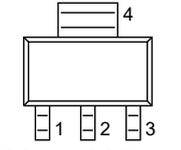
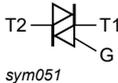
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	600	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{sp} \leq 108\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	-	1	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(\text{init})} = 25\text{ °C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	-	10	A
		full sine wave; $T_{j(\text{init})} = 25\text{ °C}$; $t_p = 16.7\text{ ms}$	-	-	11	A
T_j	junction temperature		-	-	125	°C
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ °C}$; Fig. 9	-	5	35	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ °C}$; Fig. 9	-	8	35	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ °C}$; Fig. 9	-	11	35	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G+; $T_j = 25\text{ °C}$; Fig. 9	-	30	70	mA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ °C}$; Fig. 11	-	5	15	mA
V_T	on-state voltage	$I_T = 2\text{ A}$; $T_j = 25\text{ °C}$; Fig. 12	-	1.2	1.5	V
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 402\text{ V}$; $T_j = 125\text{ °C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit	100	250	-	V/ μ s
dV_{com}/dt	rate of change of commutating voltage	$V_D = 400\text{ V}$; $T_j = 95\text{ °C}$; $dI_{com}/dt = 1.8\text{ A/ms}$; $I_T = 1\text{ A}$; gate open circuit	-	50	-	V/ μ s

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1	 <p>SC-73 (SOT223)</p>	 <p>sym051</p>
2	T2	main terminal 2		
3	G	gate		
4	T2	main terminal 2		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BT134W-600	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223

7. Marking

Table 4. Marking codes

Type number	Marking code
BT134W-600	BT134W 60

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	600	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{sp} \leq 108\text{ }^{\circ}\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	1	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	10	A
		full sine wave; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; $t_p = 16.7\text{ ms}$	-	11	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; SIN	-	0.5	A^2s
di_T/dt	rate of rise of on-state current	$I_G = 0.2\text{ A}$	-	50	$\text{A}/\mu\text{s}$
			-	50	$\text{A}/\mu\text{s}$
			-	50	$\text{A}/\mu\text{s}$
			-	10	$\text{A}/\mu\text{s}$
I_{GM}	peak gate current		-	2	A
P_{GM}	peak gate power		-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.5	W
T_{stg}	storage temperature		-40	150	$^{\circ}\text{C}$
T_j	junction temperature		-	125	$^{\circ}\text{C}$

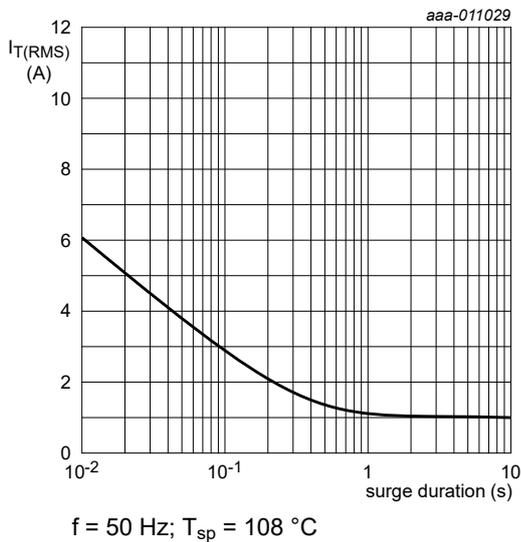


Fig. 1. RMS on-state current as a function of surge duration; maximum values

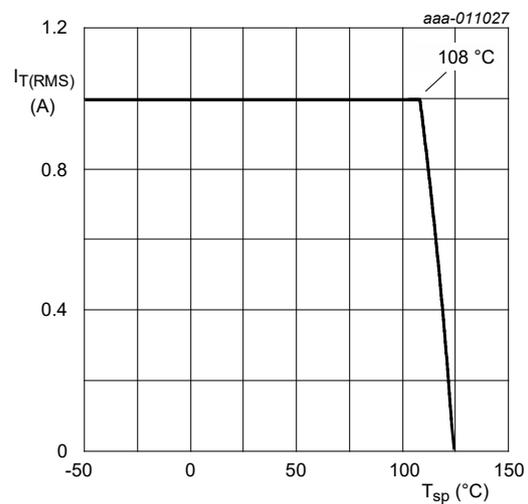


Fig. 2. RMS on-state current as a function of solder point temperature; maximum values

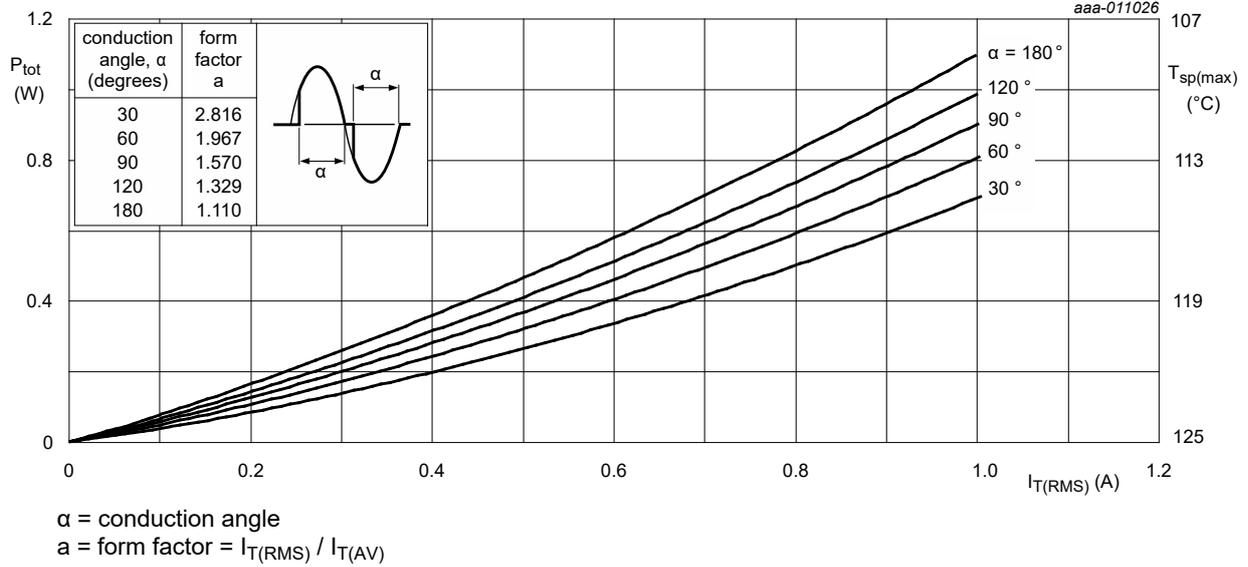


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

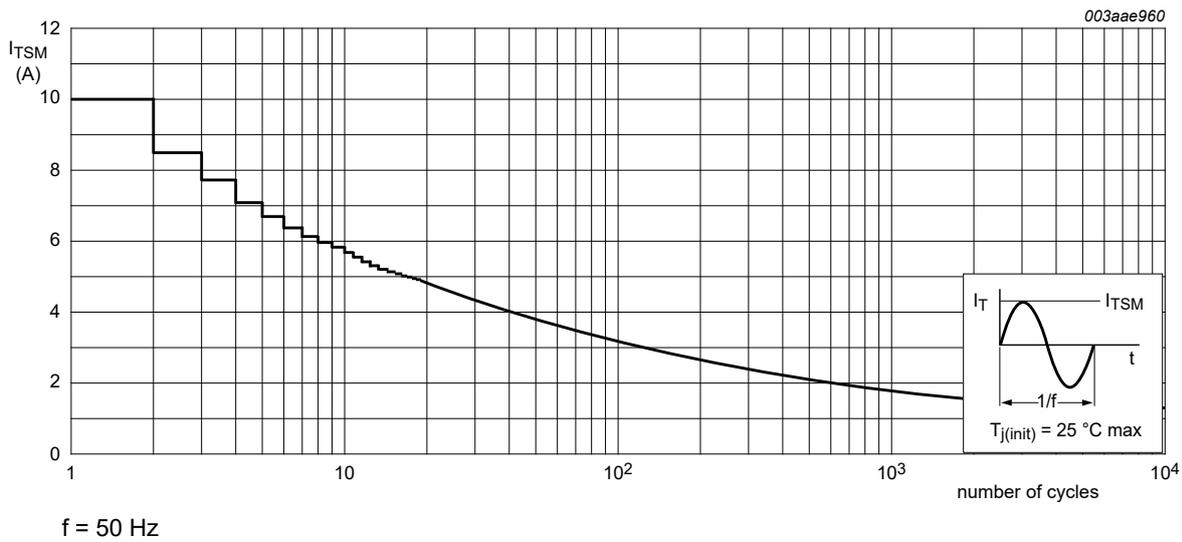
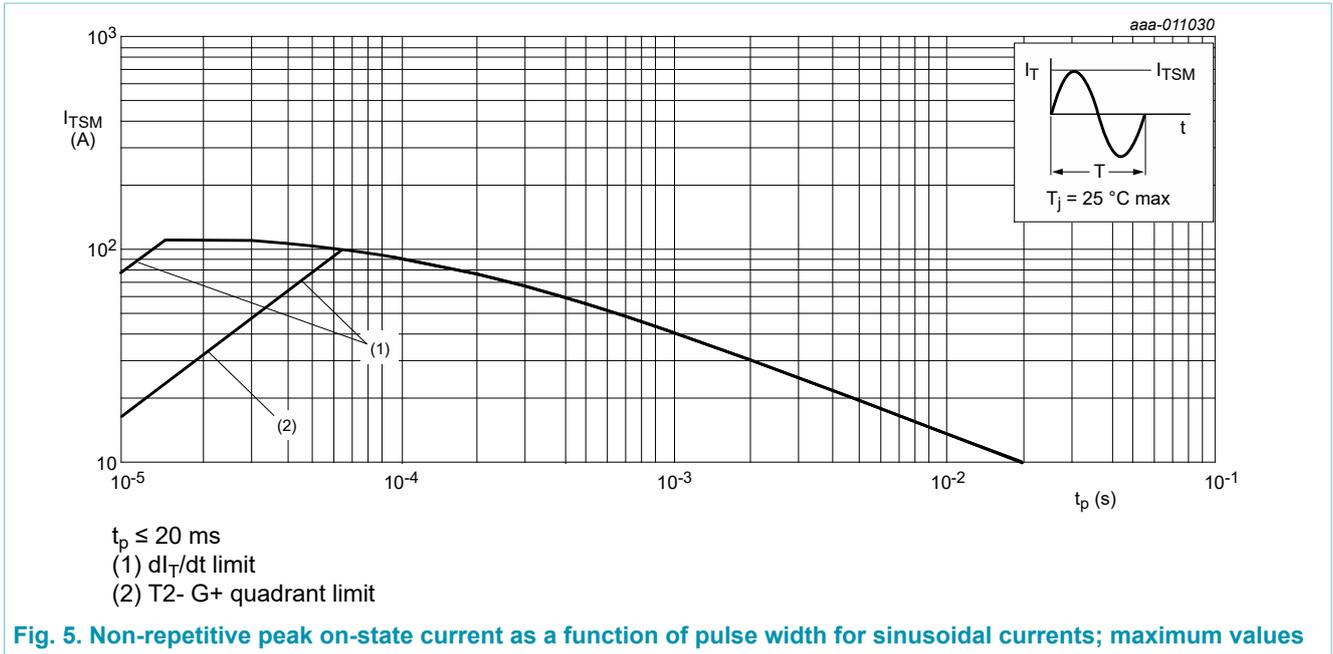


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	full cycle; Fig. 6	-	-	15	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	full cycle; printed circuit board mounted; minimum footprint; Fig. 7	-	156	-	K/W
		full cycle; printed circuit board mounted; pad area; Fig. 8	-	70	-	K/W

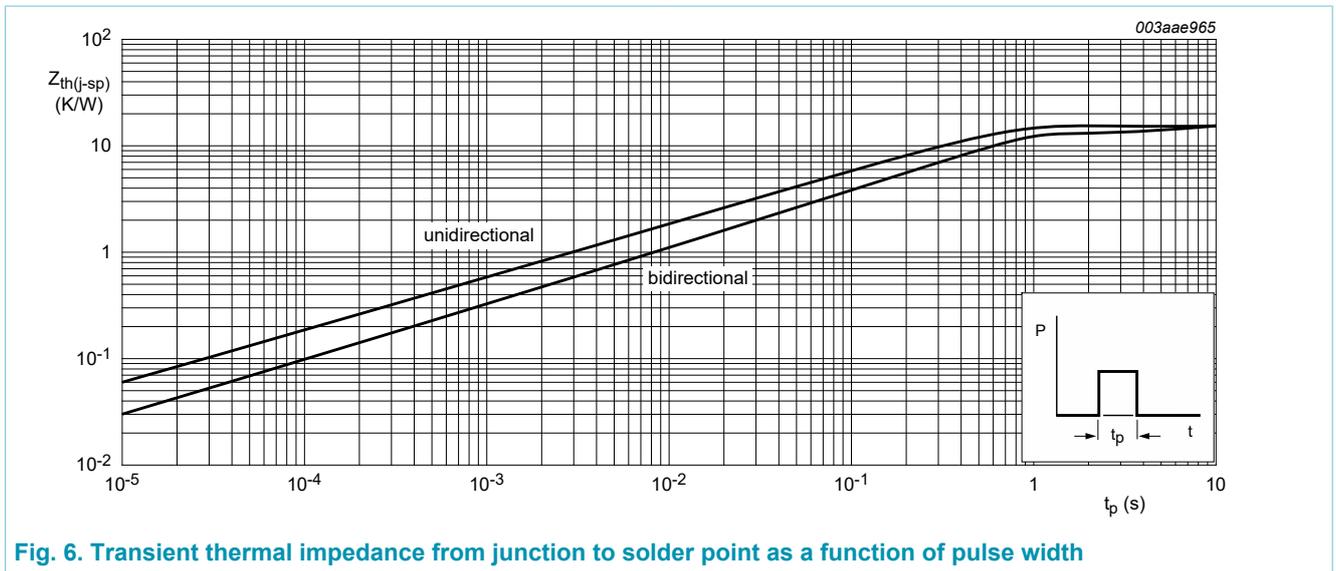
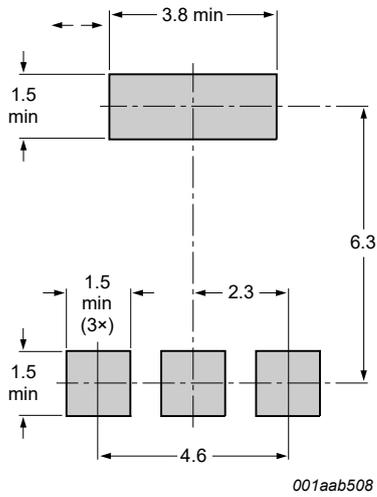
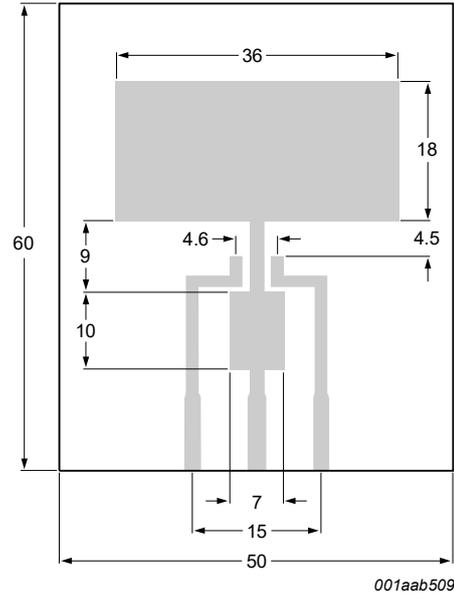


Fig. 6. Transient thermal impedance from junction to solder point as a function of pulse width



All dimensions are in mm

Fig. 7. Minimum footprint SOT223



All dimensions are in mm

Printed circuit board:

FR4 epoxy glass (1.6 mm thick), copper laminate (35 um thick)

Fig. 8. Printed circuit board pad area: SOT223

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9	-	5	35	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9	-	8	35	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9	-	11	35	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9	-	30	70	mA
I_L	latching current	$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 10	-	7	20	mA
		$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 10	-	16	30	mA
		$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 10	-	5	20	mA
		$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2- G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 10	-	7	30	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 11	-	5	15	mA
V_T	on-state voltage	$I_T = 2\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 12	-	1.2	1.5	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 13	-	0.7	1	V
		$V_D = 400\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 125\text{ }^\circ\text{C}$; Fig. 13	0.25	0.4	-	V
I_D	off-state current	$V_D = 600\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$	-	0.1	0.5	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 402\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit	100	250	-	V/ μs
dV_{com}/dt	rate of change of commutating voltage	$V_D = 400\text{ V}$; $T_j = 95\text{ }^\circ\text{C}$; $dI_{com}/dt = 1.8\text{ A/ms}$; $I_T = 1\text{ A}$; gate open circuit	-	50	-	V/ μs
t_{gt}	gate-controlled turn-on time	$I_{TM} = 1.5\text{ A}$; $V_D = 600\text{ V}$; $I_G = 0.1\text{ A}$; $dI_G/dt = 5\text{ A}/\mu\text{s}$	-	2	-	μs

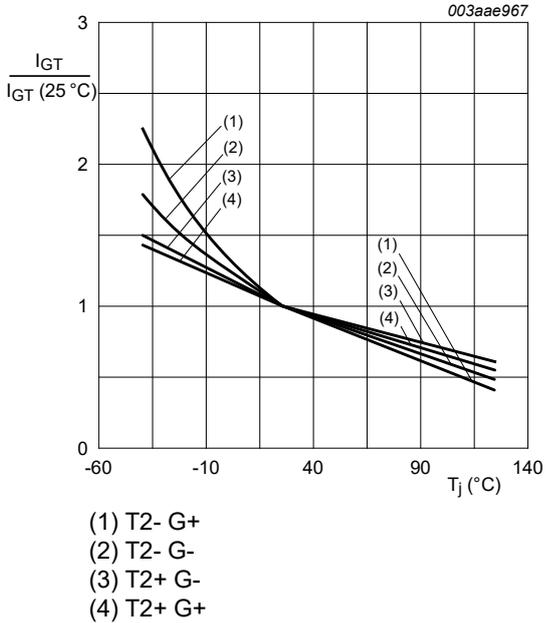


Fig. 9. Normalized gate trigger current as a function of junction temperature

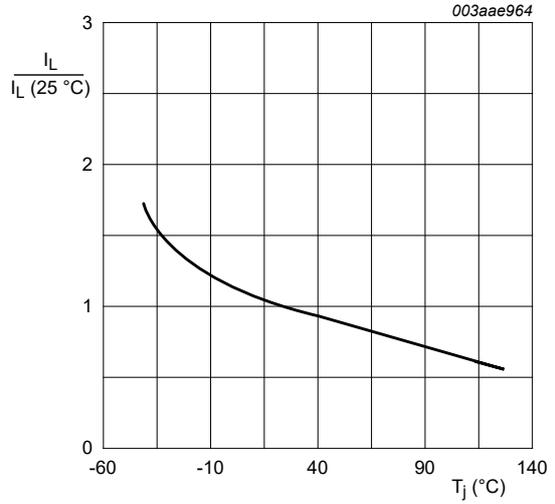


Fig. 10. Normalized latching current as a function of junction temperature

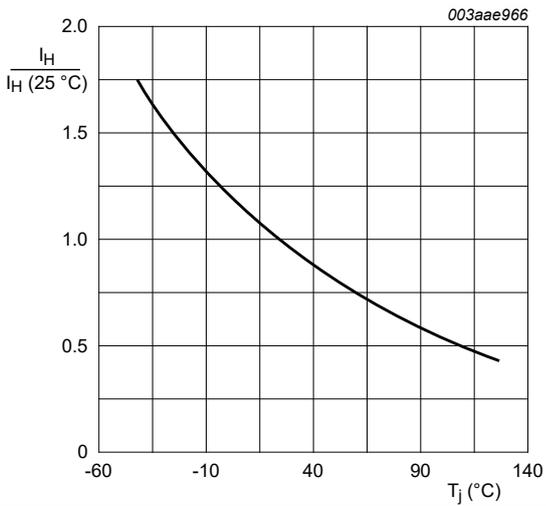


Fig. 11. Normalized holding current as a function of junction temperature

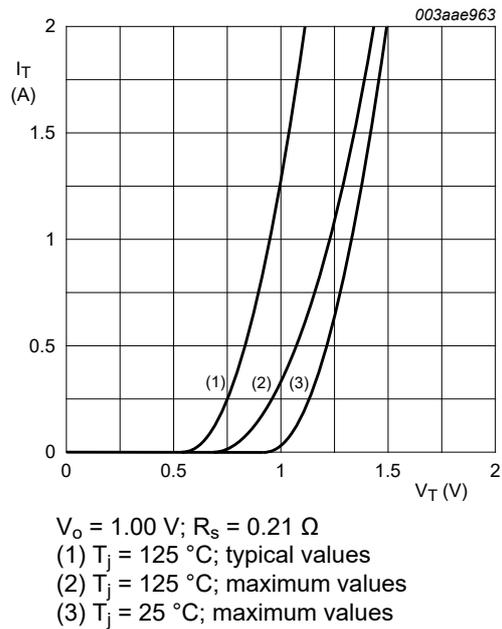


Fig. 12. On-state current as a function of on-state voltage

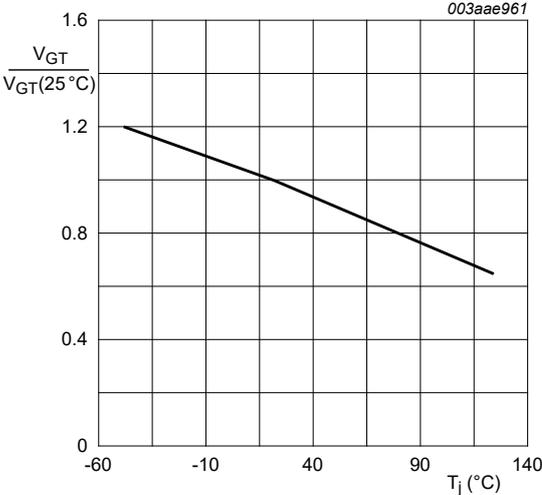


Fig. 13. Normalized gate trigger voltage as a function of junction temperature

11. Package outline

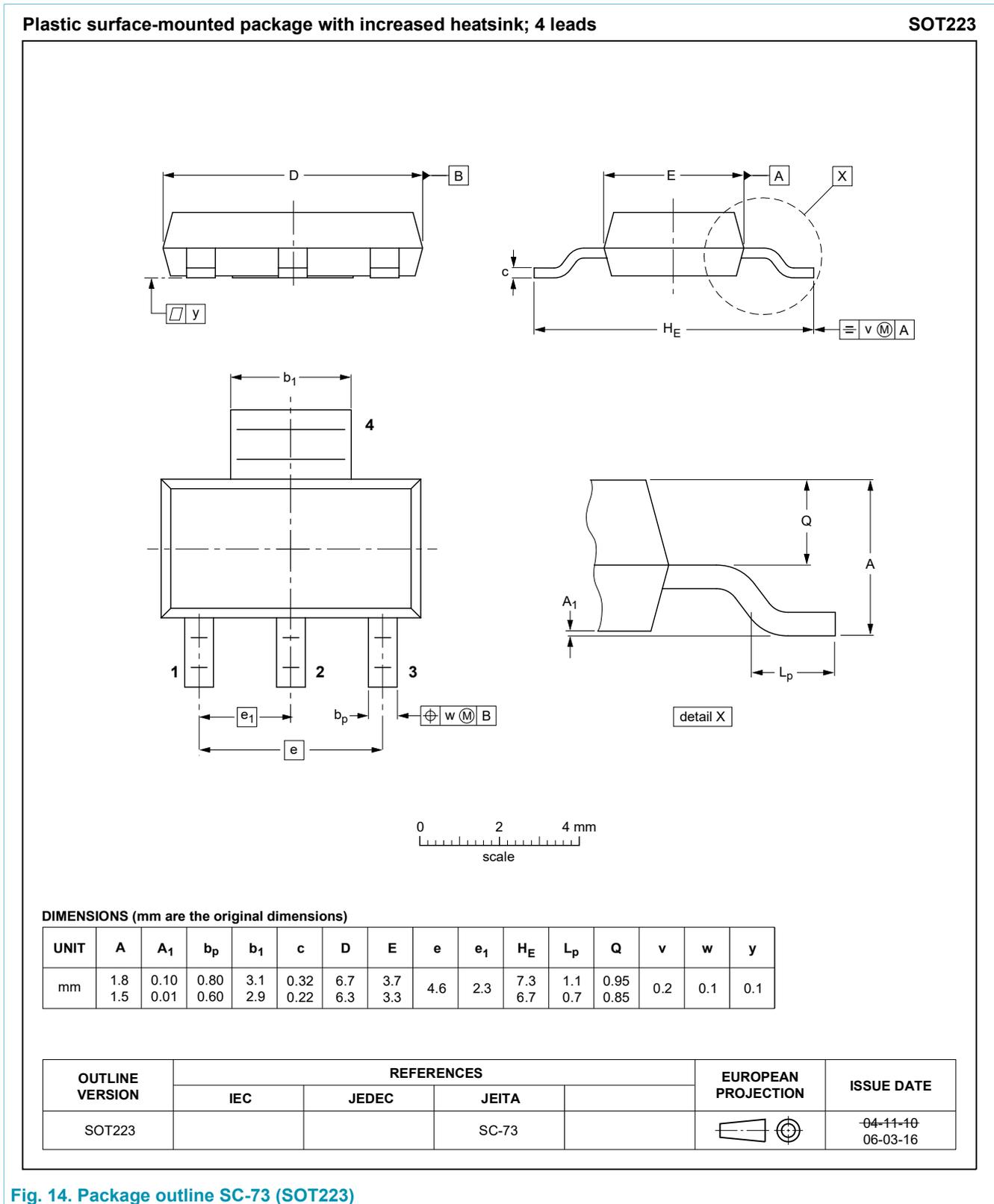


Fig. 14. Package outline SC-73 (SOT223)

12. Package outline (minimized)

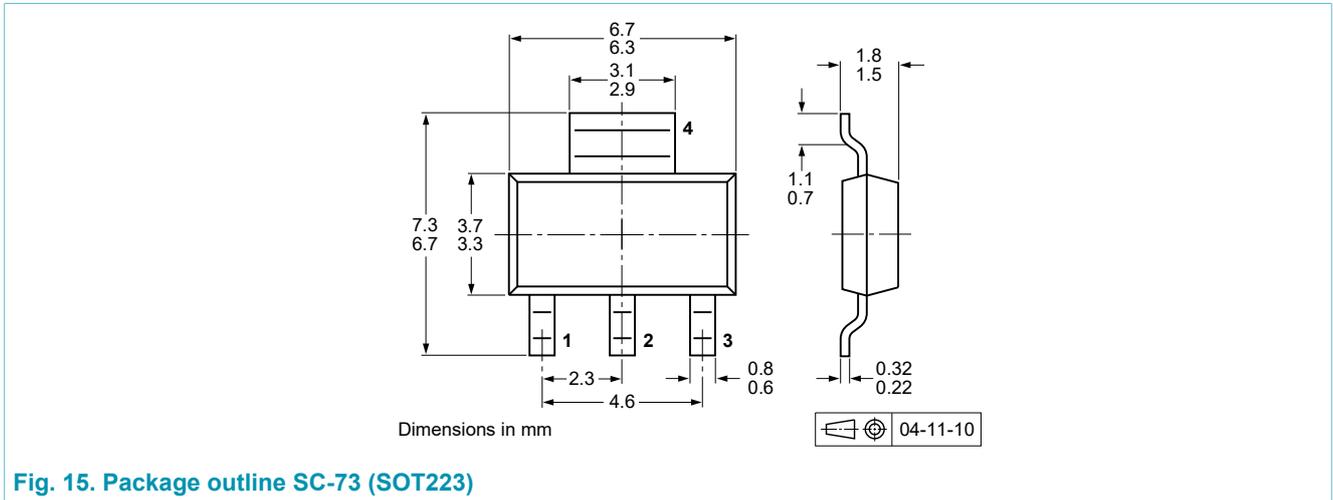


Fig. 15. Package outline SC-73 (SOT223)

13. Soldering

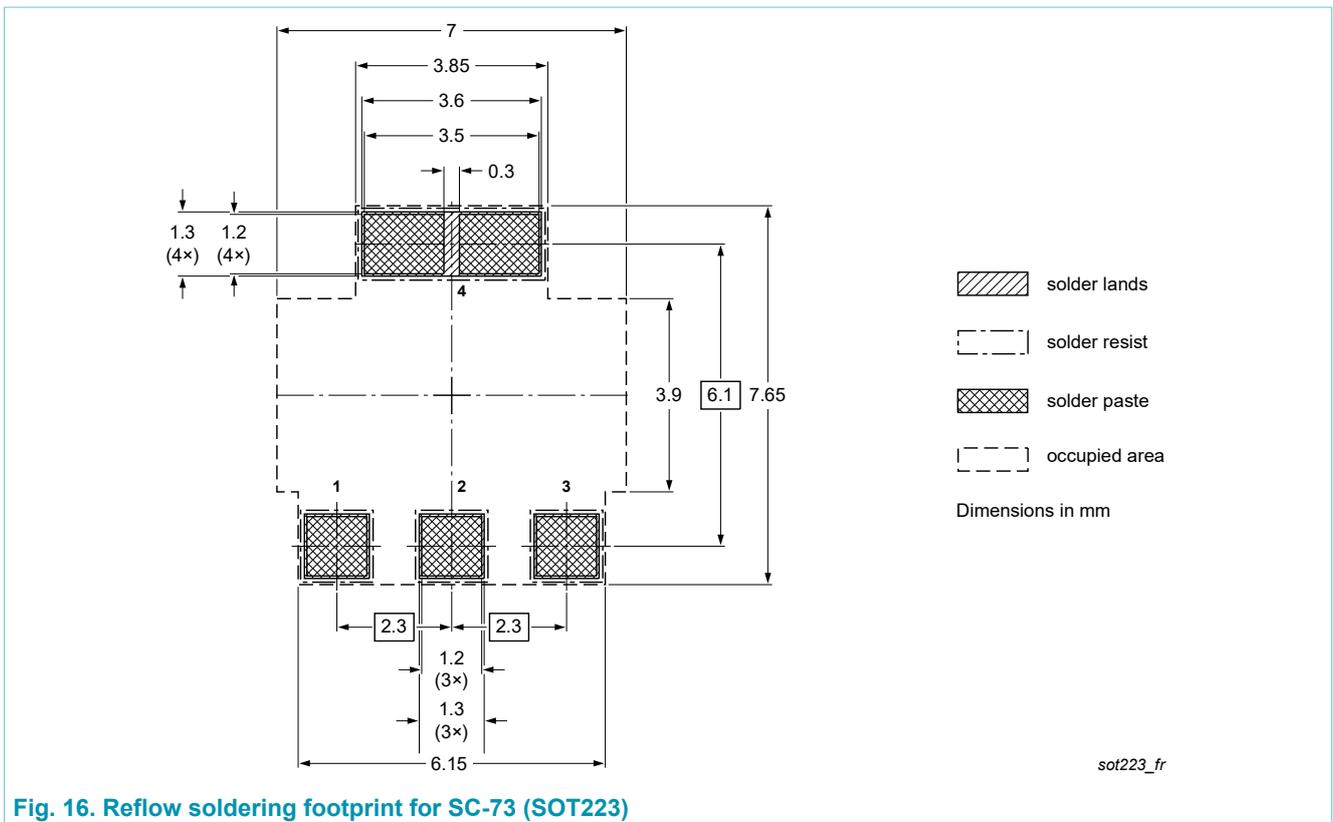


Fig. 16. Reflow soldering footprint for SC-73 (SOT223)

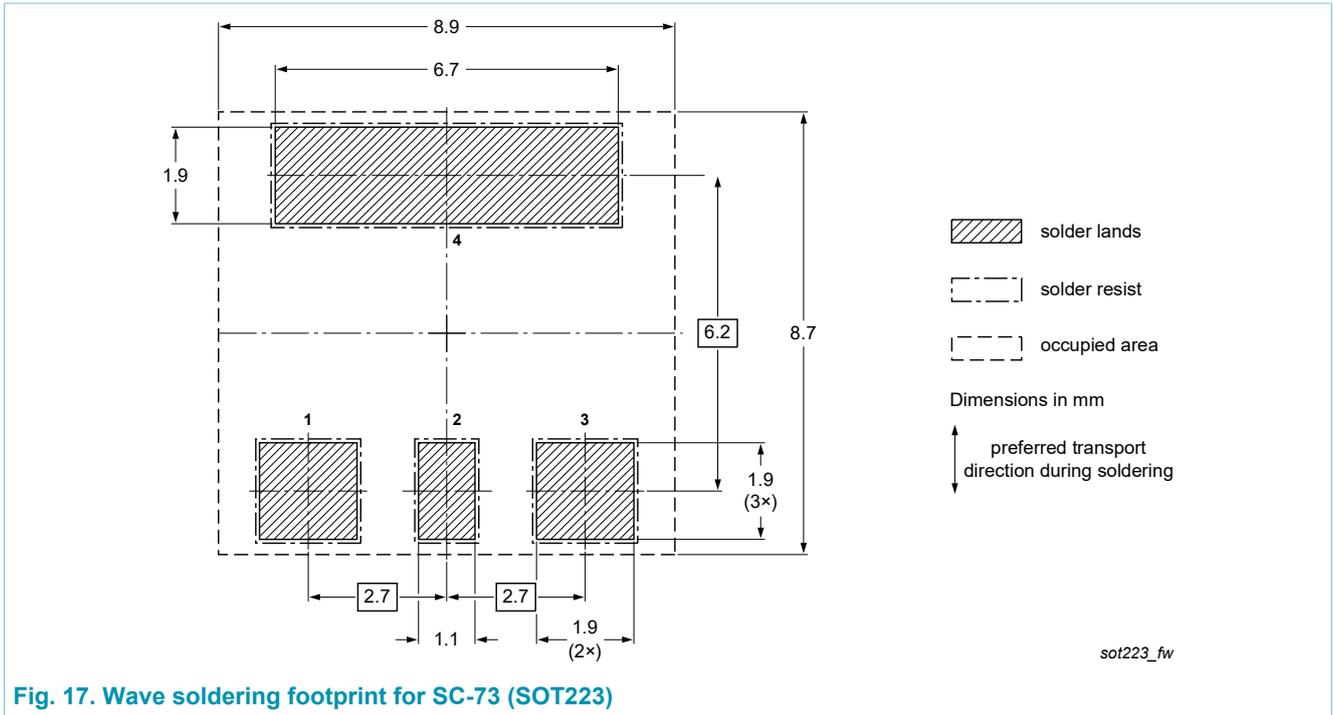


Fig. 17. Wave soldering footprint for SC-73 (SOT223)

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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15. Contents

1. General description.....	1
2. Features and benefits.....	1
3. Applications.....	1
4. Quick reference data.....	1
5. Pinning information.....	2
6. Ordering information.....	2
7. Marking.....	2
8. Limiting values.....	3
9. Thermal characteristics.....	6
10. Characteristics.....	8
11. Package outline.....	11
12. Package outline (minimized).....	12
13. Soldering.....	12
14. Legal information.....	14

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