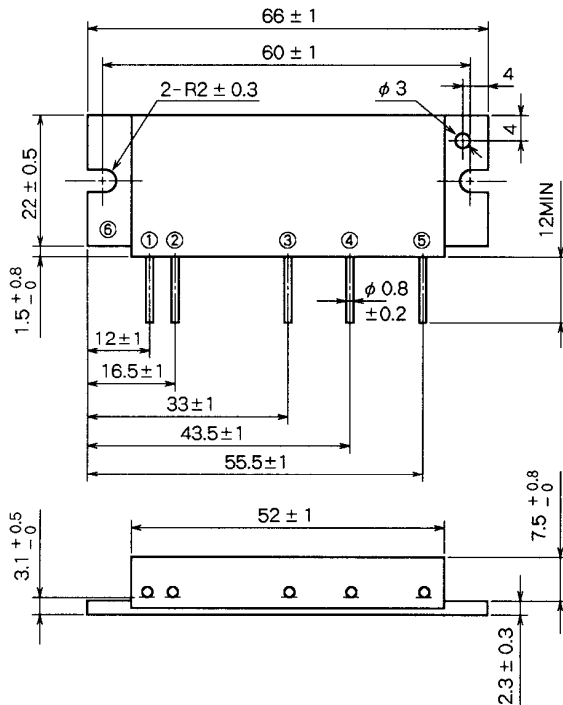
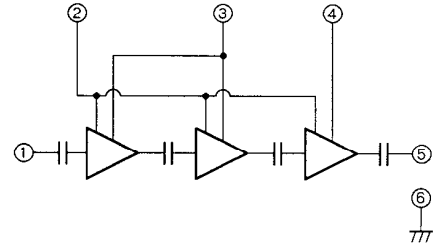


OUTLINE DRAWING

Dimensions in mm



BLOCK DIAGRAM



PIN :

- ① P_{in} : RF INPUT
- ② V_{BB} : BASE BIAS SUPPLY
- ③ V_{cc1} : 1st. DC SUPPLY
- ④ V_{cc2} : 2nd. DC SUPPLY
- ⑤ P_o : RF OUTPUT
- ⑥ GND : FIN

ABSOLUTE MAXIMUM RATINGS ($T_c = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{cc}	Supply voltage		17	V
V_{BB}	Base bias		10	V
I_{cc}	Total current		10	A
$P_{in(max)}$	Input power	$Z_G = Z_L = 50 \Omega$	0.5	W
$P_{o(max)}$	Output power	$Z_G = Z_L = 50 \Omega$	40	W
$T_{c(OP)}$	Operation case temperature		- 30 to 110	$^\circ\text{C}$
T_{stg}	Storage temperature		- 40 to 110	$^\circ\text{C}$

Note. Above parameters are guaranteed independently.

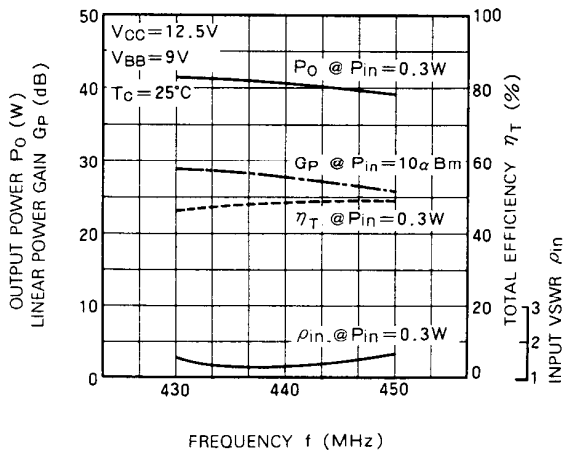
ELECTRICAL CHARACTERISTICS ($T_c = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test conditions	Limits		Unit
			Min	Max	
f	Frequency range		430	450	MHz
P_o	Output power	$P_{in} = 0.3\text{W}$	33		W
η_T	Total efficiency	$V_{cc} = 12.5\text{V}$	40		%
2fo	2nd. harmonic	$V_{BB} = 9\text{V}$		- 30	dBc
3fo	3rd. harmonic	$Z_G = Z_L = 50 \Omega$		- 30	dBc
ρ_{in}	Input VSWR			2.5	-
-	Load VSWR tolerance	$V_{cc} = 15.2\text{V}$, $V_{BB} = 9\text{V}$ $P_o = 30\text{W}$ (P_{in} : controlled) Load VSWR = 8.8 : 1 (All phase), $Z_G = 50 \Omega$	No degradation or destroy		-

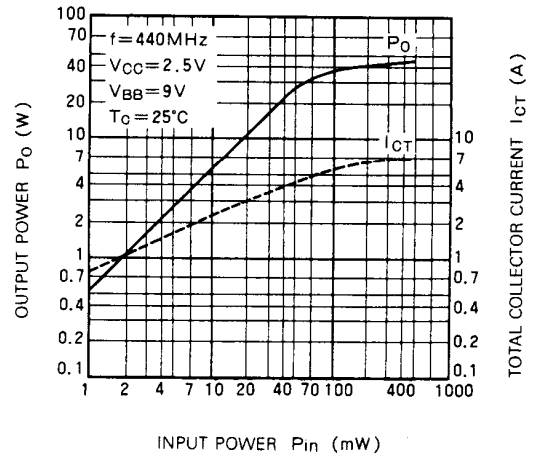
Note. Above parameters, ratings, limits and conditions are subject to change.

TYPICAL PERFORMANCE DATA

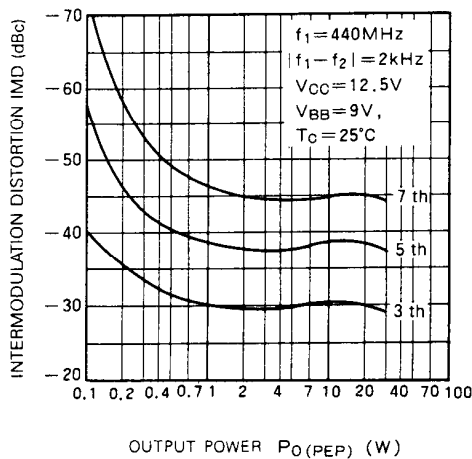
OUTPUT POWER, LINEAR POWER GAIN,
TOTAL EFFICIENCY, INPUT VSWR
VS. FREQUENCY



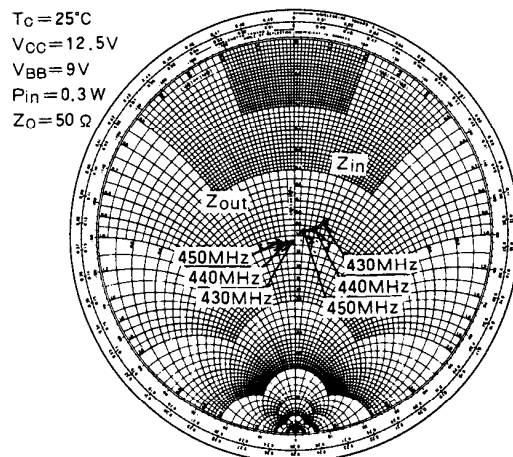
OUTPUT POWER, TOTAL COLLECTOR
CURRENT, VS. INPUT POWER



INTERMODULATION DISTORTION
VS. OUTPUT POWER



INPUT IMPEDANCE, OUTPUT IMPEDANCE
VS. FREQUENCY



DESIGN CONSIDERATION OF HEAT RADIATION.

Please refer to following consideration when designing heat sink.

1. Junction temperature of incorporated transistors at standard operation.

- (1) Thermal resistance between junction and package of incorporated transistors.

a) First stage transistor

$$R_{th(j-c)1} = 12^{\circ}\text{C/W (Typ.)}$$

b) Second stage transistor

$$R_{th(j-c)2} = 4^{\circ}\text{C/W (Typ.)}$$

c) Final stage transistor

$$R_{th(j-c)3} = 1.75^{\circ}\text{C/W (Typ.)}$$

- (2) Junction temperature of incorporated transistors at standard operation.

- Conditions for standard operation.

$P_o = 30\text{W}$, $V_{CC} = 12.5\text{V}$, $P_{in} = 0.3\text{W}$, $\eta_T = 40\%$ (minimum rating), P_{o1} (Note 1) = 2W, P_{o2} (2) = 8W, $I_T = 6\text{A}$ (I_{T1} (3) = 0.35A, I_{T2} (4) = 1.32A, I_{T3} (5) = 4.33A)

Note 1: Output power of the first stage transistor

Note 2: Output power of the second stage transistor

Note 3: Circuit current of the first stage transistor

Note 4: Circuit current of the second stage transistor

Note 5: Circuit current of the final stage transistor

- Junction temperature of the first stage transistor

$$\begin{aligned} T_{j1} &= (V_{CC} \times I_{T1} - P_{o1} + P_{in}) \times R_{th(j-c)1} + T_c^{(6)} \\ &= (12.5 \times 0.35 - 2 + 0.3) \times 12 + T_c \\ &= 32 + T_c (^{\circ}\text{C}) \end{aligned}$$

Note 6: Package temperature of device

- Junction temperature of the second stage transistor

$$\begin{aligned} T_{j2} &= (V_{CC} \times I_{T2} - P_{o2} + P_{o1}) \times R_{th(j-c)2} + T_c \\ &= (12.5 \times 1.32 - 8 + 2) \times 4 + T_c \\ &= 42 + T_c (^{\circ}\text{C}) \end{aligned}$$

- Junction temperature of the final stage transistor

$$\begin{aligned} T_{j3} &= (V_{CC} \times I_{T3} - P_o + P_{o2}) \times R_{th(j-c)3} + T_c \\ &= (12.5 \times 4.33 - 30 + 8) \times 1.75 + T_c \\ &= 56 + T_c (^{\circ}\text{C}) \end{aligned}$$

2. Heat sink design

In thermal design of heat sink, try to keep the package temperature at the upper limit of the operating ambient temperature (normally $T_a = 60^{\circ}\text{C}$) and at the output power of 30W below 90°C .

The thermal resistance $R_{th(c-a)}$ (7) of the heat sink to realize this:

$$\begin{aligned} R_{th(c-a)} &= \frac{T_c - T_a}{(P_o/\eta_T) - P_o + P_{in}} = \frac{90 - 60}{(30/0.4) - 30 + 0.3} \\ &= 0.66 (^{\circ}\text{C/W}) \end{aligned}$$

Note 7: Inclusive of the contact thermal resistance between device and heat sink.

Mounting the heat sink of the above thermal resistance on the device,

$$T_{j1} = 122^{\circ}\text{C}, T_{j2} = 132^{\circ}\text{C}, T_{j3} = 146^{\circ}\text{C} \text{ at } T_a = 60^{\circ}\text{C}, T_c = 90^{\circ}\text{C}.$$

In the annual average of ambient temperature is 30°C ,

$$T_{j1} = 92^{\circ}\text{C}, T_{j2} = 102^{\circ}\text{C}, T_{j3} = 116^{\circ}\text{C}.$$

As the maximum junction temperature of these incorporated transistors T_{jmax} are 175°C , application under fully derated condition is ensured.