



UTRON

Rev. 1.3

UT62L64C

8K X 8 BIT LOW POWER CMOS SRAM

REVISION HISTORY

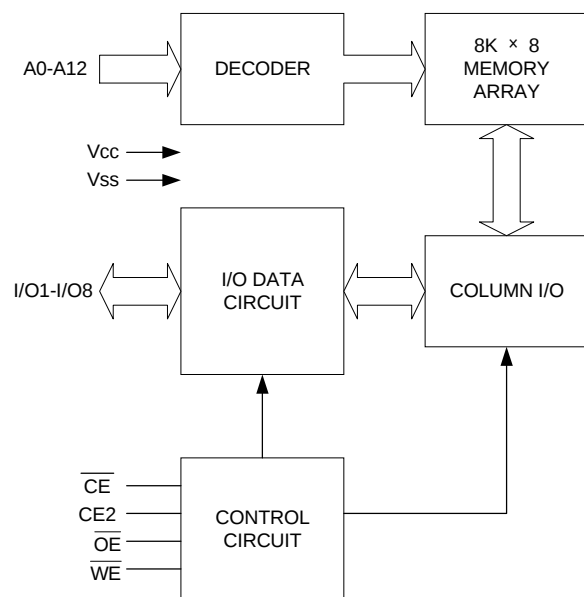
REVISION	DESCRIPTION	Released Date
Rev. 0.1	Original	May 3,2001
Rev. 1.0	Release	Feb.26,2002
Rev. 1.1	Revised - Improve I_{DR} from 20 μ A to 10 μ A (LL-version , max.)	May 14,2002
Rev. 1.2	1. Revised Single power supply : 3.3V $\rightarrow$ 3.0V~3.6V 2. Add Extended temperature : -20 ~85 3. Revised "Order information" : add Extended parts 4. AC/DC characteristics : -add Extended temperature - I_{CC1} (TYP):12 $\rightarrow$ 6mA, I_{CC1} (MAX) : 20 $\rightarrow$ 10mA - I_{CC2} (TYP):6 $\rightarrow$ 12mA, I_{CC2} (MAX) : 10 $\rightarrow$ 20mA	Jul 30,2002
Rev. 1.3	Add order information for lead free product	May 15,2003



FEATURES

- Access time : 35/70ns (max.)
- Low power consumption:
Operating : 30/20 mA (typical)
Standby : 1.5mA (typical) normal
1 μ A (typical) L-version
0.5 μ A (typical) LL-version
- Single 3.0V~3.6V power supply
- Operating temperature :
Commerical : 0 ~70
Extended : -20 ~85
- All inputs and outputs TTL compatible
- Fully static operation
- Three state outputs
- Data retention voltage : 1.5V (min.)
- Package : 28-pin 600mil PDIP
28-pin 330 mil SOP
- Substrate connected : Vcc

FUNCTIONAL BLOCK DIAGRAM

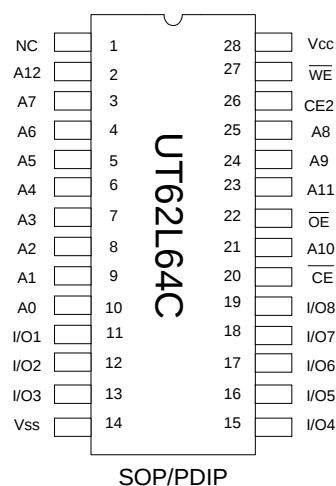


GENERAL DESCRIPTION

The UT62L64C is a 65,536-bits low power CMOS static random access memory organized as 8,192 words by 8 bits. It is fabricated using high performance, high reliability CMOS technology.

Easy memory expansion is provided by using two chip enable input. ($\overline{CE}$, CE2) The UT62L64C operates from a single 3.3V power supply and all inputs and outputs are fully TTL compatible.

PIN CONFIGURATION



PAD DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A12	Address Inputs
I/O1 - I/O8	Data Inputs/Outputs
$\overline{CE}$, CE2	Chip Enable Inputs
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V _{CC}	Power Supply
V _{SS}	Ground
NC	



ABSOLUTE MAXIMUM RATINGS*

PARAMETER		SYMBOL	RATING	UNIT
Terminal Voltage with Respect to V_{SS}		V_{TERM}	-0.5 to 4.5	V
Operating Temperature	Commerical	T_A	0 to 70	
	Extended	T_A	-20 to 85	
Storage Temperature		T_{STG}	-65 to 150	
Power Dissipation		P_D	1	W
DC Output Current		I_{OUT}	50	mA
Soldering Temperature (under 10 sec)		T_{solder}	260	

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	$\overline{CE}$	CE2	$\overline{OE}$	$\overline{WE}$	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	X	High - Z	I_{SB}, I_{SB1}
Standby	X	L	X	X	High - Z	I_{SB}, I_{SB1}
Output Disable	L	H	H	H	High - Z	I_{CC}, I_{CC1}, I_{CC2}
Read	L	H	L	H	DOUT	I_{CC}, I_{CC1}, I_{CC2}
Write	L	H	X	L	DIN	I_{CC}, I_{CC1}, I_{CC2}

note: H = V_{IH} , L = V_{IL} , X = Don't care.

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 3.0\sim 3.6V$, $T_A = 0$ to 70 / -20 to 85 (E))

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT	
Input High Voltage	V_{IH}^{*1}			2.2	-	VCC+0.5	V	
Input Low Voltage	V_{IL}^{*2}			- 0.5	-	0.6	V	
Input Leakage Current	I_{LI}	V_{SS} V_{IN} V_{CC}		- 1	-	1	μA	
Output Leakage Current	I_{LO}	V_{SS} $V_{I/O}$ V_{CC} $\overline{CE} = V_{IH}$ or $CE2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$		- 1	-	1	μA	
Output High Voltage	V_{OH}	$I_{OH} = - 1mA$		2.4	-	-	V	
Output Low Voltage	V_{OL}	$I_{OL} = 4mA$		-	-	0.4	V	
Operating Power Supply Current	I_{CC}	Cycle time=Min, $I_{I/O} = 0mA$		- 35	-	30	40	mA
		$\overline{CE} = V_{IL}$, $CE2 = V_{IH}$		- 70	-	20	30	mA
	I_{CC1}	$\overline{CE} = 0.2V$; $I_{I/O} = 0mA$ other pins at 0.2V or $V_{CC} - 0.2V$;	TCycle =1us	-	6	10	mA	
	I_{CC2}	$\overline{CE} = 0.2V$; $I_{I/O} = 0mA$ other pins at 0.2V or $V_{CC} - 0.2V$	TCycle =500ns	-	12	20	mA	
Standby Current (TTL)	I_{SB}	$\overline{CE} = V_{IH}$ or $CE2 = V_{IL}$ other pins= V_{IL} or V_{IH}	Normal	-	1	10	mA	
			- L/- LL	-	0.3	3	mA	
Standby current (CMOS)	I_{SB1}	$\overline{CE} \quad V_{CC} - 0.2V$ or $CE2 \quad 0.2V$, other pins at 0.2V or $V_{CC} - 0.2V$	Normal	-	1.5	5	mA	
			- L		1	100	μA	
			- LL	-	0.5	50	μA	

Notes:

1. Overshoot : $V_{CC}+3.0v$ for pulse width less than 10ns.
2. Undershoot : $V_{SS}-3.0v$ for pulse width less than 10ns.
3. Overshoot and Undershoot are sampled, not 100% tested.



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CAPACITANCE (TA=25 , f=1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C _{IN}	-	8	pF
Input/Output Capacitance	C _{I/O}	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	C _L = 100pF, I _{OH} /I _{OL} = -1mA/4 mA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 3.0~3.6V, T_A = 0 to 70 / -20 to 85 (E))

(1) READ CYCLE

PARAMETER	SYMBOL	UT62L64C-35		UT62L64C-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t _{RC}	35	-	70	-	ns
Address Access Time	t _{AA}	-	35	-	70	ns
Chip Enable Access Time	t _{ACE}	-	35	-	70	ns
Output Enable Access Time	t _{OE}	-	25	-	35	ns
Chip Enable to Output in Low-Z	t _{CLZ} *	10	-	10	-	ns
Output Enable to Output in Low-Z	t _{OLZ} *	5	-	5	-	ns
Chip Disable to Output in High-Z	t _{CHZ} *	-	25	-	35	ns
Output Disable to Output in High-Z	t _{OHZ} *	-	25	-	35	ns
Output Hold from Address Change	t _{OH}	5	-	5	-	ns

(2) WRITE CYCLE

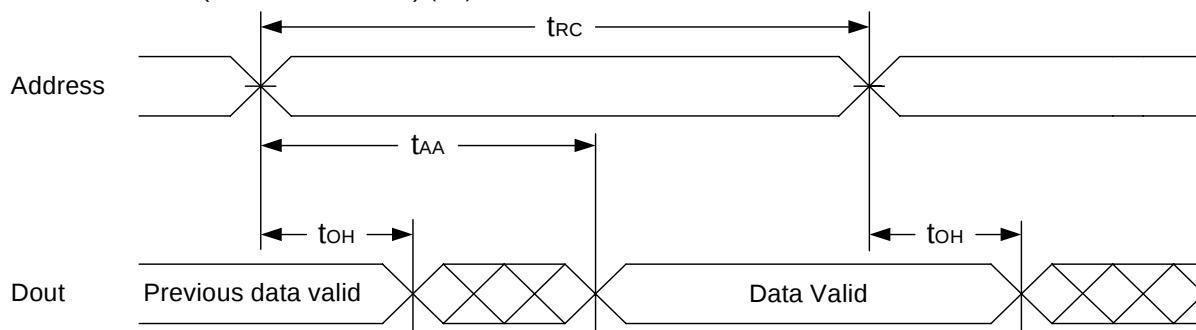
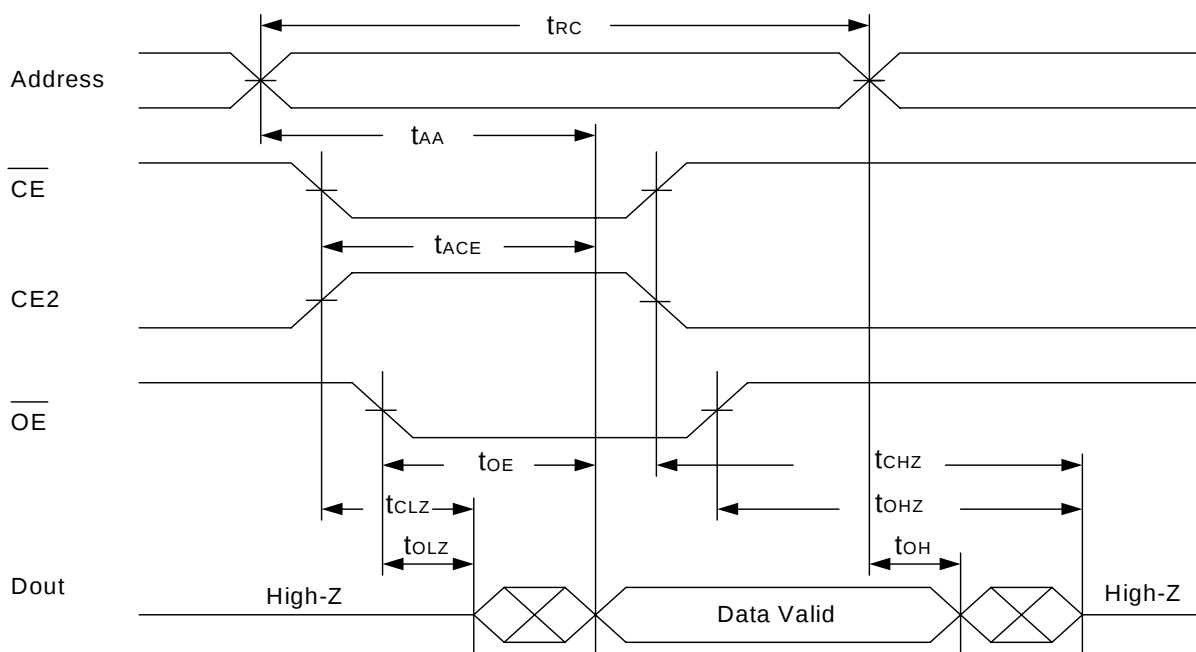
PARAMETER	SYMBOL	UT62L64C-35		UT62L64C-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t _{WC}	35	-	70	-	ns
Address Valid to End of Write	t _{AW}	30	-	60	-	ns
Chip Enable to End of Write	t _{CW}	30	-	60	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	ns
Write Pulse Width	t _{WP}	25	-	50	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	ns
Data to Write Time Overlap	t _{DW}	20	-	30	-	ns
Data Hold from End of Write-Time	t _{DH}	0	-	0	-	ns
Output Active from End of Write	t _{OW} *	5	-	5	-	ns
Write to Output in High-Z	t _{WHZ} *	-	15	-	25	ns

*These parameters are guaranteed by device characterization, but not production tested.



TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)

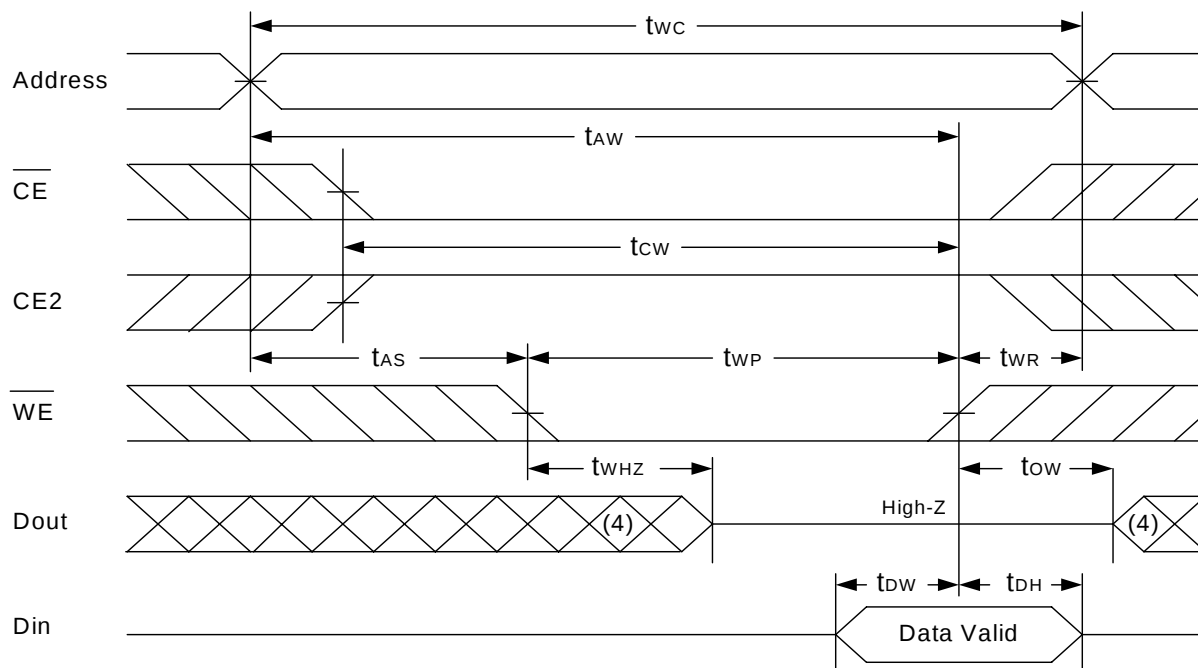
READ CYCLE 2 ($\overline{CE}$ and CE2 and $\overline{OE}$ Controlled) (1,3,4,5)

Notes :

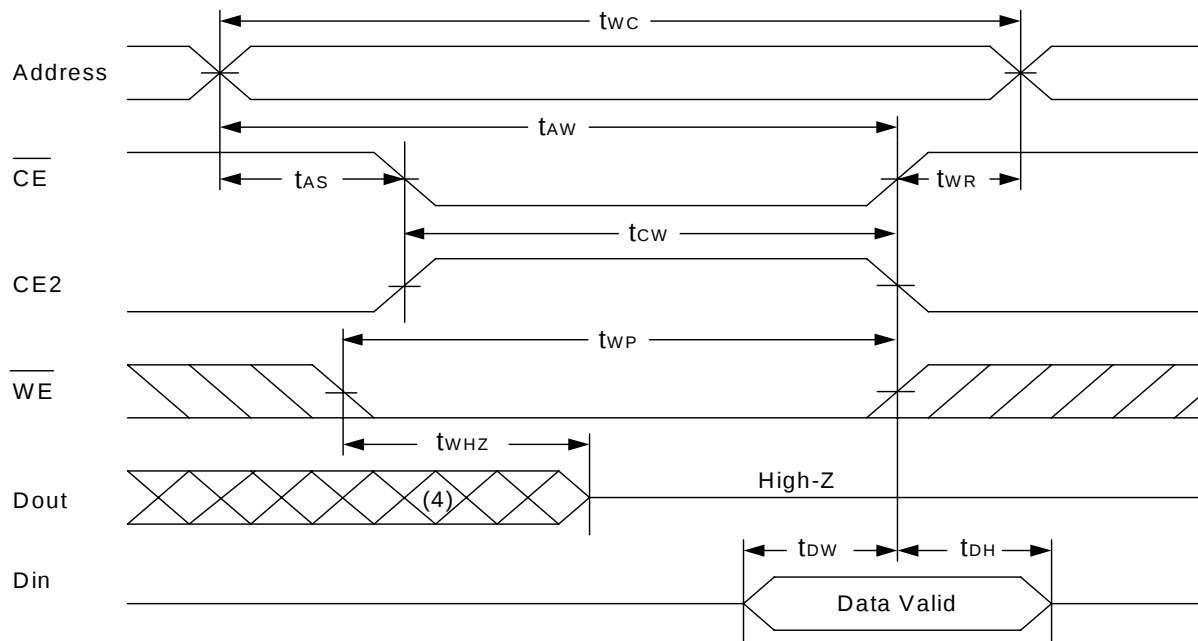
1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected $\overline{OE}$ =low, $\overline{CE}$ =low, CE2=high.
3. Address must be valid prior to or coincident with $\overline{CE}$ =low, CE2=high; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ} , t_{OLZ} , t_{CHZ} and t_{OHZ} are specified with $C_L=5pF$. Transition is measured $\pm 500mV$ from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ} .



WRITE CYCLE 1 ($\overline{\text{WE}}$ Controlled) (1,2,3,5,6)



WRITE CYCLE 2 ($\overline{\text{CE}}$ and CE2 Controlled) (1,2,5,6)



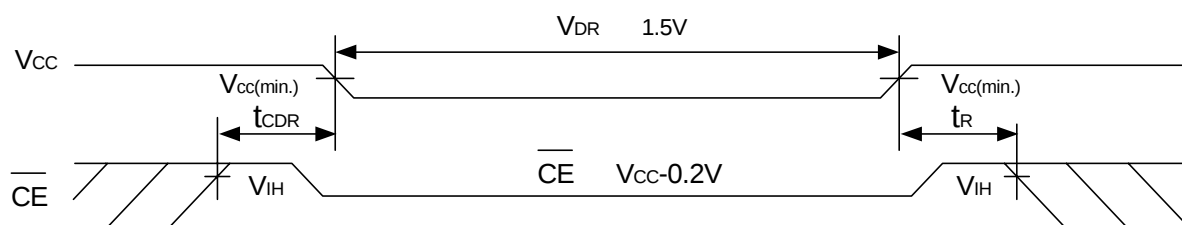
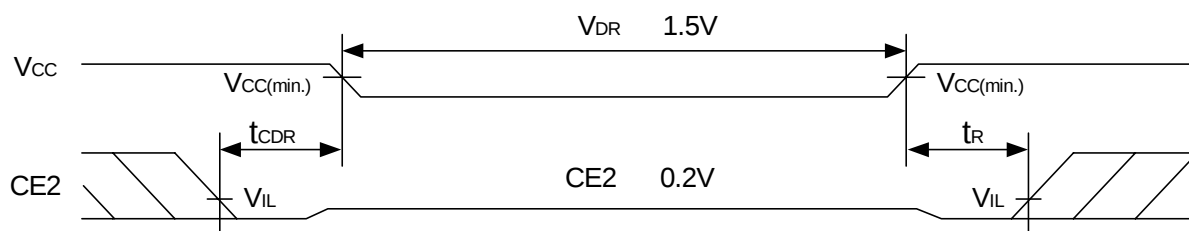


Notes :

1. $\overline{WE}$, $\overline{CE}$ must be high or $\overline{CE2}$ must be low during all address transitions.
2. A write occurs during the overlap of a low $\overline{CE}$, high $\overline{CE2}$, low $\overline{WE}$.
3. During a $\overline{WE}$ controlled write cycle with $\overline{OE}$ low, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ low transition and $\overline{CE2}$ high transition occurs simultaneously with or after $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.

DATA RETENTION CHARACTERISTICS ($T_A = 0$ to 70 / -20 to 85 (E))

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Vcc for Data Retention	V_{DR}	$\overline{CE}$ $V_{CC}-0.2V$ or $\overline{CE2} \leq 0.2V$	1.5	-	3.6	V
Data Retention Current	I_{DR}	$V_{CC}=2.5V$ $\overline{CE}$ $V_{CC}-0.2V$ or $\overline{CE2} \leq 0.2V$	-L	-	1	50 μA
			-LL	-	0.5	10 μA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	t_R		t_{RC}^*	-	-	ns

 $t_{RC}^* = \text{Read Cycle Time}$ **DATA RETENTION WAVEFORM****Low Vcc Data Retention Waveform (1)** ($\overline{CE}$ controlled)**Low Vcc Data Retention Waveform (2)** ($\overline{CE2}$ controlled)



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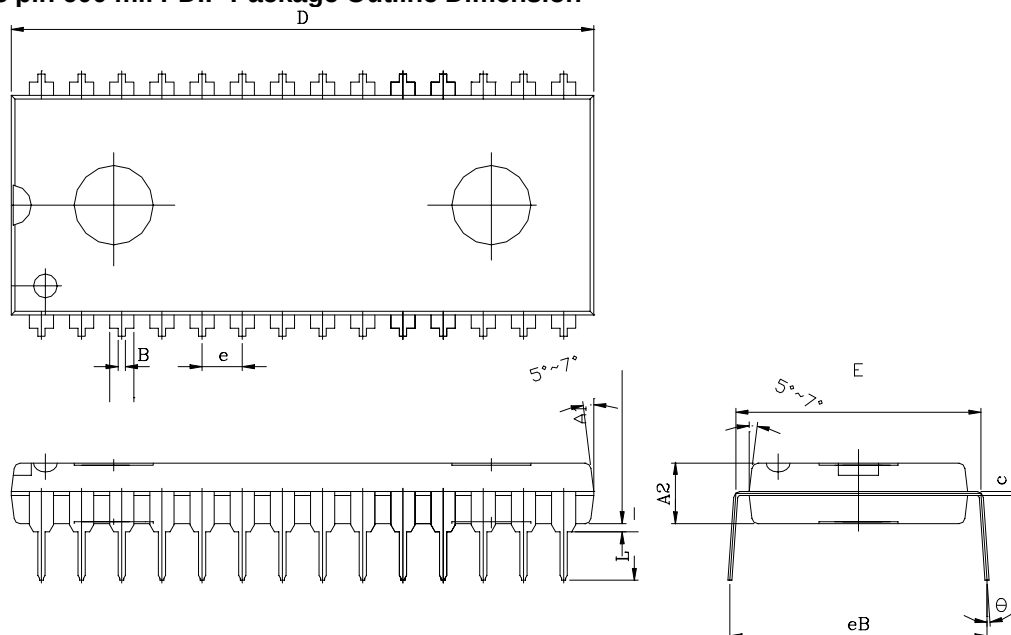
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PACKAGE OUTLINE DIMENSION

28 pin 600 mil PDIP Package Outline Dimension



SYMBOL \ UNIT	INCH(BASE)	MM(REF)
A1	0.010(MIN)	0.254(MIN)
A2	0.150± 0.001	3.810± 0.254
B	0.018± 0.005	0.457± 0.127
c	0.010± 0.004	0.254± 0.102
D	1.460± 0.005	37.084± 0.127
E	0.600± 0.010	15.240± 0.254
e	0.100 (TYP)	2.540(TYP)
eB	0.640± 0.03	16.256± 0.762
L	0.130± 0.010	3.302± 0.254
θ	0°~15°	0°~15°



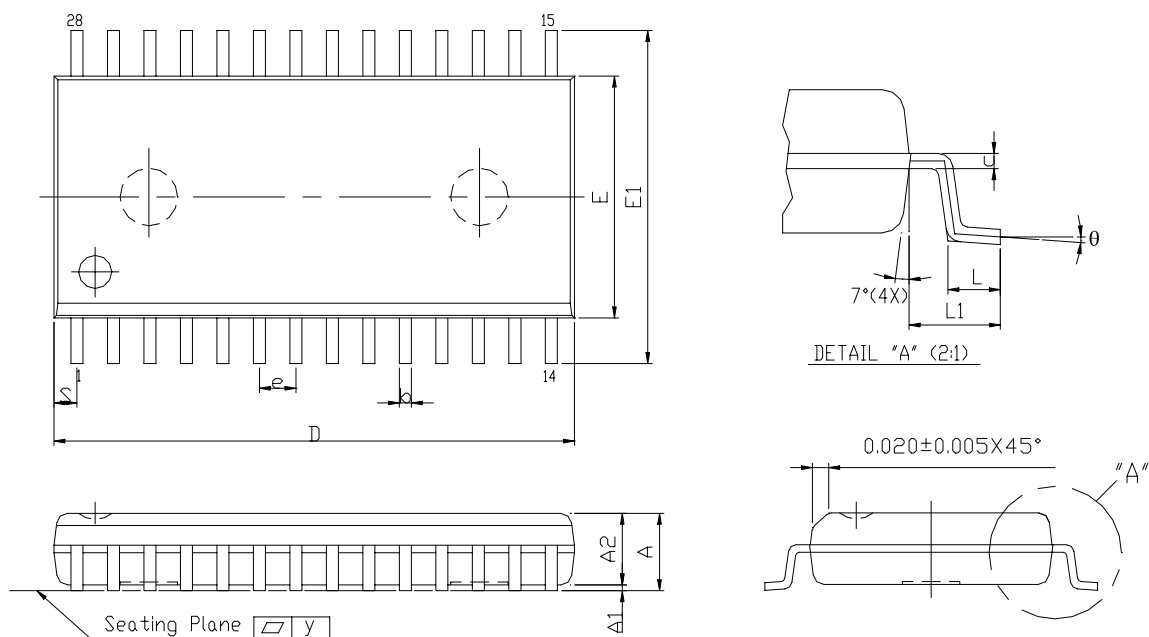
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28 pin 330 mil SOP Package Outline Dimension



UNIT SYMBOL	INCH(BASE)	MM(REF)
A	0.112 (MAX)	2.845 (MAX)
A1	0.004(MIN)	0.102(MIN)
A2	0.098± 0.005	2.489± 0.127
b	0.016 (TYP)	0.406(TYP)
c	0.010 (TYP)	0.254(TYP)
D	0.713± 0.005	18.110± 0.127
E	0.331± 0.005	8.407± 0.127
E1	0.465± 0.012	11.811± 0.305
e	0.050 (TYP)	1.270(TYP)
L	0.0404± 0.008	1.0255± 0.203
L1	0.067± 0.008	1.702 ± 0.203
S	0.047 (MAX)	1.194 (MAX)
y	0.003(MAX)	0.076(MAX)
θ	0° 10°	0° 10°

**ORDERING INFORMATION**

Commerical temperature

PART NO.	ACCESS TIME(ns)	STANDBY CURRENT (μ A) (TYP.)	PACKAGE
UT62L64CPC-35	35	1.5mA	28 PIN PDIP
UT62L64CPC-35L	35	1 μ A	28 PIN PDIP
UT62L64CPC-35LL	35	0.5 μ A	28 PIN PDIP
UT62L64CPC-70	70	1.5mA	28 PIN PDIP
UT62L64CPC-70L	70	1 μ A	28 PIN PDIP
UT62L64CPC-70LL	70	0.5 μ A	28 PIN PDIP
UT62L64CSC-35	35	1.5mA	28 PIN SOP
UT62L64CSC-35L	35	1 μ A	28 PIN SOP
UT62L64CSC-35LL	35	0.5 μ A	28 PIN SOP
UT62L64CSC-70	70	1.5mA	28 PIN SOP
UT62L64CSC-70L	70	1 μ A	28 PIN SOP
UT62L64CSC-70LL	70	0.5 μ A	28 PIN SOP

Extended temperature

PART NO.	ACCESS TIME(ns)	STANDBY CURRENT (μ A) (TYP.)	PACKAGE
UT62L64CPC-35E	35	1.5mA	28 PIN PDIP
UT62L64CPC-35LE	35	1 μ A	28 PIN PDIP
UT62L64CPC-35LLE	35	0.5 μ A	28 PIN PDIP
UT62L64CPC-70E	70	1.5mA	28 PIN PDIP
UT62L64CPC-70LE	70	1 μ A	28 PIN PDIP
UT62L64CPC-70LLE	70	0.5 μ A	28 PIN PDIP
UT62L64CSC-35E	35	1.5mA	28 PIN SOP
UT62L64CSC-35LE	35	1 μ A	28 PIN SOP
UT62L64CSC-35LLE	35	0.5 μ A	28 PIN SOP
UT62L64CSC-70E	70	1.5mA	28 PIN SOP
UT62L64CSC-70LE	70	1 μ A	28 PIN SOP
UT62L64CSC-70LLE	70	0.5 μ A	28 PIN SOP

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Commerical temperature

PART NO.	ACCESS TIME(ns)	STANDBY CURRENT (μ A) (TYP.)	PACKAGE
UT62L64CPCL-35	35	1.5mA	28 PIN PDIP
UT62L64CPCL-35L	35	1 μ A	28 PIN PDIP
UT62L64CPCL-35LL	35	0.5 μ A	28 PIN PDIP
UT62L64CPCL-70	70	1.5mA	28 PIN PDIP
UT62L64CPCL-70L	70	1 μ A	28 PIN PDIP
UT62L64CPCL-70LL	70	0.5 μ A	28 PIN PDIP
UT62L64CSCL-35	35	1.5mA	28 PIN SOP
UT62L64CSCL-35L	35	1 μ A	28 PIN SOP
UT62L64CSCL-35LL	35	0.5 μ A	28 PIN SOP
UT62L64CSCL-70	70	1.5mA	28 PIN SOP
UT62L64CSCL-70L	70	1 μ A	28 PIN SOP
UT62L64CSCL-70LL	70	0.5 μ A	28 PIN SOP

Extended temperature

PART NO.	ACCESS TIME(ns)	STANDBY CURRENT (μ A) (TYP.)	PACKAGE
UT62L64CPCL-35E	35	1.5mA	28 PIN PDIP
UT62L64CPCL-35LE	35	1 μ A	28 PIN PDIP
UT62L64CPCL-35LLE	35	0.5 μ A	28 PIN PDIP
UT62L64CPCL-70E	70	1.5mA	28 PIN PDIP
UT62L64CPCL-70LE	70	1 μ A	28 PIN PDIP
UT62L64CPCL-70LLE	70	0.5 μ A	28 PIN PDIP
UT62L64CSCL-35E	35	1.5mA	28 PIN SOP
UT62L64CSCL-35LE	35	1 μ A	28 PIN SOP
UT62L64CSCL-35LLE	35	0.5 μ A	28 PIN SOP
UT62L64CSCL-70E	70	1.5mA	28 PIN SOP
UT62L64CSCL-70LE	70	1 μ A	28 PIN SOP
UT62L64CSCL-70LLE	70	0.5 μ A	28 PIN SOP



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