

**44A, 50V, 0.022 Ohm, N-Channel UltraFET
Power MOSFET**



This N-Channel power MOSFET is manufactured using the innovative UltraFET® process. This advanced process technology achieves the

lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

Ordering Information

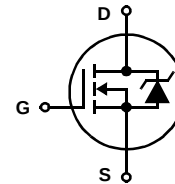
PART NUMBER	PACKAGE	BRAND
HUF75229P3	TO-220AB	75229P

NOTE: When ordering use the entire part number.

Features

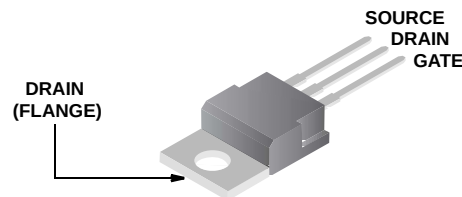
- 44A, 50V
- Low On-Resistance, $r_{DS(ON)} = 0.022\Omega$
- Temperature Compensating PSPICE® Model
- Thermal Impedance SPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
 - TB334, "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol



Packaging

JEDEC TO-220AB



Product reliability information can be found at <http://www.fairchildsemi.com/products/discrete/reliability/index.html>

For severe environments, see our Automotive HUFA series.

All Fairchild semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

HUF75229P3

Absolute Maximum Ratings $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

			UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	50	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	V_{DGR}	50	V
Gate to Source Voltage	V_{GS}	± 20	V
Drain Current			
Continuous (Figure 2)	I_D	44	A
Pulsed Drain Current	I_{DM}	Figure 5	
Pulsed Avalanche Rating	E_{AS}	Figure 6, 14, 15	
Power Dissipation	P_D	90	W
Derate Above 25°C		0.6	W/ $^{\circ}\text{C}$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	$^{\circ}\text{C}$
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s.	T_L	300	$^{\circ}\text{C}$
Package Body for 10s, See Techbrief 334.	T_{pkg}	260	$^{\circ}\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^{\circ}\text{C}$ to 150°C .

Electrical Specifications $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV _{DSS}	I _D = 250μA, V _{GS} = 0V (Figure 11)		50	-	-	V
Gate to Source Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250μA (Figure 10)		2	-	4	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 45V, V _{GS} = 0V		-	-	1	μA
		V _{DS} = 40V, V _{GS} = 0V, T _C = 150°C		-	-	250	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20V		-	-	±100	nA
Drain to Source On Resistance	r _{DS(ON)}	I _D = 44A, V _{GS} = 10V (Figure 9)		0.017	0.020	0.022	Ω
Turn-On Time	t _{ON}	V _{DD} = 30V, I _D ≅ 44A, R _L = 0.68Ω, V _{GS} = 10V, R _{GS} = 9.1Ω (Figures 18, 19)		-	-	105	ns
Turn-On Delay Time	t _{d(ON)}			-	12	-	ns
Rise Time	t _r			-	58	-	ns
Turn-Off Delay Time	t _{d(OFF)}			-	33	-	ns
Fall Time	t _f			-	33	-	ns
Turn-Off Time	t _{OFF}			-	-	100	ns
Total Gate Charge	Q _{g(TOT)}	V _{GS} = 0V to 20V	V _{DD} = 30V, I _D ≅ 44A, R _L = 0.68Ω I _{g(REF)} = 1.0mA (Figures 13, 16, 17)	-	60	75	nC
Gate Charge at 10V	Q _{g(10)}	V _{GS} = 0V to 10V		-	35	43	nC
Threshold Gate Charge	Q _{g(TH)}	V _{GS} = 0V to 2V		-	2.0	2.5	nC
Input Capacitance	C _{ISS}	V _{DS} = 25V, V _{GS} = 0V, f = 1MHz (Figure 12)		-	1060	-	pF
Output Capacitance	C _{OSS}			-	405	-	pF
Reverse Transfer Capacitance	C _{RSS}			-	95	-	pF
Thermal Resistance Junction to Case	R _{θJC}	(Figure 3)		-	-	1.66	°C/W
Thermal Resistance Junction to Ambient	R _{θJA}	TO-220		-	-	62	°C/W

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 44\text{A}$	-	-	1.25	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 44\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	72	ns
Reverse Recovered Charge	Q_{RR}	$I_{SD} = 44\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	120	nC

Typical Performance Curves

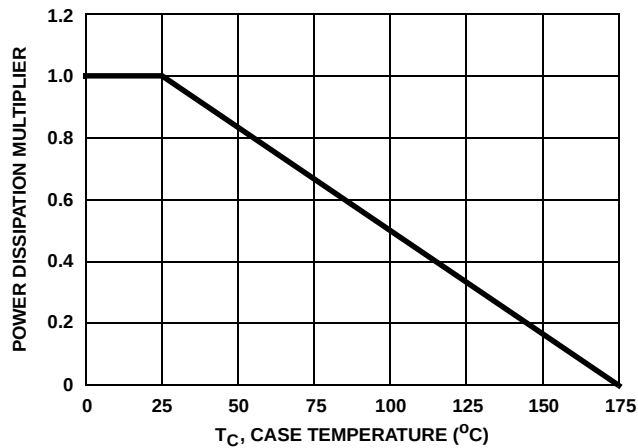


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

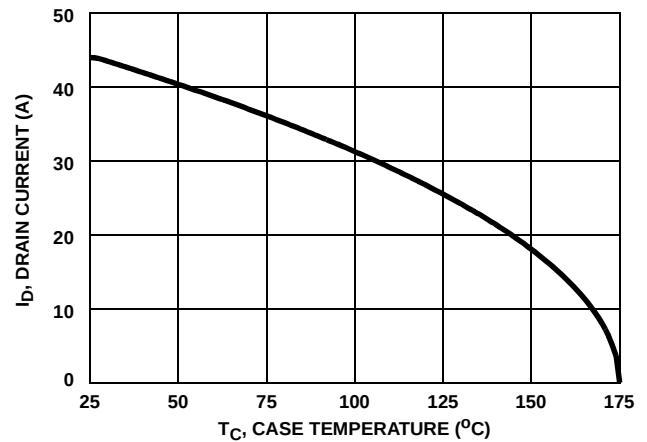


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

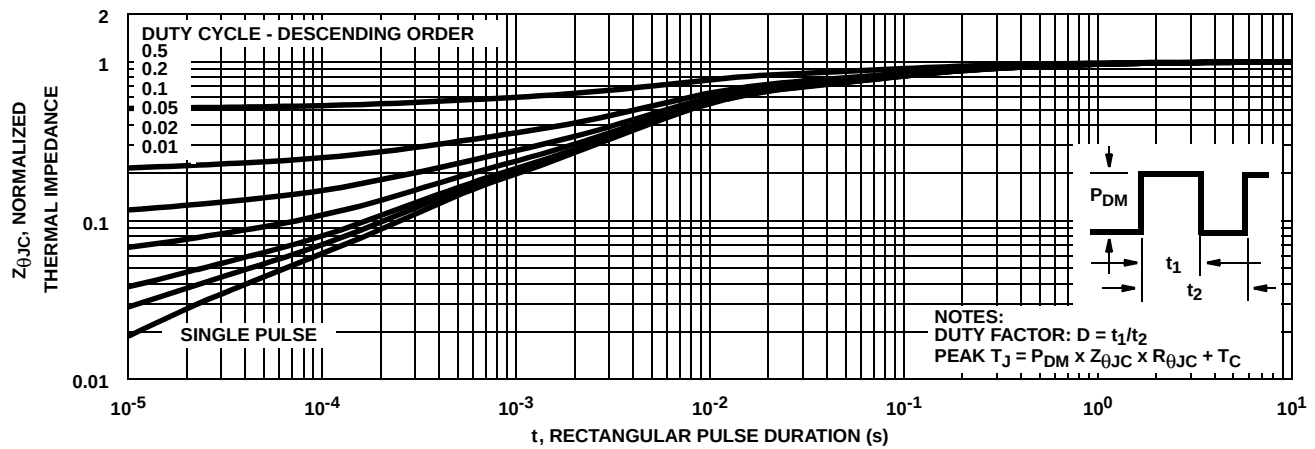


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

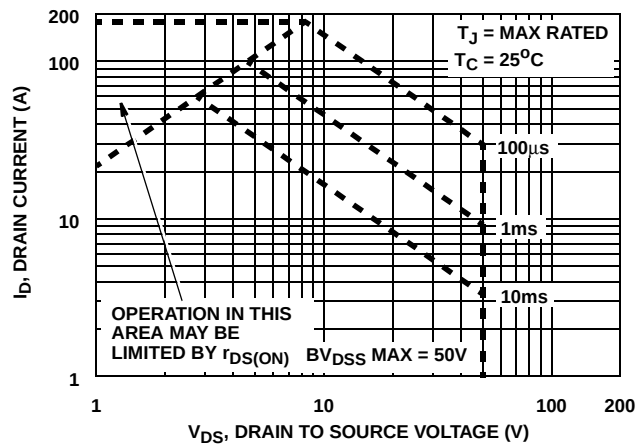


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

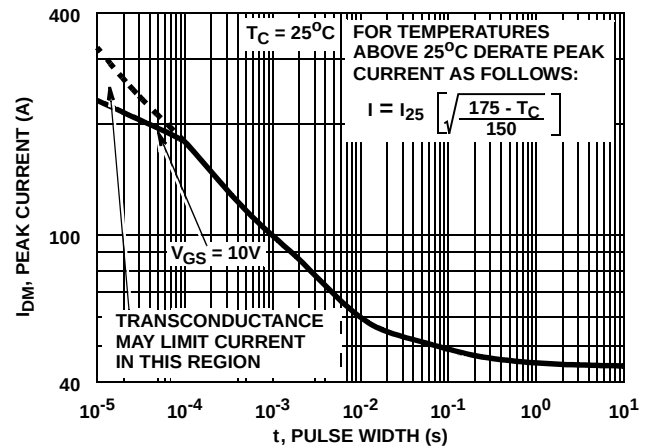
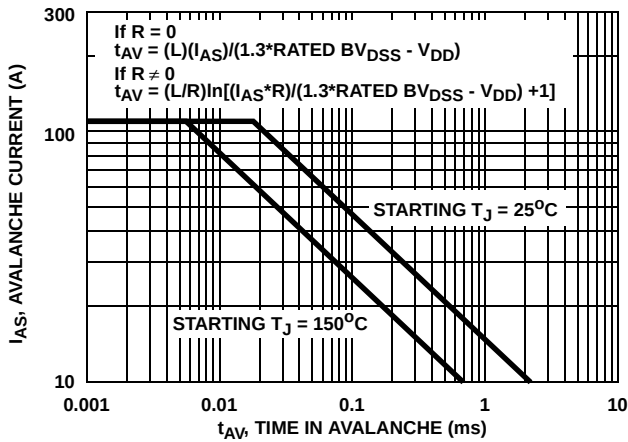


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)



NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

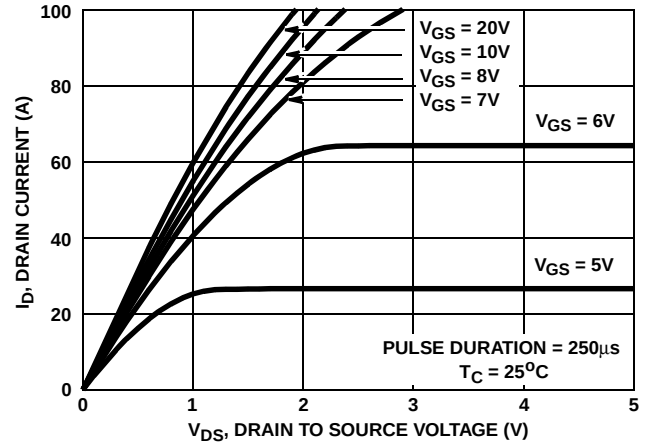


FIGURE 7. SATURATION CHARACTERISTICS

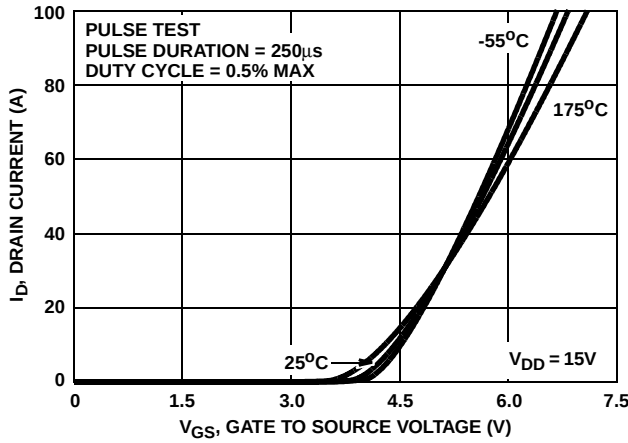


FIGURE 8. TRANSFER CHARACTERISTICS

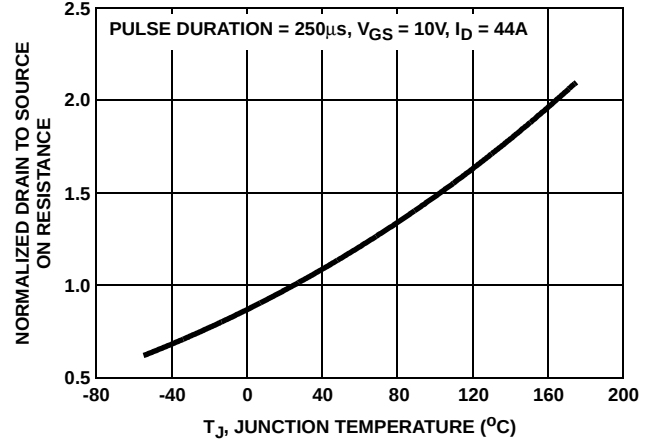


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

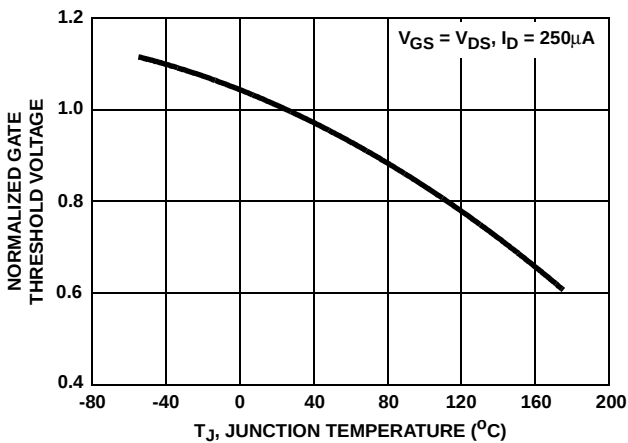


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

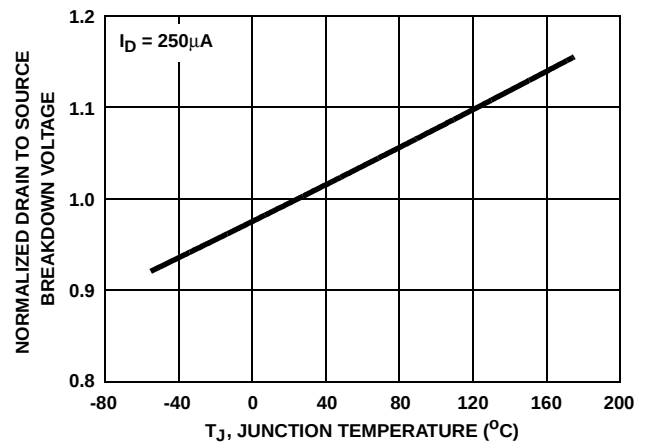


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

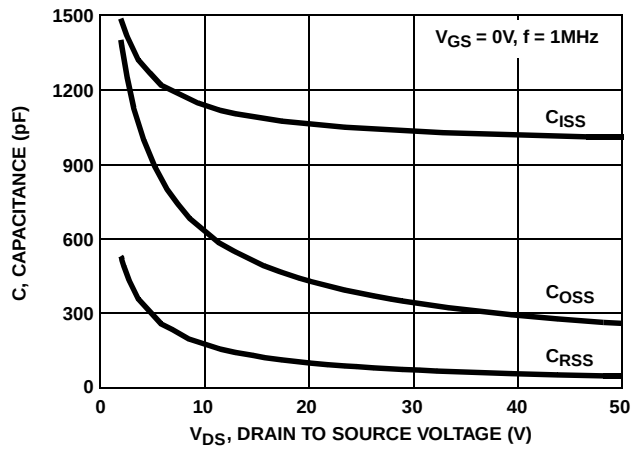
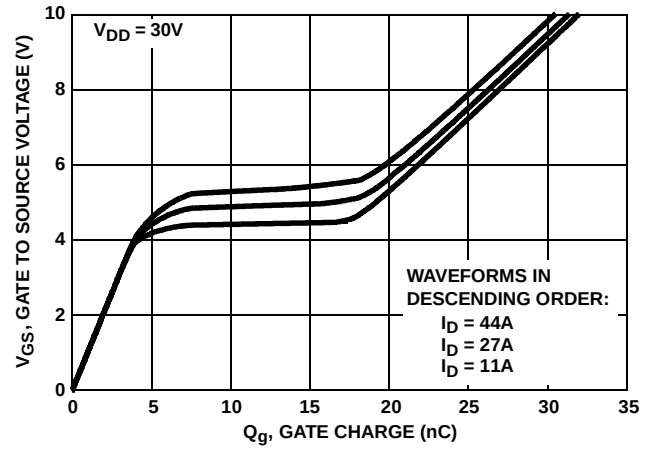


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 13. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

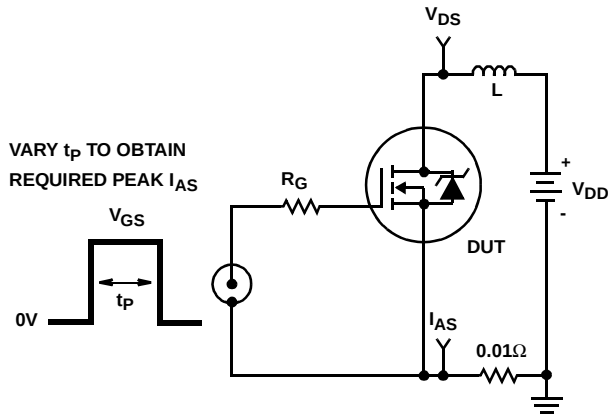


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

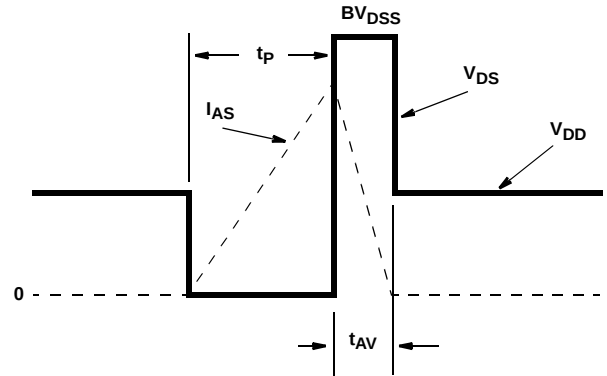


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

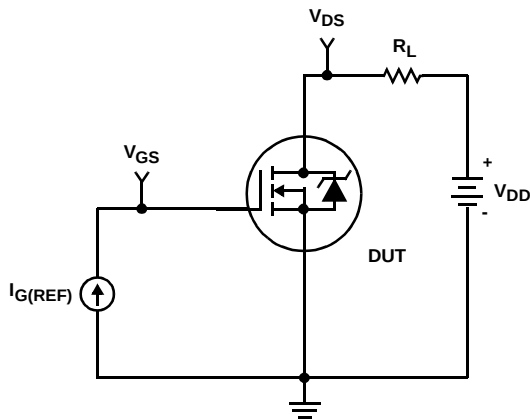


FIGURE 16. GATE CHARGE TEST CIRCUIT

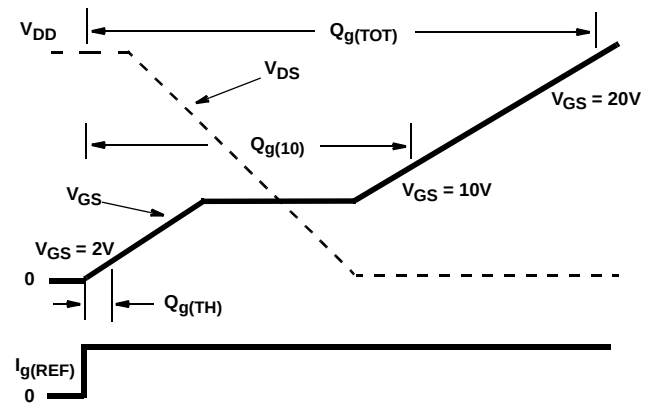


FIGURE 17. GATE CHARGE WAVEFORM

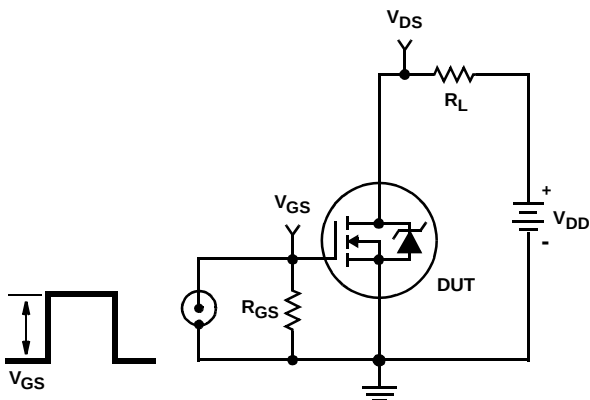


FIGURE 18. SWITCHING TIME TEST CIRCUIT

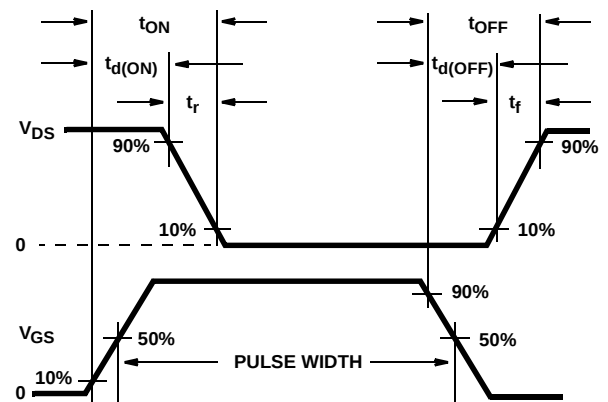


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

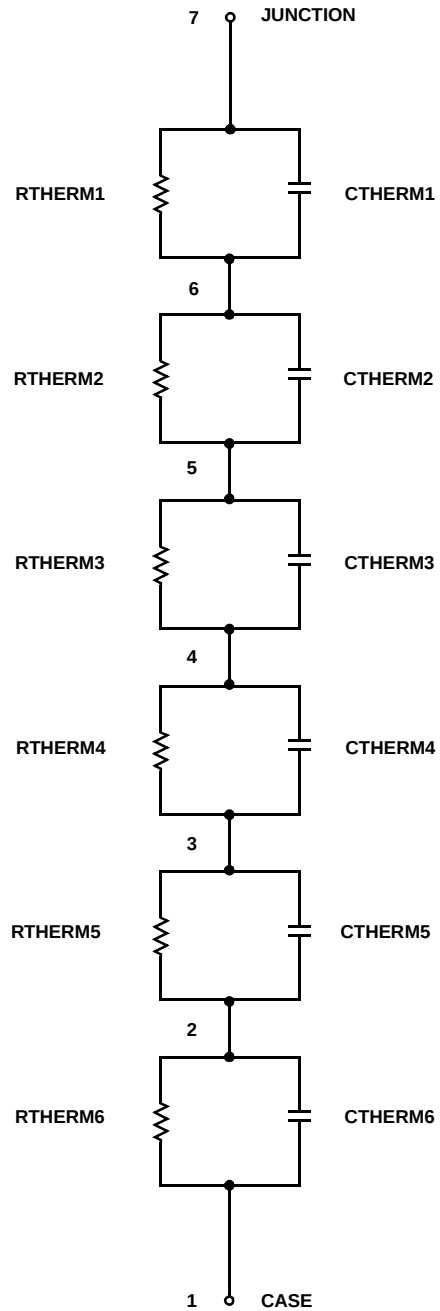
SPICE Thermal Model

REV 16 June 97

HUF75229P3

CTHERM1 7 6 4.90e-7
 CHERM2 6 5 4.90e-4
 CHERM3 5 4 1.96e-3
 CHERM4 4 3 7.90e-3
 CHERM5 3 2 1.85e-1
 CHERM6 2 1 2.70

RHERM1 7 6 1.10e-2
 RHERM2 6 5 3.30e-2
 RHERM3 5 4 1.64e-1
 RHERM4 4 3 7.90e-1
 RHERM5 3 2 3.60e-1
 RHERM6 2 1 1.60e-1



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