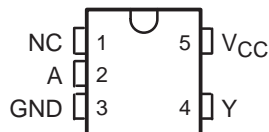


# SN74AUP1G07 LOW-POWER SINGLE BUFFER/DRIVER WITH OPEN-DRAIN OUTPUTS

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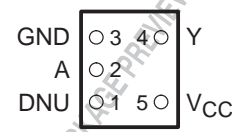
- Available in the Texas Instruments NanoStar™ and NanoFree™ Packages
- Low Static-Power Consumption;  
 $I_{CC} = 0.9 \mu A$  Max
- Low Dynamic-Power Consumption;  
 $C_{pd} = 1 \text{ pF}$  Typ at 3.3 V
- Low Input Capacitance;  $C_i = 1.5 \text{ pF}$  Typ
- Low Noise – Overshoot and Undershoot  
<10% of  $V_{CC}$
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Input Hysteresis Allows Slow Input Transition and Better Switching Noise Immunity at the Input  
( $V_{hys} = 250 \text{ mV}$  Typ at 3.3 V)
- Wide Operating  $V_{CC}$  Range of 0.8 V to 3.6 V
- Optimized for 3.3-V Operation
- 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- $t_{pd} = 3.3 \text{ ns}$  Max at 3.3 V
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- ESD Protection Exceeds  $\pm 5000 \text{ V}$  With Human-Body Model

DBV OR DCK PACKAGE  
(TOP VIEW)



NC – No internal connection

YEP OR YZP PACKAGE  
(BOTTOM VIEW)



DNU – Do not use

## description/ordering information

The AUP family is TI's premier solution to the industry's low power needs in battery-powered portable applications. This family ensures a very low static and dynamic power consumption across the entire  $V_{CC}$  range of 0.8 V to 3.6 V, resulting in an increased battery life. This product also maintains excellent signal integrity (see Figures 1 and 2).

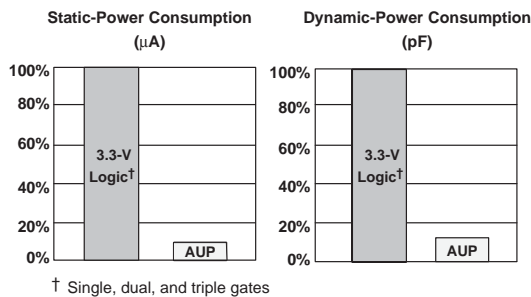


Figure 1. AUP – The Lowest-Power Family

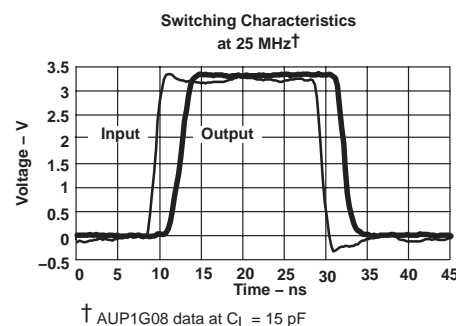


Figure 2. Excellent Signal Integrity

The output of this single buffer/driver is open drain, and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoStar and NanoFree are trademarks of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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description/ordering information (continued)

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
–40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP	Reel of 3000	SN74AUP1G07YEPR	___HV_
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)		SN74AUP1G07YZPR	
	SOT (SOT-23) – DBV	Reel of 3000	SN74AUP1G07DBVR	H07_
		Reel of 250	SN74AUP1G07DBVT	
	SOT (SC-70) – DCK	Reel of 3000	SN74AUP1G07DCKR	HV_
		Reel of 250	SN74AUP1G07DCKT	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

‡ DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site.  
YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

logic diagram (positive logic)



# SN74AUP1G07

## LOW-POWER SINGLE BUFFER/DRIVER WITH OPEN-DRAIN OUTPUTS

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1)	–0.5 V to 4.6 V
Output voltage range in the high or low state, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Continuous output current, $I_O$	±20 mA
Continuous current through $V_{CC}$ or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DBV package	206°C/W
DCK package	252°C/W
YEP/YZP package	132°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	0.8	3.6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 0.8$ V	$V_{CC}$	V
		$V_{CC} = 1.1$ V to 1.95 V	$0.65 \times V_{CC}$	
		$V_{CC} = 2.3$ V to 2.7 V	1.6	
		$V_{CC} = 3$ V to 3.6 V	2	
$V_{IL}$	Low-level input voltage	$V_{CC} = 0.8$ V	0	V
		$V_{CC} = 1.1$ V to 1.95 V	$0.35 \times V_{CC}$	
		$V_{CC} = 2.3$ V to 2.7 V	0.7	
		$V_{CC} = 3$ V to 3.6 V	0.9	
$V_I$	Input voltage	0	3.6	V
$V_O$	Output voltage	0	3.6	V
$I_{OL}^{\ddagger}$	Low-level output current	$V_{CC} = 0.8$ V	20	μA
		$V_{CC} = 1.1$ V	1.1	mA
		$V_{CC} = 1.4$ V	1.7	
		$V_{CC} = 1.65$ V	1.9	
		$V_{CC} = 2.3$ V	3.1	
		$V_{CC} = 3$ V	4	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 0.8$ V to 3.6 V	200	ns/V
$T_A$	Operating free-air temperature	–40	85	°C

<sup>‡</sup> Defined by the signal integrity requirements and design goal priorities.

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



# SN74AUP1G07

## LOW-POWER SINGLE BUFFER/DRIVER

### WITH OPEN-DRAIN OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = –40°C TO 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
V <sub>OL</sub>	I <sub>OL</sub> = 20 µA	0.8 V to 3.6 V			0.1		0.1	V
	I <sub>OL</sub> = 1.1 mA	1.1 V			0.3 × V <sub>CC</sub>		0.3 × V <sub>CC</sub>	
	I <sub>OL</sub> = 1.7 mA	1.4 V			0.31		0.37	
	I <sub>OL</sub> = 1.9 mA	1.65 V			0.31		0.35	
	I <sub>OL</sub> = 2.3 mA	2.3 V			0.31		0.33	
	I <sub>OL</sub> = 3.1 mA				0.44		0.45	
	I <sub>OL</sub> = 2.7 mA	3 V			0.31		0.33	
	I <sub>OL</sub> = 4 mA				0.44		0.45	
I <sub>I</sub>	A input	V <sub>I</sub> = GND to 3.6 V			0.1		0.5	µA
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V			0.2		0.6	µA
ΔI <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V			0.2		0.6	µA
I <sub>CC</sub>		V <sub>I</sub> = GND or V <sub>CC</sub> to 3.6 V, I <sub>O</sub> = 0			0.5		0.9	µA
ΔI <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> – 0.6 V, I <sub>O</sub> = 0			40		50	µA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	0 V		1.5				pF
		3.6 V		1.7				
C <sub>O</sub>	V <sub>O</sub> = GND	0 V		1.7				pF

switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 5 pF (unless otherwise noted) (see Figures 3 and 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = –40°C TO 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	0.8 V			12.2			ns
			1.2 V ± 0.1 V	3.4	5.1	7.5	1.5	14.7	
			1.5 V ± 0.1 V	2.3	3.6	5.1	1.3	8.3	
			1.8 V ± 0.15 V	2.4	3.1	4	1	6.3	
			2.5 V ± 0.2 V	1.5	2.1	2.9	0.9	4.1	
			3.3 V ± 0.3 V	1.8	2.2	2.8	1.1	3.3	

switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 10 pF (unless otherwise noted) (see Figures 3 and 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = –40°C TO 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	0.8 V			15			ns
			1.2 V ± 0.1 V	4	6.2	9	2.4	16.2	
			1.5 V ± 0.1 V	3.1	4.4	6.1	2	9.4	
			1.8 V ± 0.15 V	3.3	3.9	4.8	1.6	7.1	
			2.5 V ± 0.2 V	2.1	2.8	3.5	1.3	4.8	
			3.3 V ± 0.3 V	2.3	3	4	1.4	4.5	



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switching characteristics over recommended operating free-air temperature range,  $C_L = 15 \text{ pF}$  (unless otherwise noted) (see Figures 3 and 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ TO $85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A	Y	0.8 V		18.2				ns
			$1.2 \text{ V} \pm 0.1 \text{ V}$	4.9	7.3	10.4	3.2	17.6	
			$1.5 \text{ V} \pm 0.1 \text{ V}$	3.8	5.2	6.8	2.6	10.2	
			$1.8 \text{ V} \pm 0.15 \text{ V}$	3.4	4.8	6.7	2.2	7.9	
			$2.5 \text{ V} \pm 0.2 \text{ V}$	2.4	3.4	4.5	1.9	5.3	
			$3.3 \text{ V} \pm 0.3 \text{ V}$	2.2	3.7	5.4	1.8	6.1	

switching characteristics over recommended operating free-air temperature range,  $C_L = 30 \text{ pF}$  (unless otherwise noted) (see Figures 3 and 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ TO $85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A	Y	0.8 V		26.5				ns
			$1.2 \text{ V} \pm 0.1 \text{ V}$	8.1	10.7	14.4	4.5	21.9	
			$1.5 \text{ V} \pm 0.1 \text{ V}$	6.5	7.7	9.4	3.8	13	
			$1.8 \text{ V} \pm 0.15 \text{ V}$	5.8	7.5	9.7	3.2	11	
			$2.5 \text{ V} \pm 0.2 \text{ V}$	4.5	5.4	6.7	3	7.1	
			$3.3 \text{ V} \pm 0.3 \text{ V}$	3.9	6.3	9.7	2.8	10.4	

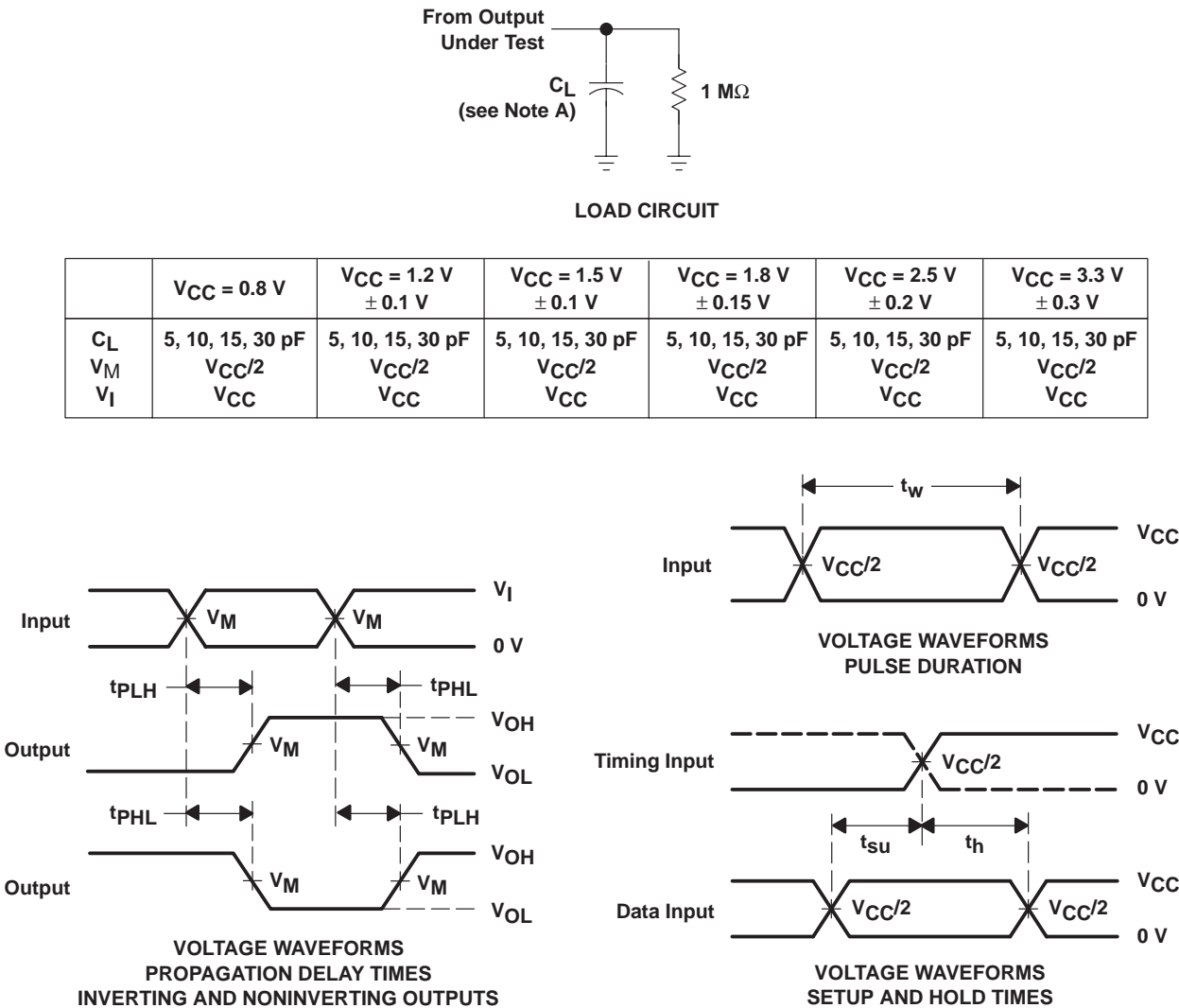
operating characteristics,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC}$	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	$f = 10 \text{ MHz}$	0.8 V	1	pF
			$1.2 \text{ V} \pm 0.1 \text{ V}$	1	
			$1.5 \text{ V} \pm 0.1 \text{ V}$	1	
			$1.8 \text{ V} \pm 0.15 \text{ V}$	1	
			$2.5 \text{ V} \pm 0.2 \text{ V}$	1	
			$3.3 \text{ V} \pm 0.3 \text{ V}$	1	

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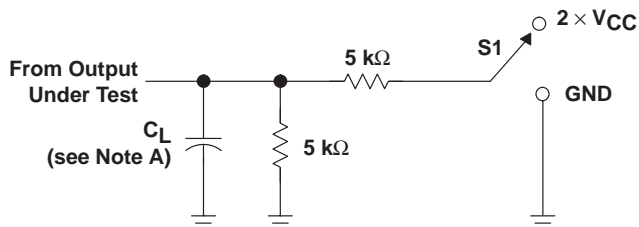
**PARAMETER MEASUREMENT INFORMATION**  
(Propagation Delays, Setup and Hold Times, and Pulse Width)



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50\ \Omega$ ,  $t_r/t_f = 3\text{ ns}$ .  
C. The outputs are measured one at a time, with one transition per measurement.  
D.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
E. All parameters and waveforms are not applicable to all devices.

**Figure 3. Load Circuit and Voltage Waveforms**

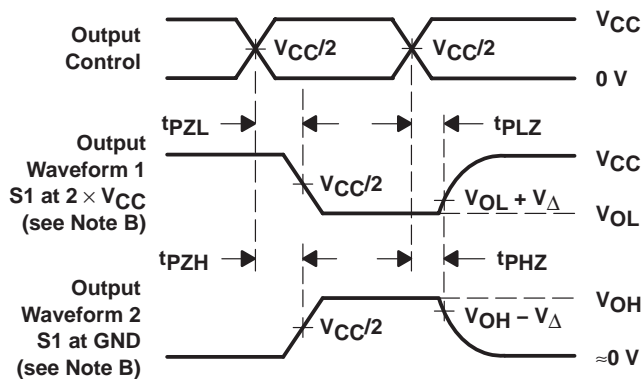
### PARAMETER MEASUREMENT INFORMATION (Enable and Disable Times)



TEST	S1
$t_{PLZ}/t_{PZL}$ $t_{PHZ}/t_{PZH}$	2 $\times$ $V_{CC}$ GND

LOAD CIRCUIT

	$V_{CC} = 0.8\text{ V}$	$V_{CC} = 1.2\text{ V}$ $\pm 0.1\text{ V}$	$V_{CC} = 1.5\text{ V}$ $\pm 0.1\text{ V}$	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$
$C_L$	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
$V_M$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
$V_I$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$
$V_{\Delta}$	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



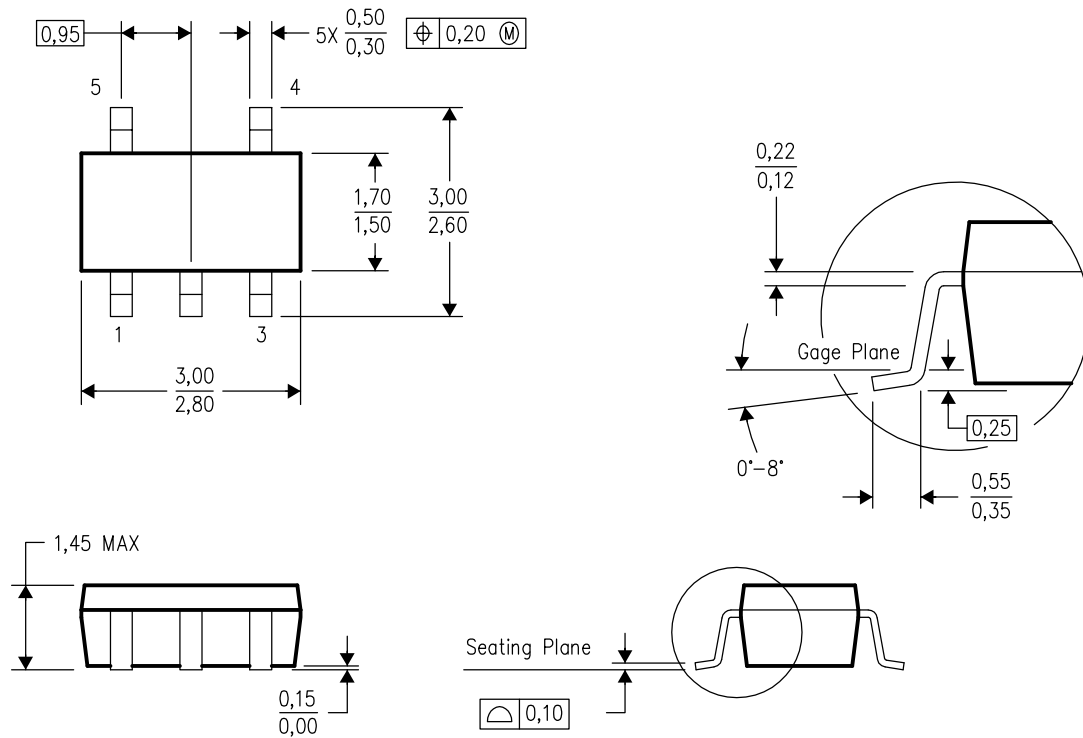
VOLTAGE WAVEFORMS  
 ENABLE AND DISABLE TIMES  
 LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r/t_f = 3\text{ ns}$ .
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

## DBV (R-PDSO-G5)

## PLASTIC SMALL-OUTLINE PACKAGE



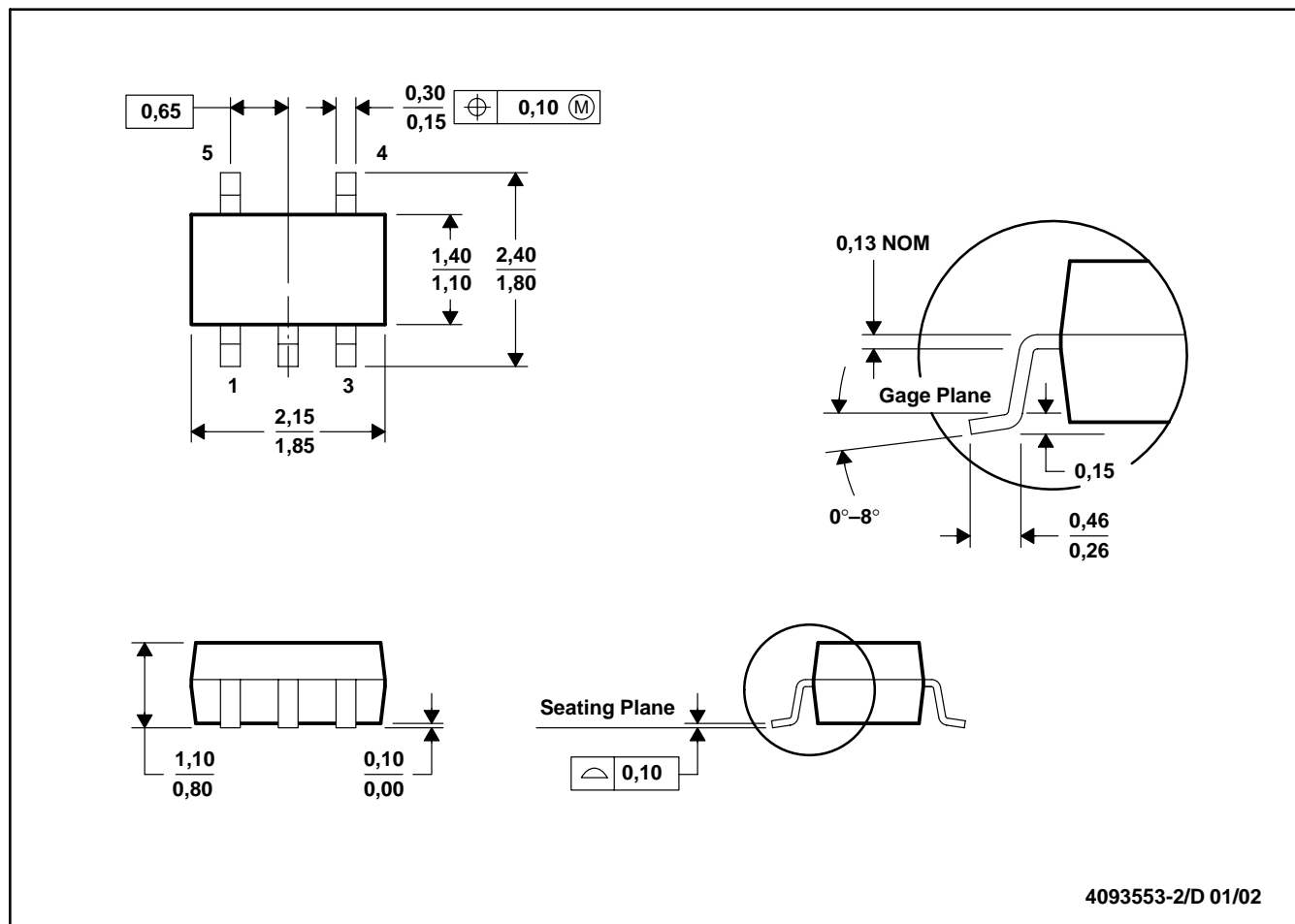
4073253-4/H 10/2003

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion.
  - D. Falls within JEDEC MO-178 Variation AA.



## DCK (R-PDSO-G5)

## PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion.
  - Falls within JEDEC MO-203

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