

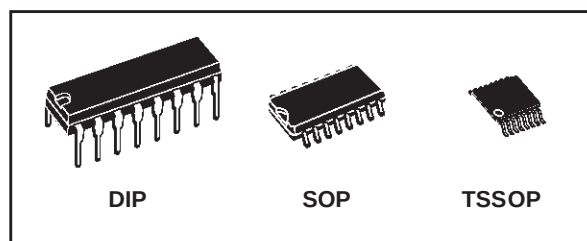
3 TO 8 LINE DECODER/LATCH (INVERTING)

- HIGH SPEED:
 $t_{PD} = 17\text{ns}$ (TYP.) at $V_{CC} = 4.5\text{V}$
- LOW POWER DISSIPATION:
 $I_{CC} = 4\mu\text{A}$ (MAX.) at $T_A = 25^\circ\text{C}$
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 4\text{mA}$ (MIN)
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \approx t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:
 V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 137

DESCRIPTION

The M74HCT137 is an high speed CMOS 3 TO 8 LINE DECODER/LATCH (INVERTING) fabricated with silicon gate C²MOS technology.

This device is a 3 to 8 line decoder with latches on the three address inputs. When $\overline{GL}$ goes from low to high, the addresses present at the select inputs (A , B , and C) is stored in the latches. As long as $\overline{GL}$ remains high no address changes will be recognized. Output enable pins $G1$ and $\overline{G2}$, control the state of the outputs independently of the select or latch-enable inputs. All the outputs

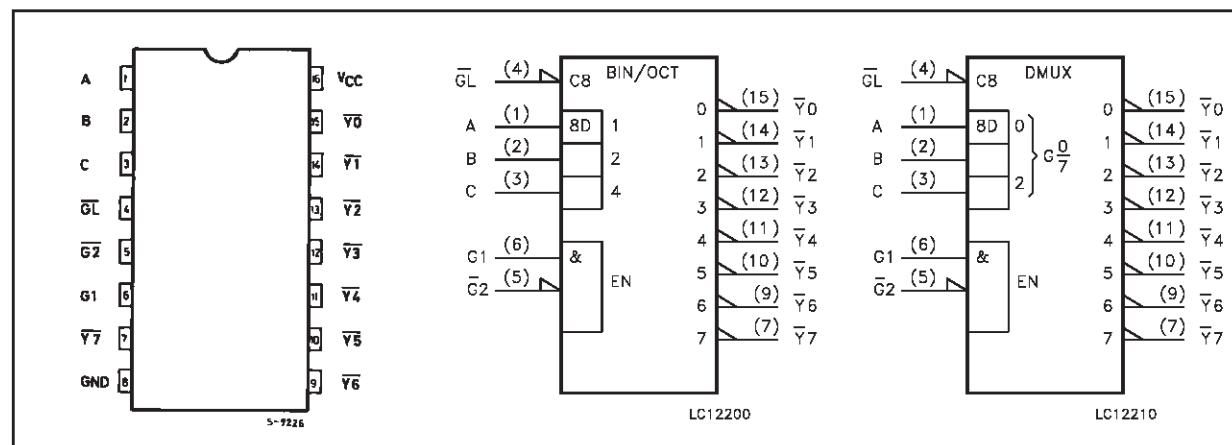


ORDER CODES

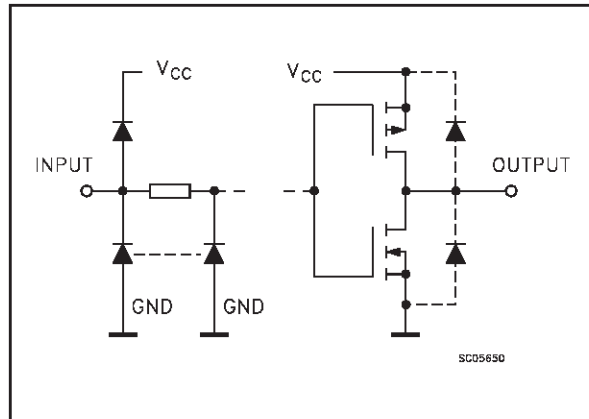
PACKAGE	TUBE	T & R
DIP	M74HCT137B1R	
SOP	M74HCT137M1R	M74HCT137RM13TR
TSSOP		M74HCT137TTR

are high unless $G1$ is high and $\overline{G2}$ is low. The 74HCT137 is ideally suited for the implementation of glitch-free decoders in stored-address application in bus oriented systems. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT AND OUTPUT EQUIVALENT CIRCUIT



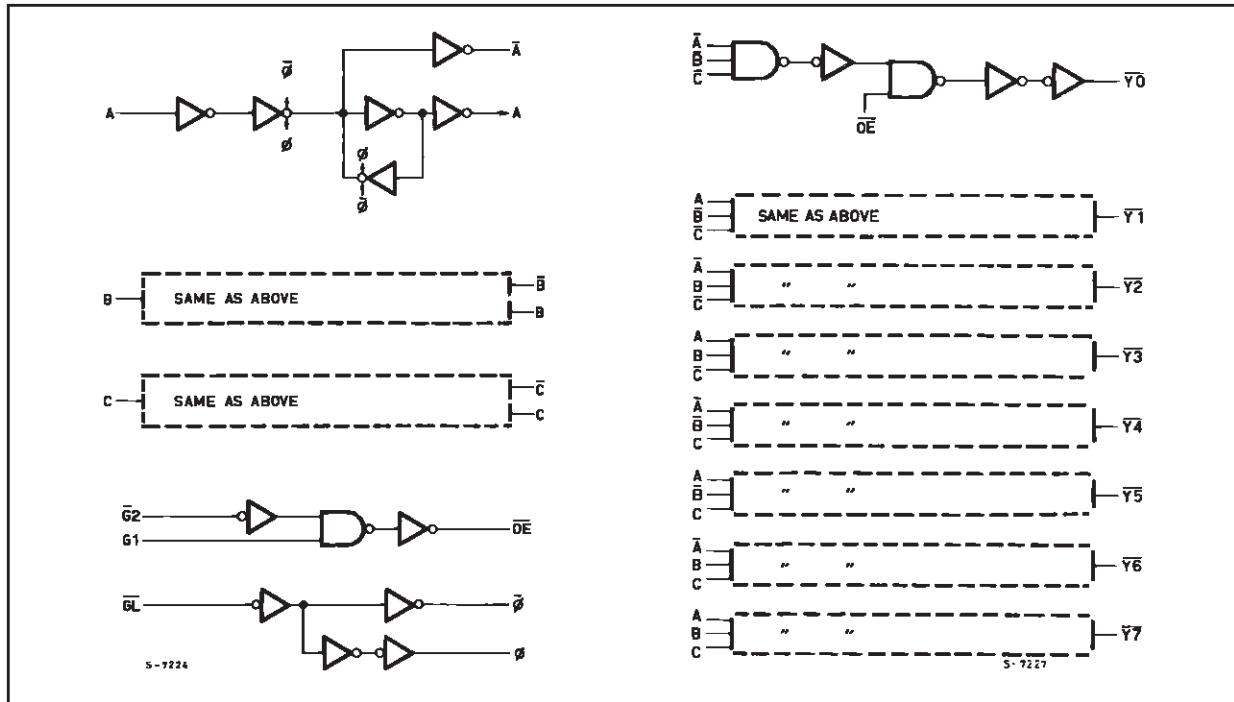
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 2, 3	A to C	Data Inputs
4	$\overline{\text{GL}}$	Latch Enable Input (Active LOW)
5	$\overline{\text{G2}}$	Data Enable Input (Active LOW)
6	G1	Data Enable Input (Active HIGH)
9, 10, 11, 12, 13, 14, 15, 7	Y0 to Y7	Multiplexer Outputs
8	GND	Ground (0V)
16	V _{CC}	Positive Supply Voltage

TRUTH TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{\text{GL}}$	G1	$\overline{\text{G2}}$	C	B	A	$\overline{\text{Y0}}$	$\overline{\text{Y1}}$	$\overline{\text{Y2}}$	$\overline{\text{Y3}}$	$\overline{\text{Y4}}$	$\overline{\text{Y5}}$	$\overline{\text{Y6}}$	$\overline{\text{Y7}}$
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Outputs corresponding to stored address L: all others H							

LOGIC DIAGRAM



This logic diagram has not be used to estimate propagation delays

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500(*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

(*) 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature	-55 to 125	°C
t_r, t_f	Input Rise and Fall Time ($V_{CC} = 4.5$ to $5.5V$)	0 to 500	ns

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value								Unit
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C			
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
V _{IH}	High Level Input Voltage	4.5 to 5.5		2.0			2.0		2.0		V	
V _{IL}	Low Level Input Voltage	4.5 to 5.5				0.8		0.8		0.8	V	
V _{OH}	High Level Output Voltage	4.5	I _O =-20 μA	4.4	4.5		4.4		4.4		V	
			I _O =-4.0 mA	4.18	4.31		4.13		4.10			
V _{OL}	Low Level Output Voltage	4.5	I _O =20 μA		0.0	0.1		0.1		0.1	V	
			I _O =4.0 mA		0.17	0.26		0.33		0.40		
I _I	Input Leakage Current	5.5	V _I = V _{CC} or GND			± 0.1		± 1		± 1	μA	
I _{CC}	Quiescent Supply Current	5.5	V _I = V _{CC} or GND			4		40		80	μA	
Δ I _{CC}	Additional Worst Case Supply Current	5.5	Per Input pin V _I = 0.5V or V _I = 2.4V Other Inputs at V _{CC} or GND I _O = 0			2.0		2.9		3.0	mA	

AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

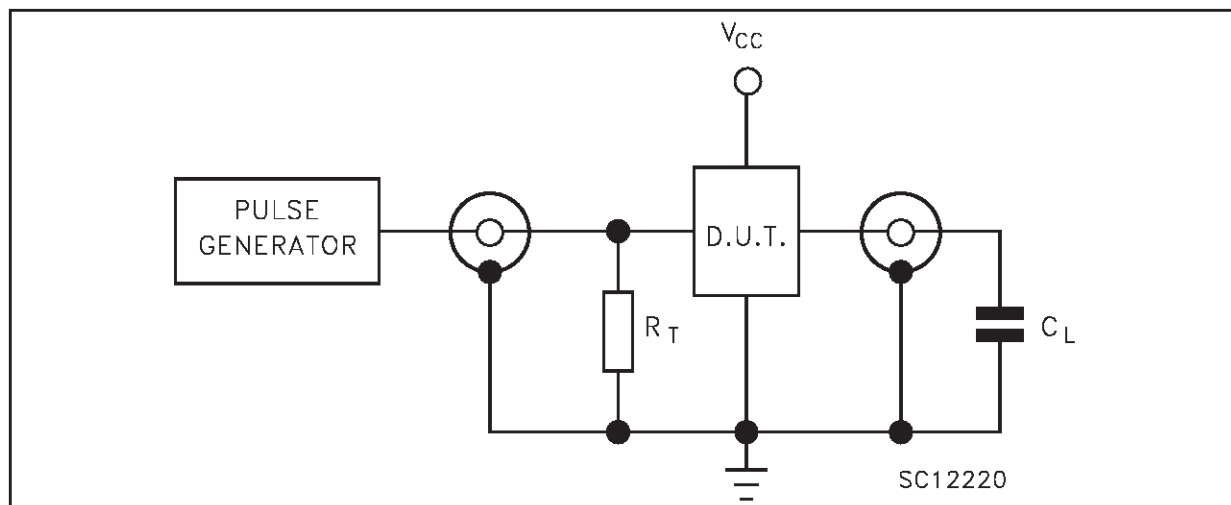
Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t _{TLH} t _{THL}	Output Transition Time	4.5			8	15		19		22	ns
t _{PLH} t _{PHL}	Propagation Delay Time (G1 - Y _n)	4.5			17	27		34		41	ns
t _{PLH} t _{PHL}	Propagation Delay Time (G2 - Y _n)	4.5			18	28		35		42	ns
t _{PLH} t _{PHL}	Propagation Delay Time (GL - Y _n)	4.5			25	39		49		59	ns
t _{PLH} t _{PHL}	Propagation Delay Time (A, B, C - Y)	4.5			24	37		46		56	ns
t _{W(H)} t _{W(L)}	Minimum Pulse Width (GL)	4.5			8	15		19		22	ns
t _s	Minimum Set-up Time (A, B, C - GL)	4.5				5		6		8	ns
t _h	Minimum Hold Time (A, B, C - GL)	4.5				5		6		8	ns

CAPACITIVE CHARACTERISTICS

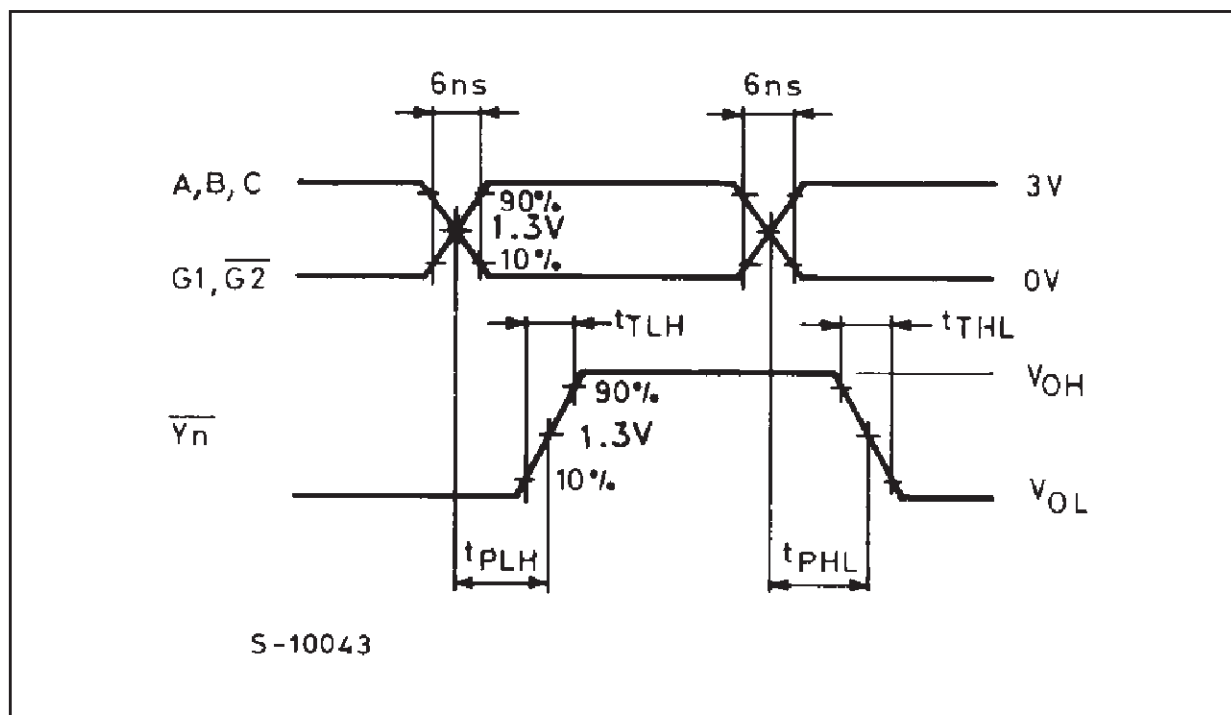
Symbol	Parameter	Test Condition		Value								Unit
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C			
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
C _{IN}	Input Capacitance				5	10		10		10	pF	
C _{PD}	Power Dissipation Capacitance (note 1)				58						pF	

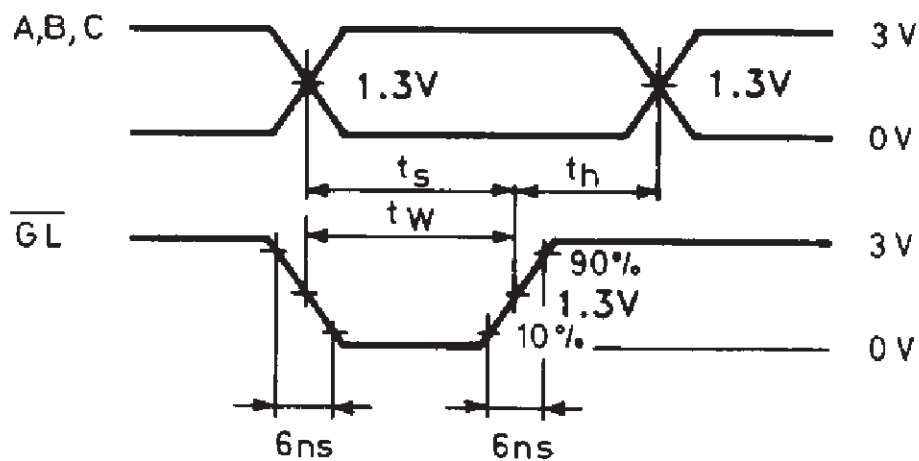
1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

TEST CIRCUIT



$C_L = 50\text{pF}$ or equivalent (includes jig and probe capacitance)
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

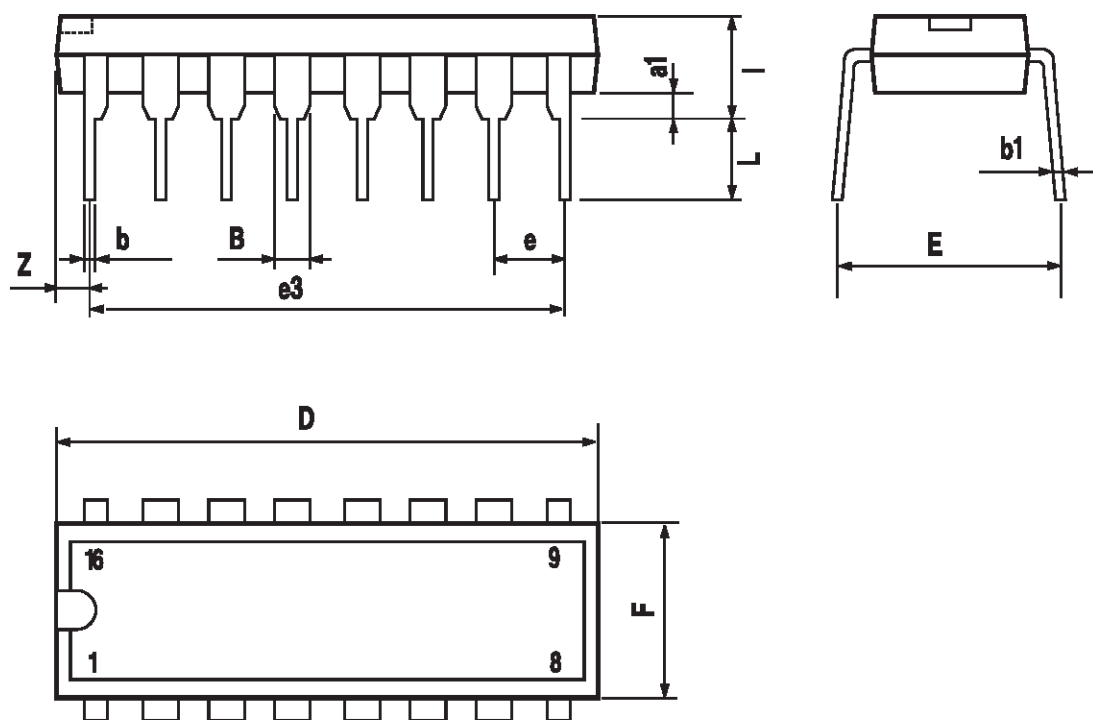
WAVEFORM 1 : PROPAGATION DELAY TIMES ($f=1\text{MHz}$; 50% duty cycle)

WAVEFORM 2 : MINIMUM PULSE WIDTH, SETUP AND HOLD TIME ($f=1\text{MHz}$; 50% duty cycle)

S-10044

Plastic DIP-16 (0.25) MECHANICAL DATA

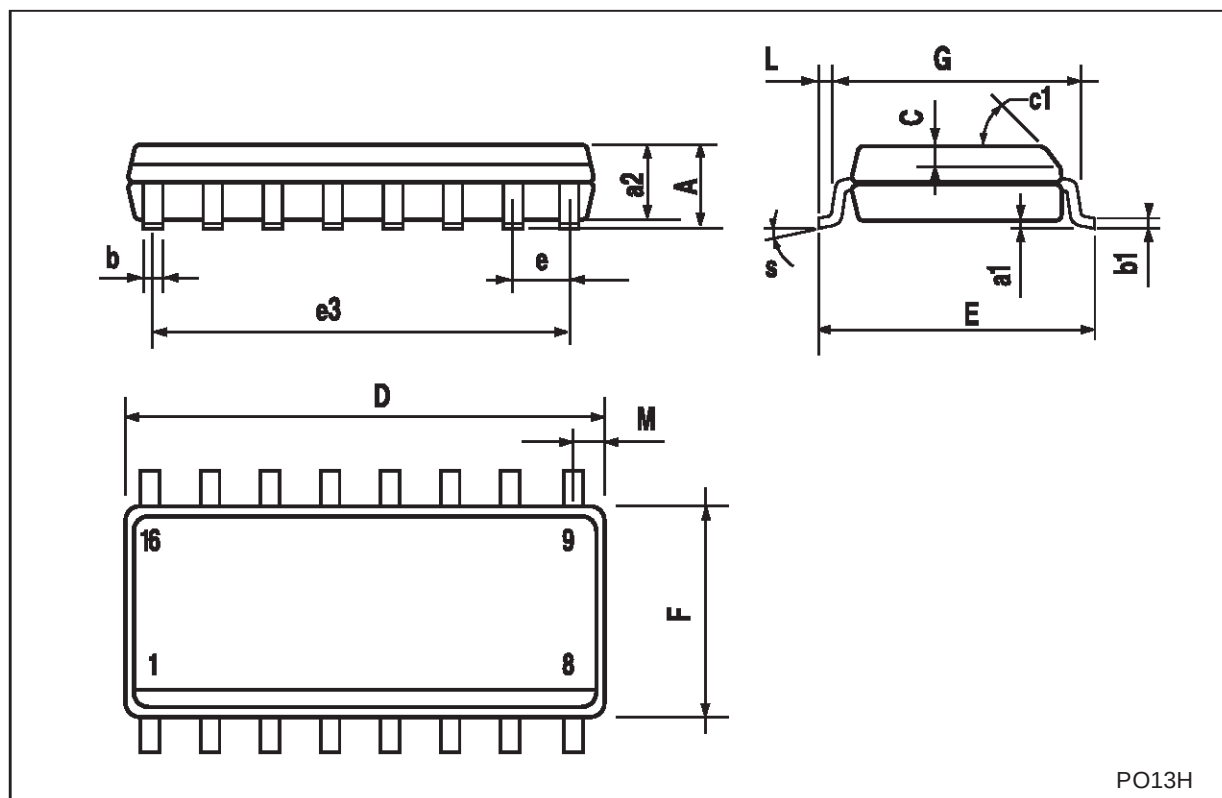
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

SO-16 MECHANICAL DATA

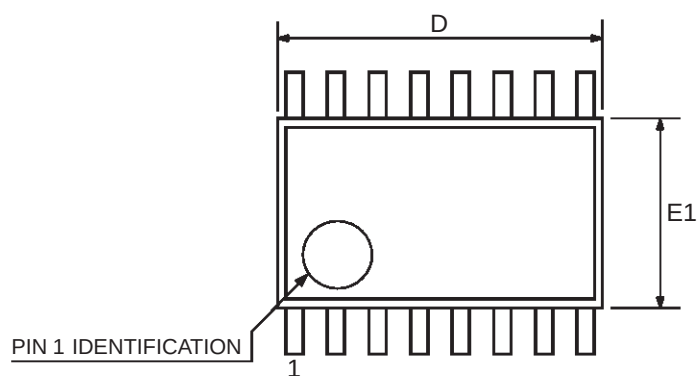
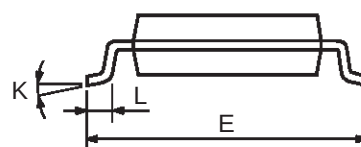
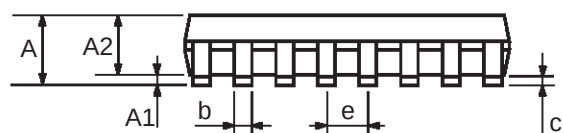
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PO13H

TSSOP16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



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