TPS793-Q1 Automotive, Ultra-Low Noise, High-PSRR, Fast RF, 200mA, Low-Dropout Linear Regulator

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
- Available in fixed and adjustable options
- High PSRR: 43dB at 100kHz (legacy chip)
- High PSRR: 39dB at 100kHz (new chip)
- Fast start-up time: 50µs (legacy chip)
- Internal 500µs soft-start time to reduce inrush current (new chip)
- Stable with a 2.2µF ceramic capacitor
- Very low dropout 112mV (typ) at full load
- Packages:
  - 6-pin SOT-23
  - 5-pin SOT-23

2 Applications

- Automotive head units
- Hybrid instrument clusters
- Telematics control units
- DC/DC converters

3 Description

The TPS793-Q1 is a low-dropout (LDO), low-power, linear voltage regulator. This device features high power-supply rejection ratio (PSRR), ultra-low noise, fast start-up, and excellent line and load transient response. The TPS793-Q1 is available in small-outline SOT-23 packages that sources 200mA.

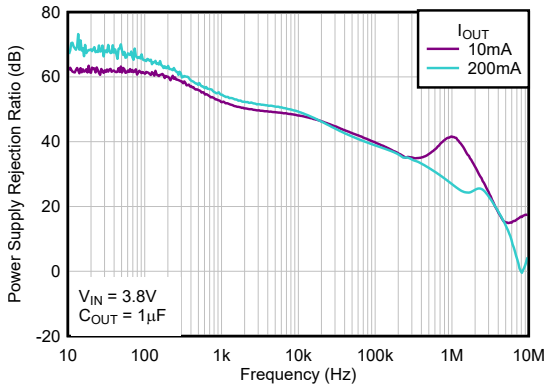
The TPS793-Q1 is designed for post-regulation applications, offering fixed and adjustable options supporting common voltage rails like 3.3V. The low noise and PSRR performance makes the device designed for power-sensitive analog loads.

The TPS793-Q1 offers foldback current limit to reduce power dissipation during overcurrent condition. The EN input helps with power-sequencing requirements of the system. The internal soft-start provides a controlled start-up, reducing inrush current and allowing lower input capacitance to be used.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS793-Q1	DBV (SOT-23, 6)	2.9mm × 2.8mm
	DBV (SOT-23, 5)	2.8mm × 2.8mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



TPS79328-Q1 Ripple Rejection vs Frequency (New Chip)

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4 Pin Configuration and Functions

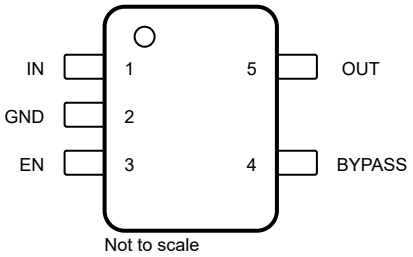


Figure 4-1. Fixed Option (Legacy Chip): DBV Package, 5-Pin SOT-23 (Top View)

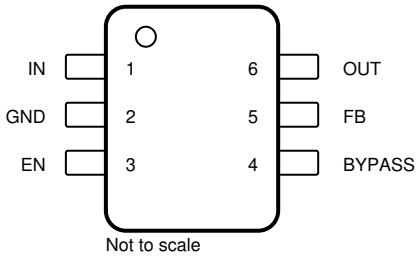


Figure 4-2. Adjustable Option (Legacy Chip): DBV Package, 6-Pin SOT-23 (Top View)

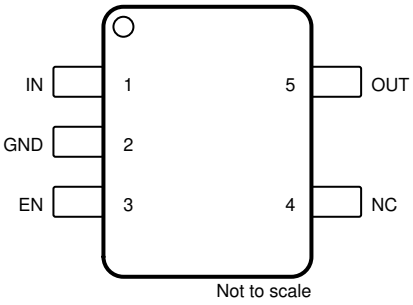


Figure 4-3. Fixed Option (New Chip): DBV Package, 5-Pin SOT-23 (Top View)

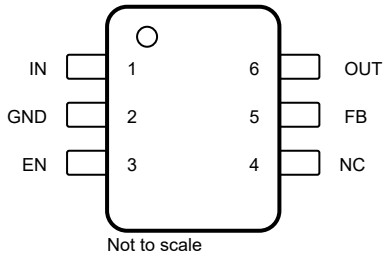


Figure 4-4. Adjustable Option (New Chip): DBV Package, 6-Pin SOT-23 (Top View)

Table 4-1. Pin Functions

PIN					TYPE	DESCRIPTION
NAME	ADJ (Legacy)	FIXED (Legacy)	ADJ (New)	FIXED (New)		
BYPASS	4	4	—	—	—	Legacy chip: An external bypass capacitor, connected to this pin and in conjunction with an internal resistor, creates a low-pass filter to further reduce regulator noise.
EN	3	3	3	3	I	Enable input that enables or shuts down the device. When EN goes to a logic high, the device is enabled. When the device goes to a logic low, the device is in shutdown mode.
FB	5	—	5	—	I	Feedback input voltage for the adjustable device
GND	2	2	2	2	—	Regulator ground
IN	1	1	1	1	I	Input to the device
NC	—	—	4	4	—	New chip: No connect pin. This pin is not internally connected. Connect to ground for best thermal performance or leave floating.
OUT	6	5	6	5	O	Regulated output of the device

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	V_{IN} , V_{EN}, V_{OUT} (Legacy Chip)	–0.3	6	V
	V_{IN} , V_{EN} (New Chip)	–0.3	6.5	V
	V_{OUT} (New Chip)	–0.3	V_{IN} + 0.3 (2)	
Current	Output, I_{OUT}	Internally limited		
Temperature	Operating junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The absolute maximum rating is V_{IN} + 0.3 V or 6.5 V, whichever is smaller.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011(2)	±250	
		Charged-device model (CDM), per AEC Q100-011(3)	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) Legacy Chip.
(3) New Chip.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.7		5.5	V
V_{EN}	Enable voltage	0		5.5	V
V_{OUT}	Output voltage	V_{FB}		5	V
I_{OUT}	Output current	0		200	mA
T_J	Operating junction temperature	–40		125	°C
C_{IN}	Input capacitor	0.1	1		µF
C_{OUT}	Output capacitor (Legacy Chip)	2.2(1)	10		µF
	Output capacitor (New Chip)	1(2)	10	200	
C_{NR}	Noise reduction capacitor(3)	0	10		nF
C_{FF}	Feed-forward capacitor (Legacy Chip)		15		pF
	Feed-forward capacitor (New Chip)(4)	0	10	100	nF
R_2	Lower feedback resistor (Legacy Chip)		30.1		kΩ
F_{EN}	Enable toggle frequency (New Chip)			10	kHz

(1) Legacy Chip only: if C_{FF} is not used or V_{OUT}(nom) < 1.8V, the minimum recommended C_{OUT} = 4.7µF.
(2) The minimum effective capacitance is 0.47 µF.
(3) Legacy Chip only. The New Chip does not have a Noise Reduction pin.
(4) Feed-forward capacitor is optional and not required for stability.

5.4 Thermal Information

THERMAL METRIC(1)		TPS793-Q1			UNIT
		DBV (SOT23-6)	DBV (SOT23-6)(2)	DBV (SOT23-5)(2)	
		6 PINS	6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	225.1	171.7	182.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.4	110.8	114.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.7	85.4	79.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.3	54.4	56.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	53.8	85.2	78.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(2) New Chip.

5.5 Electrical Characteristics

over recommended operating temperature range, T_J = –40°C to +125°C $V_{EN} = V_{IN}$, $V_{IN} = V_{O(typ)}$ + 1V, I_{OUT} = 1 mA, C_{OUT} = 10 µF, C_{NR} = 0.01 µF (Legacy Chip) (unless otherwise noted). All typical values at T_J= 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range			2.7		5.5	V
I_{OUT}	Continuous output current			0		200	mA
T_J	Operating junction temperature			-40		125	°C
V_{OUT}	Output voltage range	TPS79301-Q1		V_{FB}		5.5 – $V_{DROPOUT}$	V
		TPS79318-Q1	0µA < I_{OUT} < 200mA, 2.8V < V_{IN} < 5.5V	1.764	1.8	1.836	
		TPS79325-Q1	0µA < I_{OUT} < 200mA, 3.5V < V_{IN} < 5.5V	2.45	2.5	2.55	
		TPS79328-Q1	0µA < I_{OUT} < 200mA, 3.8V < V_{IN} < 5.5V	2.744	2.8	2.856	
		TPS79330-Q1 (legacy chip only)	0µA < I_{OUT} < 200mA, 4V < V_{IN} < 5.5V	2.94	3	3.06	
		TPS79333-Q1	0µA < I_{OUT} < 200mA, 4.3V < V_{IN} < 5.5V	3.234	3.3	3.366	
		TPS793475-Q1 (legacy chip only)	0µA < I_{OUT} < 200mA, 5.25V < V_{IN} < 5.5V	4.655	4.75	4.845	
I_{GND}	Quiescent current (GND current)	0µA ≤ I_O ≤ 200mA (Legacy Chip)			170	220	µA
		0µA ≤ I_O ≤ 200mA(New Chip)			250	1000	
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	0µA ≤ I_{OUT} ≤ 200mA			5		mV
$\Delta V_{OUT}/\Delta VIN$	Line regulation	V_{OUT} + 1V ≤ V_{IN} ≤ 5.5V			0.05	0.12	%/V
Vn	Output noise voltage TPS79328-Q1	BW = 100Hz to 100kHz, I_{OUT} = 200mA	C_{NR} = 0.001µF		55		μV_{RMS}
		BW = 100Hz to 100kHz, I_{OUT} = 200mA	C_{NR} = 0.0047µF		36		
		BW = 100Hz to 100kHz, I_{OUT} = 200mA	C_{NR} = 0.01µF		33		
		BW = 100Hz to 100kHz, I_{OUT} = 200mA	C_{NR} = 0.1µF		32		
		BW = 100Hz to 100kHz, I_{OUT} = 200mA	(New Chip)		69		
t_{STR}	Time, start-up (TPS79328-Q1)	R_L = 14 Ω, C_{OUT} = 1µF	C_{NR} = 0.001µF		50		µs
			C_{NR} = 0.0047µF		50		
			C_{NR} = 0.01µF		50		
			(New Chip)		500		

5.5 Electrical Characteristics (continued)

over recommended operating temperature range, T_J = –40°C to +125°C V_{EN} = V_{IN}, V_{IN} = $V_{O(typ)}$ + 1V, I_{OUT} = 1 mA, C_{OUT} = 10 µF, C_{NR} = 0.01 µF (Legacy Chip) (unless otherwise noted). All typical values at T_J= 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CL}	Output current limit	V_{OUT} = 0V(Legacy Chip)		285		600	mA
		V_{IN} = $V_{OUT(NOM)}$ + 1 V, V_{OUT} = 0.9 x $V_{OUT(NOM)}$ (New Chip only)		320		460	
I_{SC}	Short-circuit current limit	V_{OUT} = 0V (New Chip)			175		mA
I_{SHDN}	Shutdown current	V_{EN} = 0V, 2.7V < V_I < 5.5V(Legacy Chip)			0.07	1	µA
		V_{EN} = 0V, 2.7V < V_I < 5.5V(New Chip)			0.01	1	
$V_{EN(HI)}$	High-level enable input voltage	2.7V ≤ V_{IN} ≤ 5.5V		1.7		V_{IN}	V
		2.7V ≤ V_{IN} ≤ 5.5V (New Chip)		0.85		V_{IN}	
$V_{EN(LOW)}$	Low-level enable input voltage	2.7V ≤ V_{IN} ≤ 5.5V		0		0.7	V
		2.7V ≤ V_{IN} ≤ 5.5V (New Chip)		0		0.425	
I_{EN}	Enable pin current	V_{EN} = 0 V		–1		1	µA
I_{FB}	Feedback pin current	V_{FB} = 1.8V (Legacy Chip)				1	µA
		V_{FB} = 1.8V (New Chip)				0.05	
V_{REF}	Internal reference			1.201	1.225	1.25	V
PSRR	Power-supply rejection ratio (TPS79328-Q1)	f = 100Hz	I_{OUT} = 10mA (Legacy Chip)		70		dB
			I_{OUT} = 10mA (New Chip)		64		
			I_{OUT} = 200mA (Legacy Chip)		68		
			I_{OUT} = 200mA (New Chip)		65		
		f = 10kHz	I_{OUT} = 200mA (Legacy Chip)		70		
			I_{OUT} = 200mA (New Chip)		49		
		f = 100kHz	I_{OUT} = 200mA (Legacy Chip)		43		
			I_{OUT} = 200mA (New Chip)		39		
V_{DO}	Dropout voltage (TPS79328-Q1)	V_{IN}= V_{OUT} - 0.1V, I_{OUT} = 200mA			120	200	mV
	Dropout voltage (TPS793285-Q1) (legacy chip only)	V_{IN}= V_{OUT} - 0.1V, I_{OUT} = 200mA			120	200	
	Dropout voltage (TPS79330-Q1)	V_{IN}= V_{OUT} - 0.1V, I_{OUT} = 200mA			112	200	
	Dropout voltage (TPS79333-Q1)	V_{IN}= V_{OUT} - 0.1V, I_{OUT} = 200mA			112	180	
	Dropout voltage (TPS793475-Q1) (legacy chip only)	V_{IN}= V_{OUT} - 0.1V, I_{OUT} = 200mA			77	125	

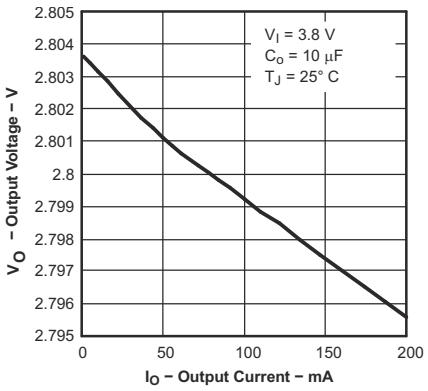
5.5 Electrical Characteristics (continued)

over recommended operating temperature range, T_J = –40°C to +125°C V_{EN} = V_{IN}, V_{IN} = $V_{O(typ)}$ + 1V, I_{OUT} = 1 mA, C_{OUT} = 10 µF, C_{NR} = 0.01 µF (Legacy Chip) (unless otherwise noted). All typical values at T_J= 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{UVLO}	UVLO threshold	V_{IN} rising (Legacy Chip)	2.25		2.65	V
		VIN rising (New Chip)	1.32		1.6	
$V_{UVLO(HYST)}$	UVLO hysteresis	T_J = 25°C, V_{CC} rising (Legacy Chip)		100		mV
		T_J = 25°C, V_{CC} rising (New Chip)		130		

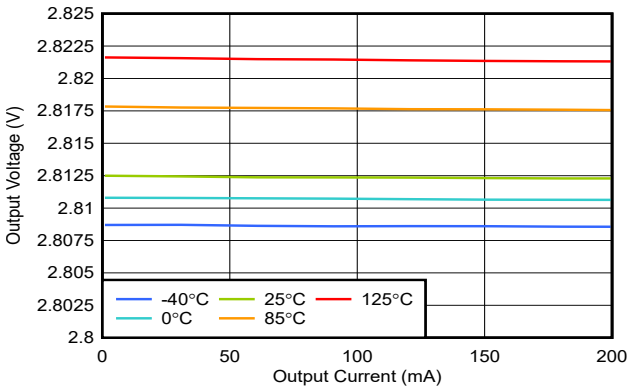
5.6 Typical Characteristics

over recommended operating temperature range, T_J = –40°C to +125°C $V_{EN} = V_{IN}$, $V_{IN} = V_{O(typ)}$ + 1V, I_{OUT} = 1mA, C_{OUT} = 10µF, C_{NR} = 0.01µF (legacy chip) (unless otherwise noted); all typical values at T_J = 25°C



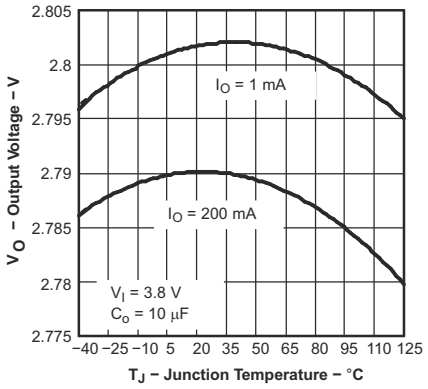
Legacy chip

Figure 5-1. TPS793-Q1 Output Voltage vs Output Current



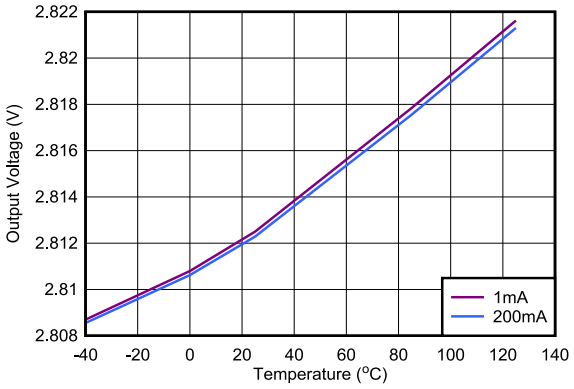
New chip

Figure 5-2. TPS793-Q1 Output Voltage vs Output Current



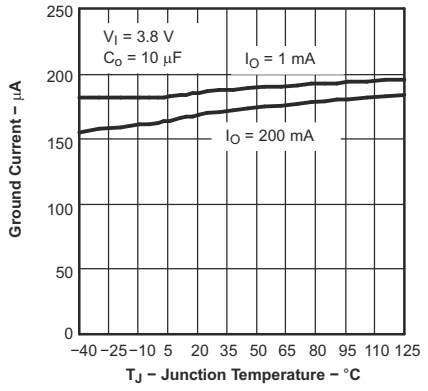
Legacy chip

Figure 5-3. TPS793-Q1 Output Voltage vs Junction Temperature



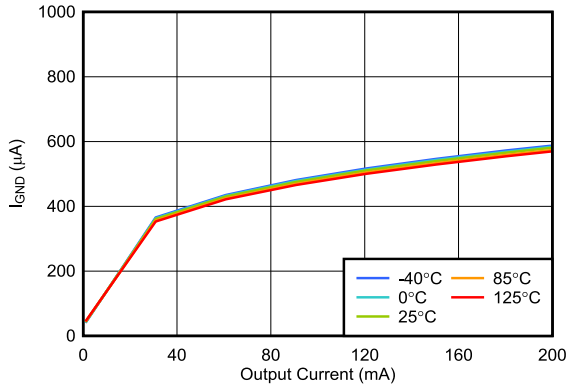
New chip

Figure 5-4. TPS793-Q1 Output Voltage vs Junction Temperature



Legacy chip

Figure 5-5. TPS793-Q1 Ground Current vs Junction Temperature

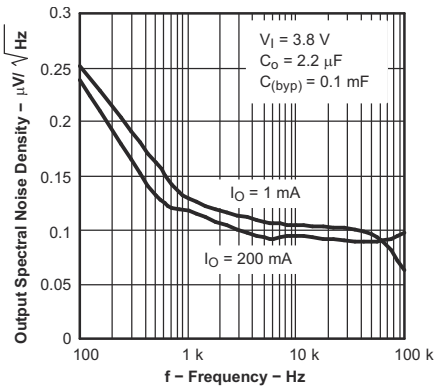


New chip

Figure 5-6. TPS793-Q1 Ground Current vs Junction Temperature

5.6 Typical Characteristics (continued)

over recommended operating temperature range, T_J = –40°C to +125°C $V_{EN} = V_{IN}$, $V_{IN} = V_{O(typ)}$ + 1V, I_{OUT} = 1mA, C_{OUT} = 10µF, C_{NR} = 0.01µF (legacy chip) (unless otherwise noted); all typical values at T_J = 25°C



Legacy chip

Figure 5-7. TPS793-Q1 Output Spectral Noise Density vs Frequency

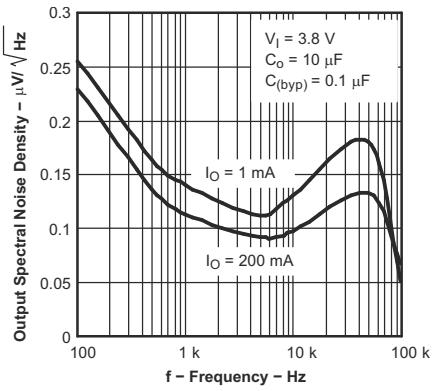


Figure 5-8. TPS793-Q1 Output Spectral Noise Density vs Frequency

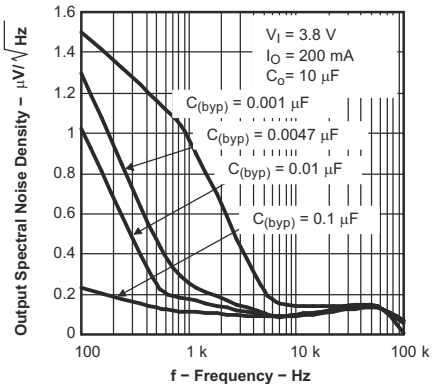
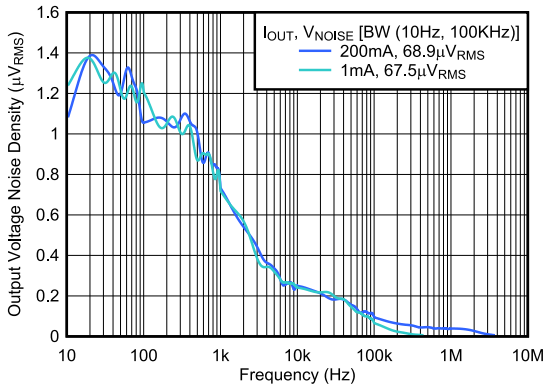
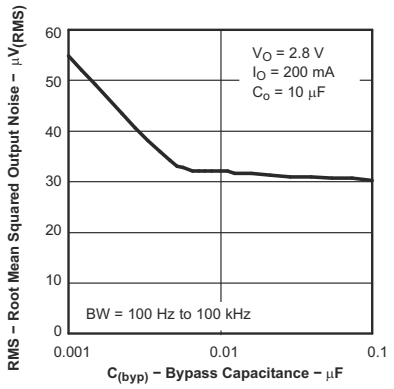


Figure 5-9. TPS793-Q1 Output Spectral Noise Density vs Frequency



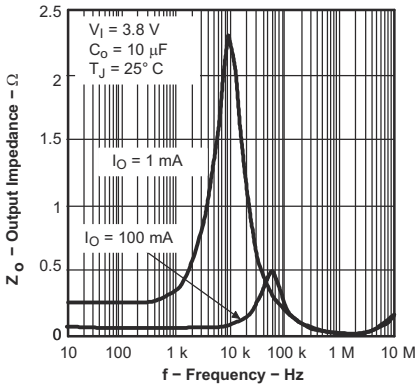
C_{OUT} = 10uF (new chip)

Figure 5-10. TPS793-Q1 Output Spectral Noise Density vs Frequency



Legacy chip

Figure 5-11. Root Mean Squared Output Noise vs Bypass Capacitance



Legacy chip

Figure 5-12. Output Impedance vs Frequency

5.6 Typical Characteristics (continued)

over recommended operating temperature range, T_J = –40°C to +125°C V_{EN} = V_{IN}, V_{IN} = $V_{O(typ)}$ + 1V, I_{OUT} = 1mA, C_{OUT} = 10µF, C_{NR} = 0.01µF (legacy chip) (unless otherwise noted); all typical values at T_J = 25°C

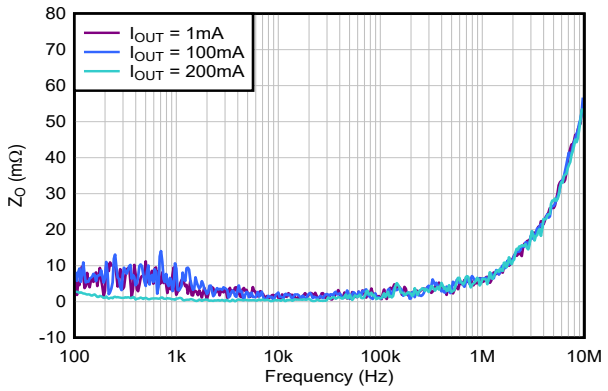


Figure 5-13. Output Impedance vs Frequency

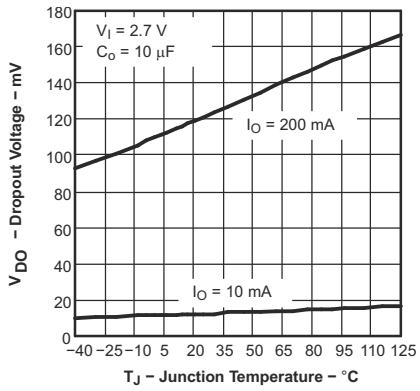


Figure 5-14. TPS793-Q1 Dropout Voltage vs Junction Temperature

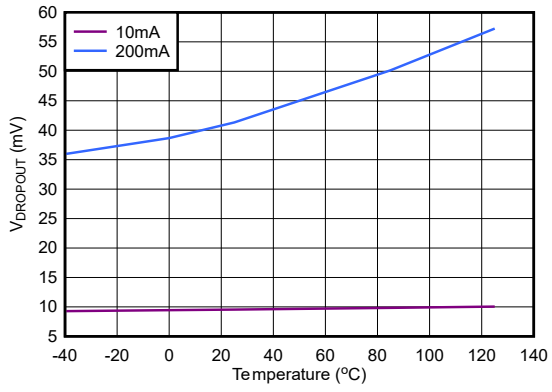


Figure 5-15. TPS793-Q1 Dropout Voltage vs Junction Temperature

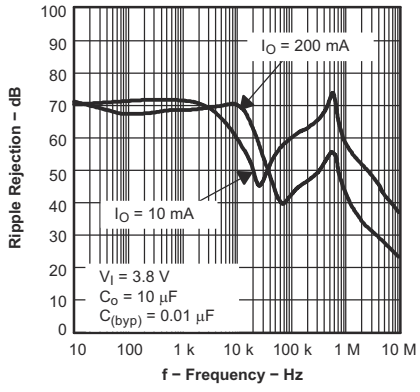


Figure 5-16. TPS793-Q1 Ripple Rejection vs Frequency

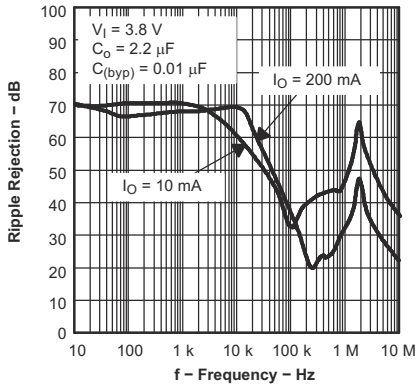


Figure 5-17. TPS793-Q1 Ripple Rejection vs Frequency

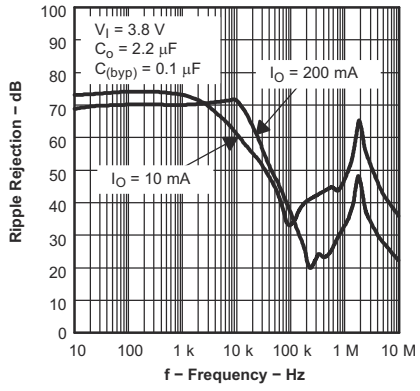


Figure 5-18. TPS793-Q1 Ripple Rejection vs Frequency

5.6 Typical Characteristics (continued)

over recommended operating temperature range, T_J = –40°C to +125°C V_{EN} = V_{IN}, V_{IN} = $V_{O(typ)}$ + 1V, I_{OUT} = 1mA, C_{OUT} = 10µF, C_{NR} = 0.01µF (legacy chip) (unless otherwise noted); all typical values at T_J = 25°C

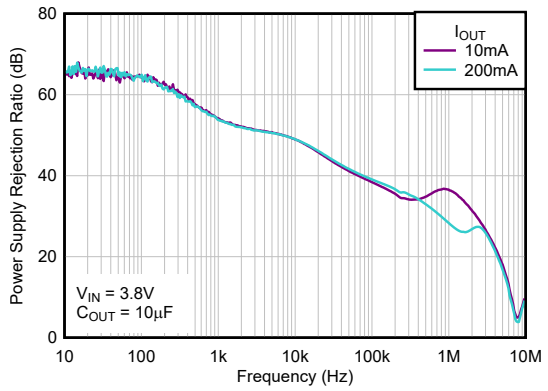


Figure 5-19. TPS793-Q1 Ripple Rejection vs Frequency

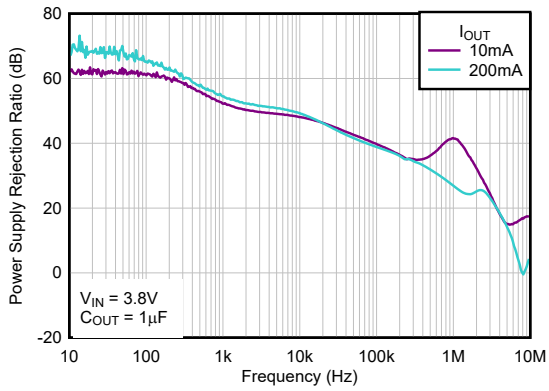


Figure 5-20. TPS793-Q1 Ripple Rejection vs Frequency

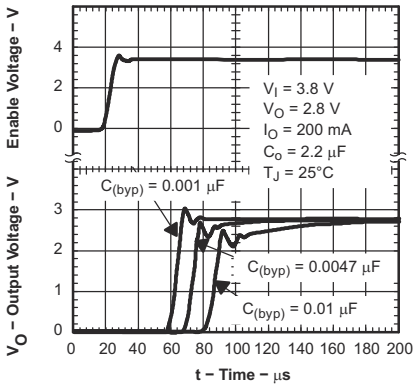


Figure 5-21. TPS793-Q1 Output Voltage and Enable Voltage vs Time (Start-Up)

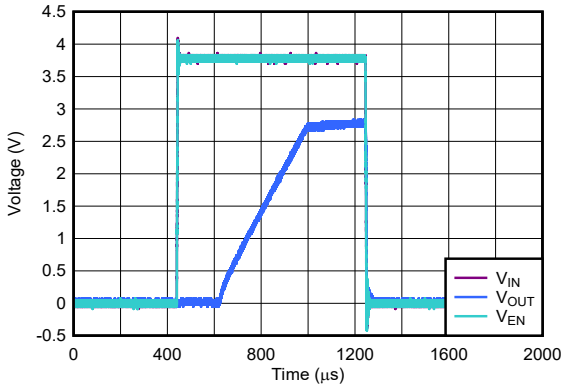


Figure 5-22. TPS793-Q1 Output Voltage, Enable Voltage vs Time (Start-Up)

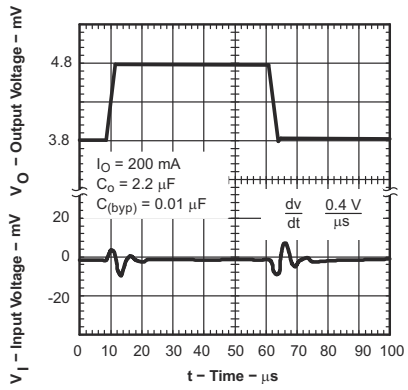


Figure 5-23. TPS793-Q1 Line Transient Response

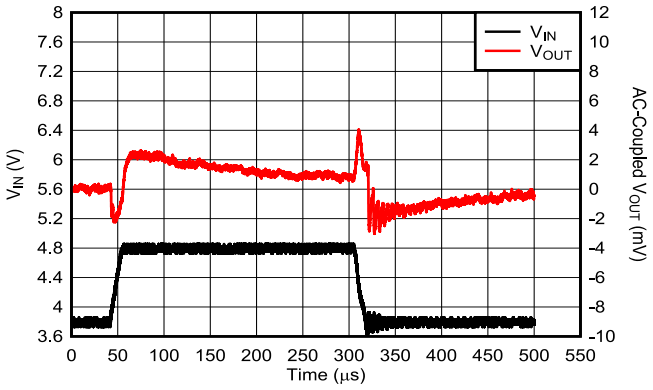
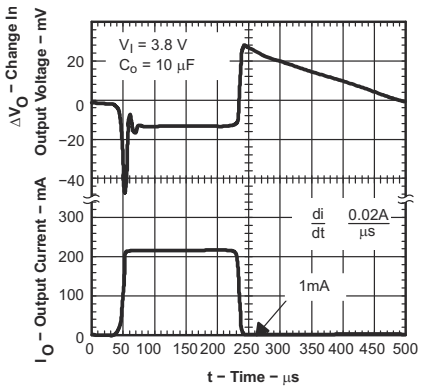


Figure 5-24. TPS793 Line Transient Response

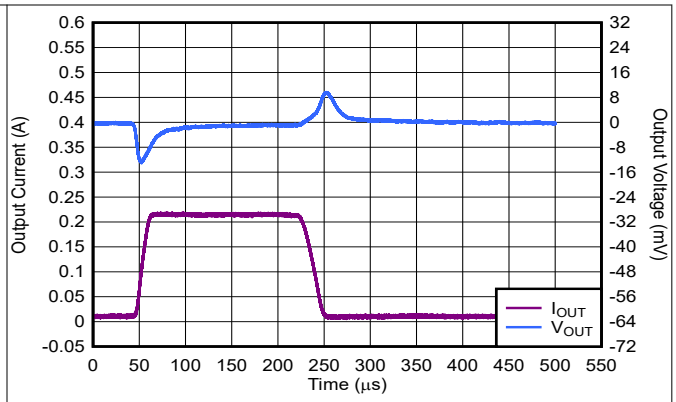
5.6 Typical Characteristics (continued)

over recommended operating temperature range, T_J = –40°C to +125°C V_{EN} = V_{IN}, V_{IN} = $V_{O(typ)}$ + 1V, I_{OUT} = 1mA, C_{OUT} = 10µF, C_{NR} = 0.01µF (legacy chip) (unless otherwise noted); all typical values at T_J = 25°C



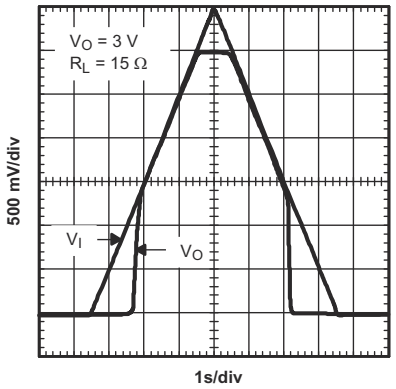
Legacy chip

Figure 5-25. TPS793-Q1 Load Transient Response



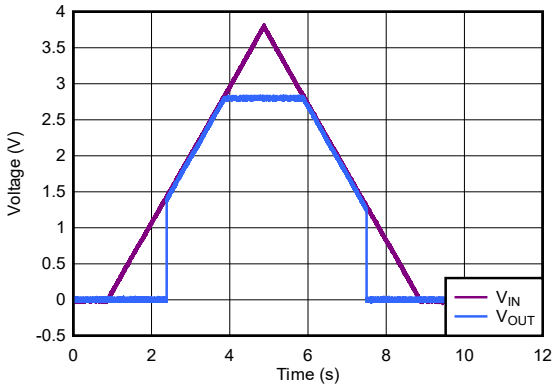
New chip, C_{OUT} = 10uF, dI/dt = 0.02A/µs

Figure 5-26. TPS79328 Load Transient Response



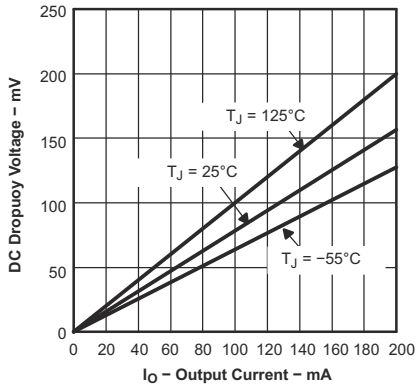
Legacy chip

Figure 5-27. Power-Up and Power-Down



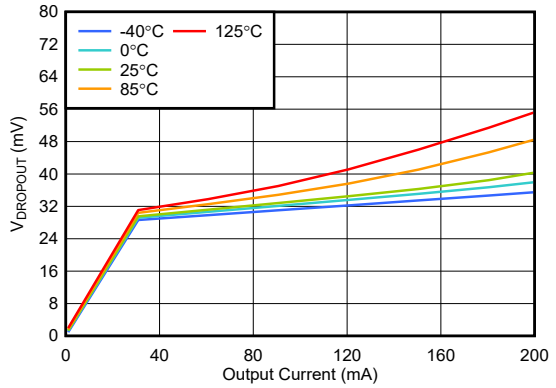
New chip

Figure 5-28. Power-Up and Power-Down



Legacy chip

Figure 5-29. Dropout Voltage vs Output Current

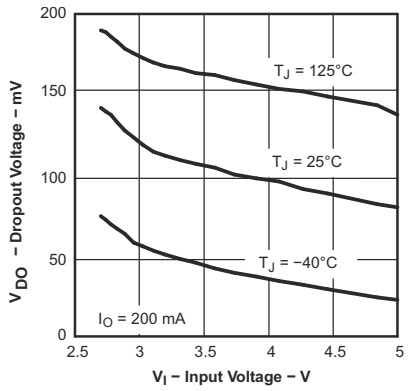


New chip

Figure 5-30. Dropout Voltage vs Output Current

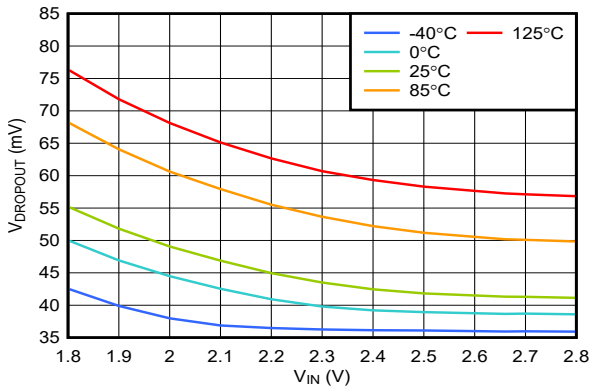
5.6 Typical Characteristics (continued)

over recommended operating temperature range, T_J = –40°C to +125°C $V_{EN} = V_{IN}$, $V_{IN} = V_{O(typ)}$ + 1V, I_{OUT} = 1mA, C_{OUT} = 10µF, C_{NR} = 0.01µF (legacy chip) (unless otherwise noted); all typical values at T_J = 25°C



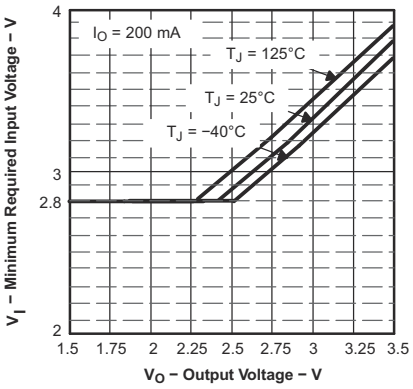
Legacy chip

Figure 5-31. TPS793-Q1 Dropout Voltage vs Input Voltage



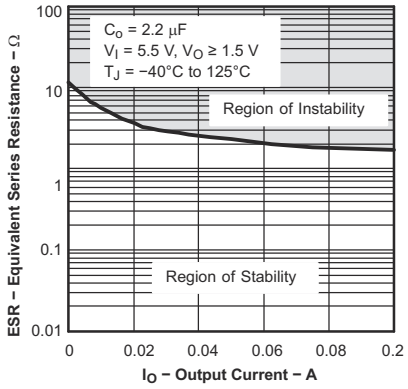
New chip, I_{OUT} = 200mA

Figure 5-32. TPS793-Q1 Dropout Voltage vs Input Voltage



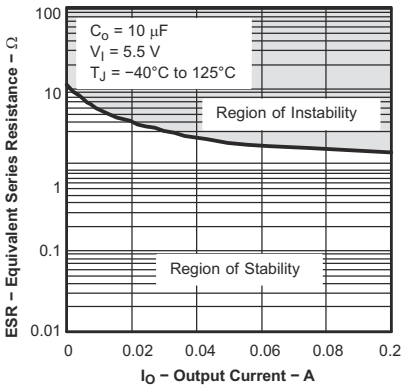
Legacy chip

Figure 5-33. Minimum Required Input Voltage vs Output Voltage



Legacy chip

Figure 5-34. Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current



Legacy chip

Figure 5-35. Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

6 Detailed Description

6.1 Overview

The TPS793-Q1 is a low-dropout, high PSRR, high-accuracy linear voltage regulator optimized for use in noise-sensitive, battery-operated equipment with excellent transient performance. These characteristics make the device designed for most automotive applications.

This regulator offers current limit, output enable, active discharge, undervoltage lockout (UVLO), and thermal protection.

6.2 Functional Block Diagrams

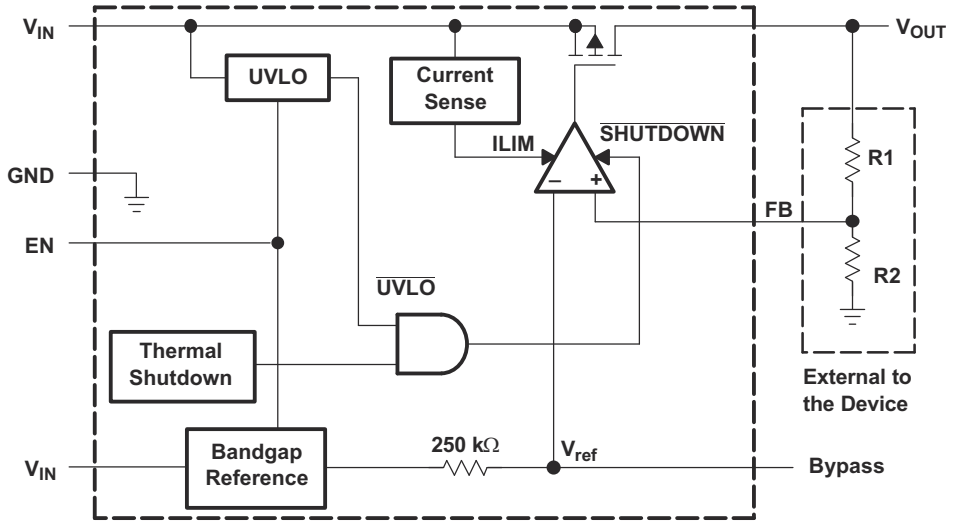


Figure 6-1. Adjustable Version (Legacy Chip)

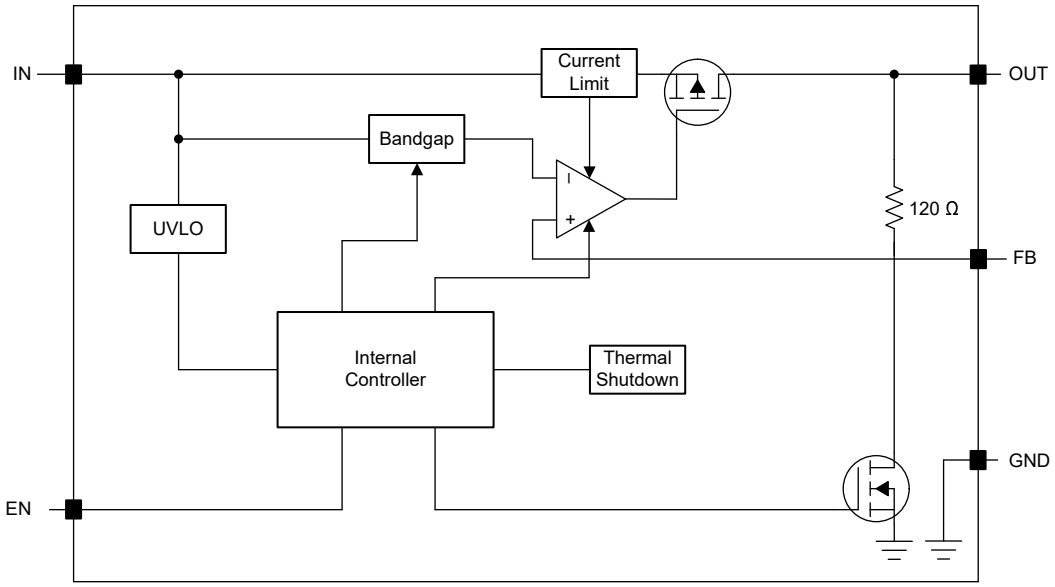


Figure 6-2. Adjustable Version (New Chip)

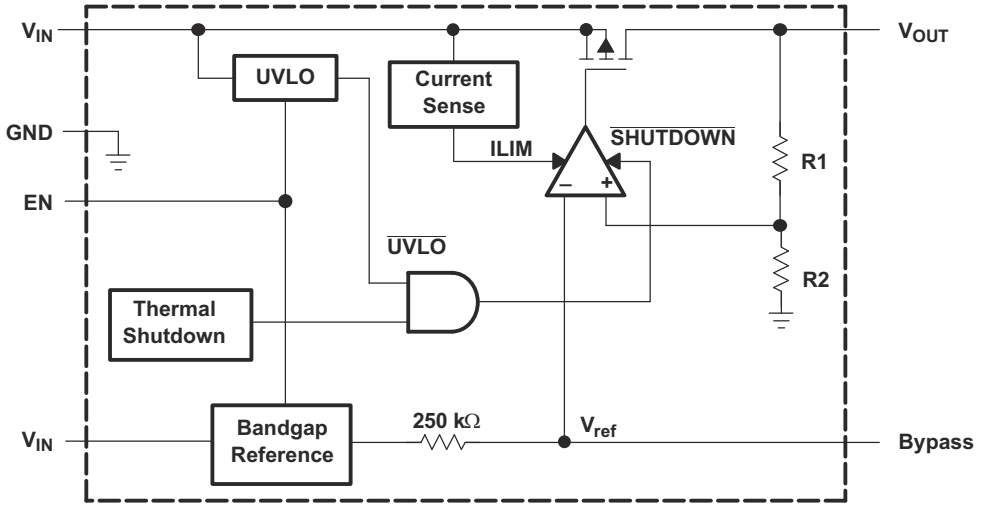


Figure 6-3. Fixed Version (Legacy Chip)

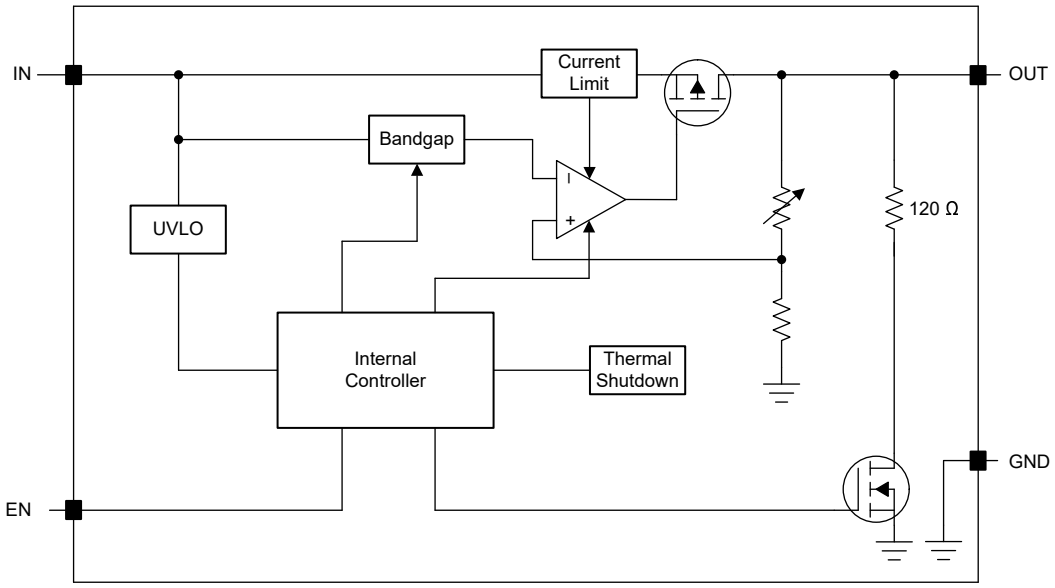


Figure 6-4. Fixed Version (New Chip)

6.3 Feature Description

6.3.1 Undervoltage Lockout (UVLO)

The TPS793-Q1 uses an undervoltage lockout (UVLO) circuit that disables the output until the input voltage is greater than the rising UVLO voltage. This circuit makes sure the device does not exhibit unpredictable behavior when the supply voltage is lower than the operational range of the internal circuitry, $V_{IN(min)}$.

The UVLO circuit makes sure that the device stays disabled before the input supply reaches the minimum operational voltage range, and makes sure that the device shuts down when the input supply collapses. Figure 6-5 shows the UVLO circuit response to various input voltage events. The diagram can be separated into the following parts:

- Region A: The device does not start until the input reaches the UVLO rising threshold.
- Region B: Normal operation, regulating device.
- Region C: Brownout event above the UVLO falling threshold (UVLO rising threshold – UVLO hysteresis). The output may fall out of regulation but the device remains enabled.
- Region D: Normal operation, regulating device.
- Region E: Brownout event below the UVLO falling threshold. The device is disabled in most cases and the output falls because of the load and active discharge circuit. The device is reenabled when the UVLO rising threshold is reached by the input voltage and a normal start-up follows.
- Region F: Normal operation followed by the input falling to the UVLO falling threshold.
- Region G: The device is disabled when the input voltage falls below the UVLO falling threshold to 0 V. The output falls because of the load and active discharge circuit.

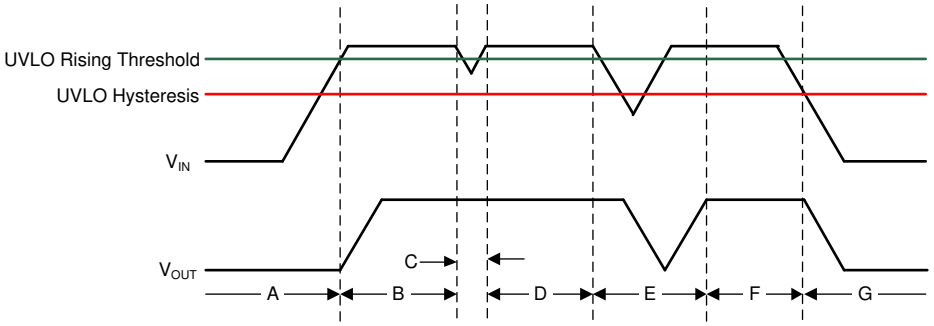


Figure 6-5. Typical UVLO Operation

6.3.2 Shutdown

The enable pin (EN) is active high. Enable the device by forcing the EN pin to exceed $V_{EN(high)}$. Turn off the device by forcing the EN pin to drop below the maximum EN pin low-level input voltage (see the *Electrical Characteristics* table). If shutdown capability is not required, connect EN to IN.

6.3.3 Foldback Current Limit

The TPS793-Q1 features internal current limiting and thermal protection. During normal operation, the TPS793-Q1 limits output current to approximately 400mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. Although current limiting is designed to prevent gross device failure, take care not to exceed package power dissipation ratings or device absolute maximum voltage ratings.

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brick-wall-foldback scheme. The current limit transitions from a brick-wall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brick-wall scheme limits the output current to the current limit (I_{CL}). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current as the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the short-circuit current limit (I_{SC}). I_{CL} and I_{SC} are listed in the *Electrical Characteristics* table.

For this device, $V_{FOLDBACK} = 0.4 \times V_{OUT(NOM)}$.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{CL}]. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{SC}]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application note.

Figure 6-6 shows a diagram of the foldback current limit.

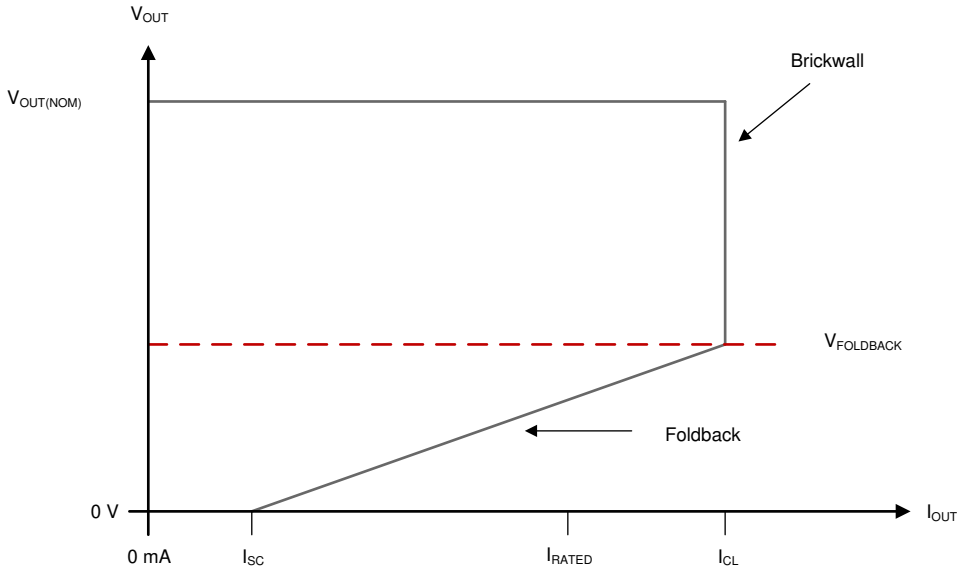


Figure 6-6. Foldback Current Limit

6.3.4 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 165°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit cycles on and off. This cycling limits regulator dissipation, protecting the device from damage as a result of overheating. Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, limit junction temperature to 125°C maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered. Use worst-case loads and signal conditions.

The TPS793-Q1 internal protection circuitry is designed to protect against overload conditions. This circuitry is not intended to replace proper heat sinking. Continuously running the TPS793-Q1 into thermal shutdown degrades device reliability.

6.3.5 Reverse Current Operation

The TPS793-Q1 legacy chip PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage. For example, during power down. Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended.

The TPS793-Q1 new chip, as with most modern LDOs, excessive reverse current damages this device.

Reverse current flows through the body diode on the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device as a result of one of the following conditions:

- Degradation caused by electromigration
- Excessive heat dissipation
- Potential for a latch-up condition

Conditions where reverse current occurs are outlined in this section, all of which potentially exceed the absolute maximum rating of $V_{OUT} > V_{IN} + 0.3V$:

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, use external protection to protect the device. Figure 6-7 shows one approach of protecting the device.

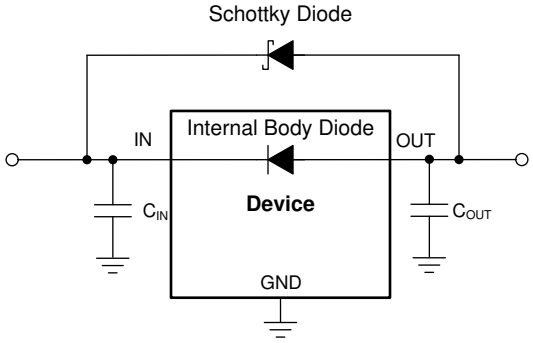


Figure 6-7. Example Circuit for Reverse Current Protection Using a Schottky Diode

6.4 Device Functional Modes

Table 6-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

Table 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	— (TBD the template shows $I_{OUT} < I_{OUT(max)}$)	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{EN(LOW)}$	Not applicable	$T_J > T_{SD(shutdown)}$ (1)

(1) Approximate value for thermal shutdown

6.4.1 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is at least as high as $V_{IN(min)}$
- The input voltage is greater than the nominal output voltage added to the dropout voltage
- The enable voltage is greater than $V_{EN(min)}$
- The output current is less than the current limit
- The device junction temperature is less than the maximum specified junction temperature

6.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, the device operates in dropout mode. However, make sure all other conditions are met for normal operation. In this mode of operation, the output voltage is the same as the input voltage minus the dropout voltage. The device transient performance is significantly degraded because the pass transistor is in the linear region and no longer controls the current through the LDO. Line or load transients in dropout potentially result in large output voltage deviations.

6.4.3 Disabled

The device is disabled under the following conditions:

- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold
- The device junction temperature is greater than the thermal shutdown temperature
- The input voltage is less than $UVLO_{falling}$

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TPS793-Q1 low-dropout (LDO) regulator is optimized for use in noise-sensitive, battery-operated equipment. The device features extremely low dropout voltages, high PSRR, ultra-low output noise, low quiescent current, and enable input. These features help reduce supply currents when the regulator is turned off.

7.1.1 Exiting Dropout

Some applications have transients that place the LDO into dropout, such as slower ramps on V_{IN} during start-up. As with other LDOs, the output potentially overshoots on recovery from these conditions. Figure 7-1 shows that a ramping input supply causes an LDO to overshoot on start-up. This condition occurs when the slew rate and voltage levels are in the correct range. Use an enable signal to avoid this condition.

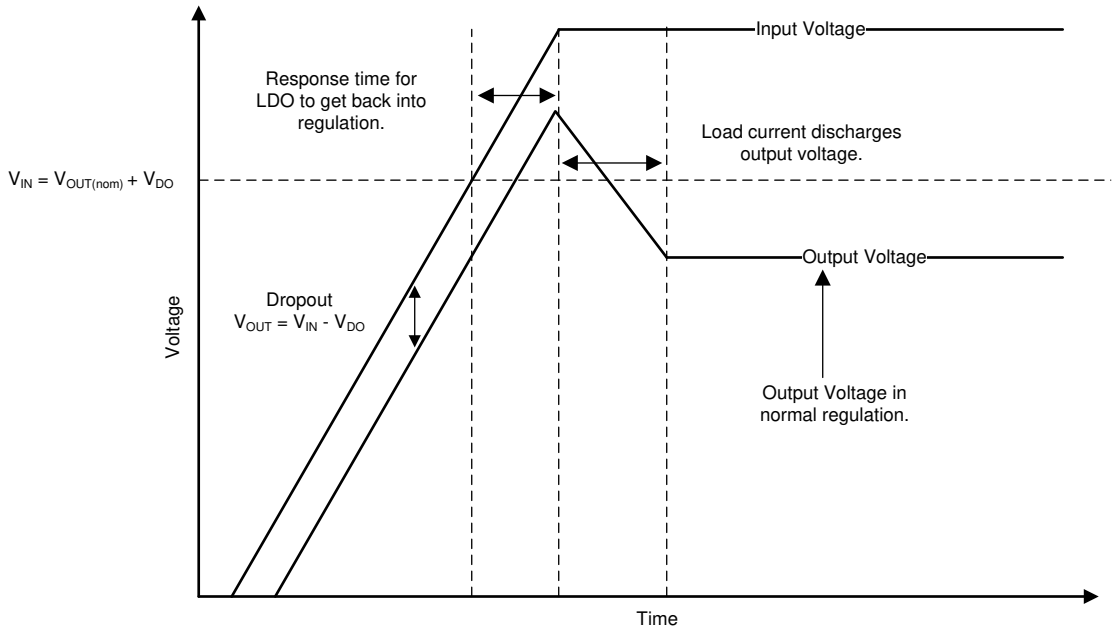


Figure 7-1. Start-Up Into Dropout

Line transients out of dropout also cause overshoot on the output of the regulator. These overshoots are caused by the error amplifier having to drive the gate capacitance of the pass transistor. Subsequently, the error amplifier then brings the gate back to the correct voltage for proper regulation. Figure 7-2 illustrates what is happening internally with the gate voltage and how overshoot is caused during operation. When the LDO is placed in dropout, the gate voltage (V_{GS}) is pulled to ground to give the pass transistor the lowest on-resistance possible. However, if a line transient occurs when the device is in dropout, the loop is not in regulation. This condition causes the output to overshoot until the loop responds and the output current pulls the output voltage back down into regulation. If these transients are not acceptable, then continue to add input capacitance in the system until the transient is slow enough to reduce the overshoot.

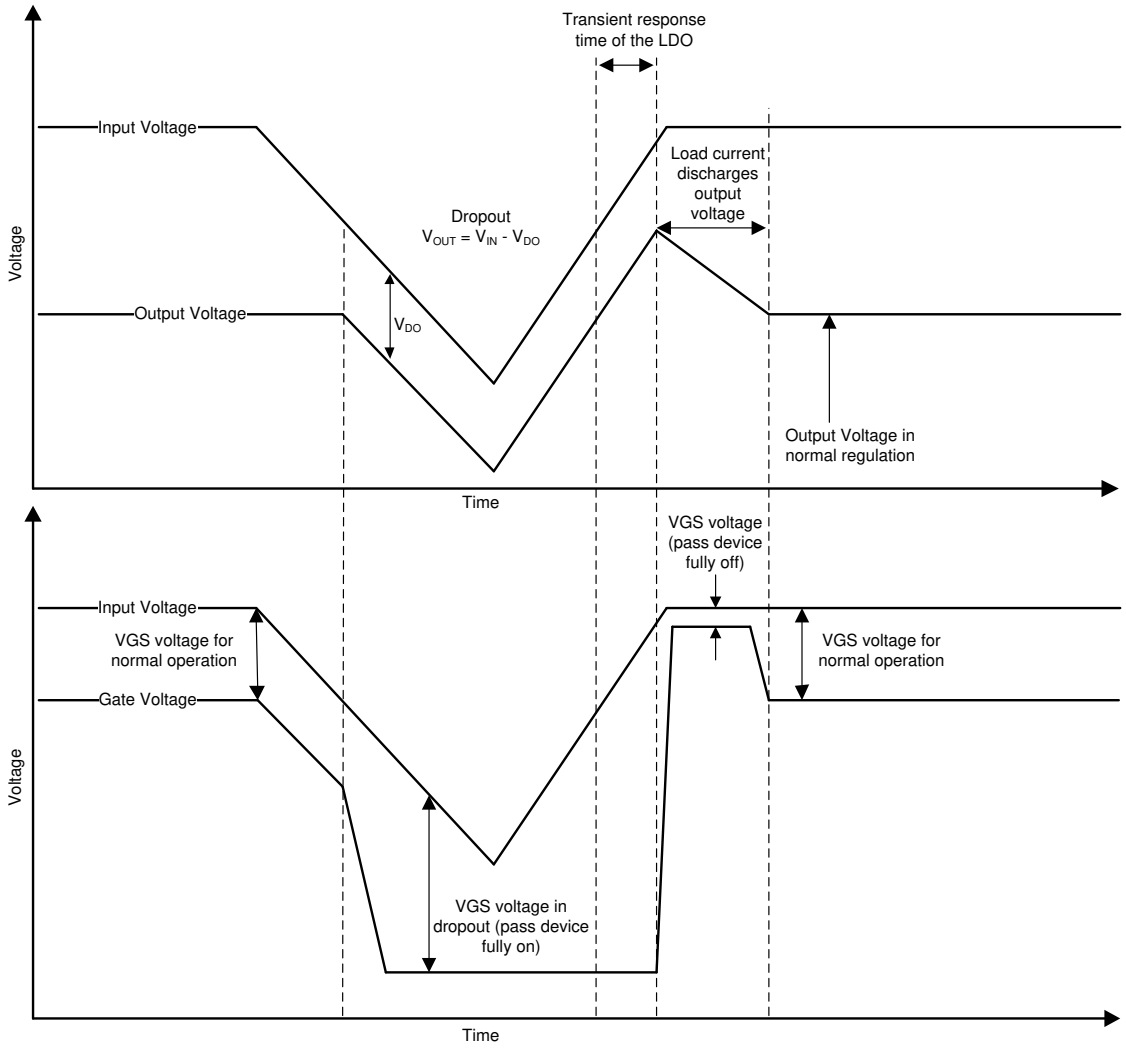


Figure 7-2. Line Transients From Dropout

7.2 Typical Application

Figure 7-3 and Figure 7-4 show typical application circuits for the legacy chip and new chip, respectively.

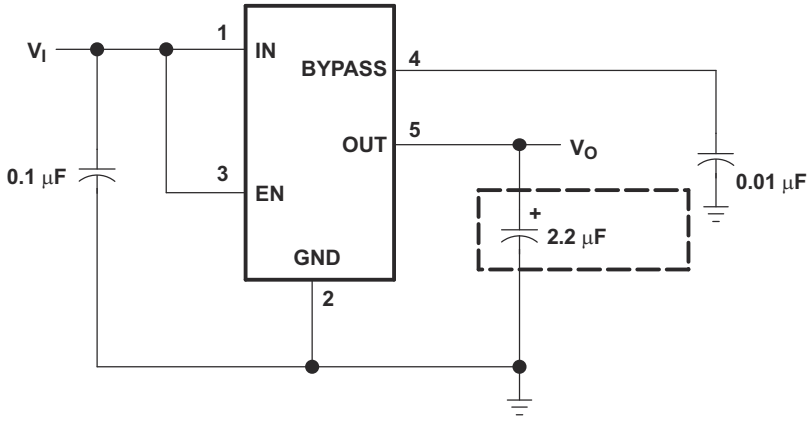


Figure 7-3. Typical Application Circuit (Legacy chip)

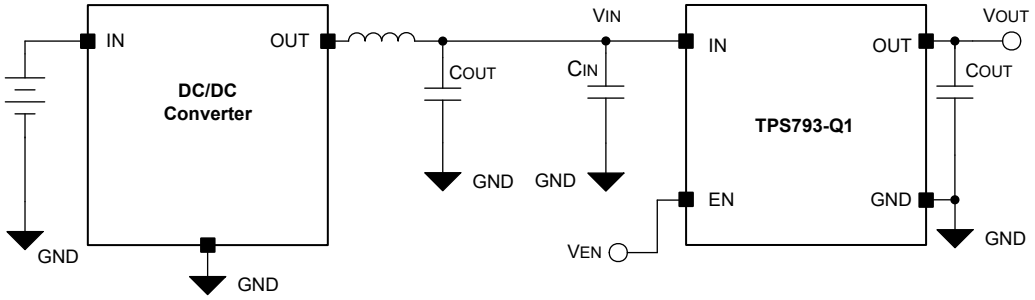


Figure 7-4. Typical Application Circuit (New Chip)

7.2.1 Design Requirements

Table 7-1 lists the design requirements.

Table 7-1. Design Parameters

PARAMETER	DESIGN REQUIREMENTS
Input voltage	3V – 4V
Output voltage	2.8V
DC output current	10mA
Peak output current	75mA
Maximum ambient temperature	65°C

7.2.2 Detailed Design Procedure

7.2.2.1 External Capacitor Requirements

A 0.1µF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS793-Q1, is required for stability. This capacitor improves transient response, noise rejection, and ripple rejection. A higher-value electrolytic input capacitor is necessary if large, fast, rise-time load transients are anticipated and the device is located several inches from the power source.

The TPS793-Q1 requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitor for the legacy chip is 2.2µF. The minimum recommended capacitance for the new chip is 0.47µF. Any 2.2µF or larger ceramic capacitor is permissible, provided the capacitance does not vary significantly over temperature.

The internal voltage reference is a key source of noise in an LDO regulator. The TPS793-Q1 (legacy chip) has a BYPASS pin that is connected to the voltage reference through a 250kΩ internal resistor. The 250kΩ internal resistor, in conjunction with an external bypass capacitor connected to the BYPASS pin, creates a low pass filter. This filter reduces the voltage reference noise and, therefore, the noise at the regulator output. For the regulator to operate properly, make sure the current flow out of the BYPASS pin is at a minimum. Any leakage current creates an IR drop across the internal resistor, thus creating an output error. Therefore, make sure the bypass capacitor has minimal leakage current.

7.2.2.2 Adjustable Operation

Figure 7-5 shows how the output voltage of the TPS79301-Q1 adjustable regulator is programmed with an external resistor divider. The output voltage is calculated using Equation 1.

$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

where:

- V_{ref} = 1.225V typical (the internal reference voltage)

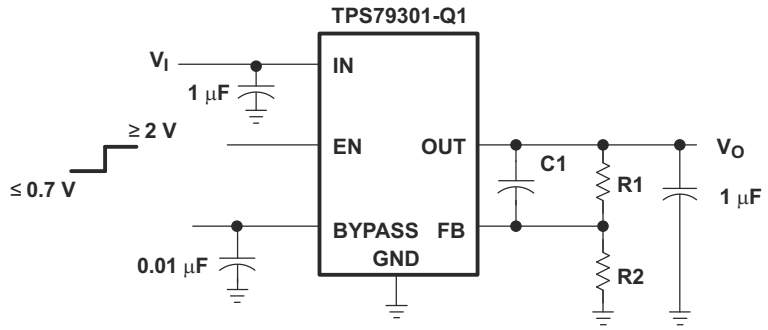


Figure 7-5. TPS79301-Q1 Adjustable LDO Regulator Programming

7.2.2.2.1 Adjustable Operation (Legacy Chip)

Choose resistors R1 and R2 for approximately a 50µA divider current. Using lower-value resistors improves noise performance, but the solution consumes more power. Avoid higher resistor values because leakage current from FB across R1 and R2 creates an offset voltage that artificially increases or decreases the feedback voltage. Thus, causing output voltage (V_O) to erroneously decrease or increase. The recommended design procedure is to choose R2 = 30.1kΩ to set the divider current at 50µA. Set C1 = 15pF for stability, then calculate R1 with the following equation.

$$R1 = \left(\frac{V_O}{V_{ref}} - 1 \right) \times R2 \tag{2}$$

To improve the stability of the adjustable version, place a small compensation capacitor between the OUT and FB (feed-forward capacitor) pins. For voltages <1.8V, make sure the value of this capacitor is 100pF. For voltages >1.8V, the following equation calculates the approximate value of this capacitor.

$$C1 = \frac{(3 \times 10^{-7}) \times (R1 + R2)}{(R1 \times R2)} \tag{3}$$

Table 7-2 lists the suggested value of this capacitor for several resistor ratios. If this capacitor is not used (such as in a unity-gain configuration) or if an output voltage <1.8V is chosen, use a larger output capacitor. The minimum recommended output capacitor in this case is 4.7µF instead of 2.2µF.

Table 7-2. Output Voltage Programming Guide

OUTPUT VOLTAGE	R1	R2	C1
2.5V	31.6kΩ	30.1kΩ	22pF
3.3V	51kΩ	30.1kΩ	15pF
3.6V	59kΩ	30.1kΩ	15pF

7.2.2.2.2 Adjustable Operation (New Chip)

To disregard the effect of the FB pin current and achieve best accuracy, choose R2 to be equal to or smaller than 550kΩ. Make sure the current flowing through R1 and R2 is at least 100 times larger than the I_{FB} current listed in the *Electrical Characteristics* table. Lowering the value of R2 increases the immunity against noise injection. Increasing the value of R2 reduces the quiescent current for achieving higher efficiency at low load currents. The following equation calculates the setting that provides the maximum feedback divider series resistance.

$$(R1 + R2) \leq V_{OUT} / (I_{FB} \times 100) \tag{4}$$

7.2.3 Application Curves

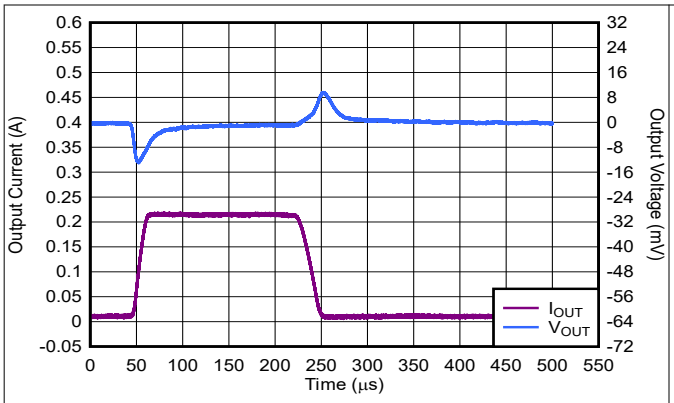


Figure 7-6. TPS793-Q1 Load Transient Response

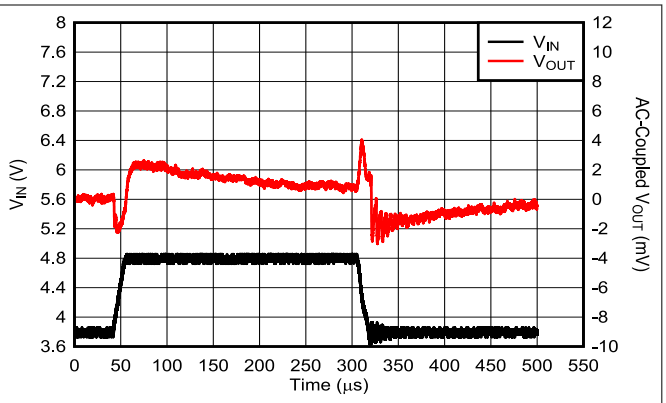


Figure 7-7. TPS793-Q1 Line Transient Response

7.3 Power Supply Recommendations

This device is designed to operate from an input voltage supply range from 2.7V to 5.5V. Make sure the input voltage range provides adequate headroom for the device to have a regulated output. Make sure this input supply is well-regulated and stable. A 0.1µF input capacitor is required for stability. If the input supply is noisy, additional input capacitors with low ESR helps improve the output noise performance.

7.4 Layout

7.4.1 Layout Guidelines

Layout is a critical part of good power-supply design. There are several signal paths that conduct fast-changing currents or voltages that interact with stray inductance or parasitic capacitance, generating noise or degrading power-supply performance. To help eliminate these problems, bypass the IN pin to ground with a low ESR ceramic bypass capacitor with an X5R or X7R dielectric.

Minimize equivalent series inductance (ESL) and equivalent series resistance (ESR) to maximize performance and provide stability. Place each capacitor (C_{IN}, C_{OUT}, C_{NR}, C_{FF}) as close as possible to the device and on the same side of the PCB as the regulator. Do not place any capacitors on the opposite side of the PCB from where the regulator is installed. Using vias and long traces is strongly discouraged because these circuits potentially impact system performance negatively, and even cause instability.

7.4.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve ac measurements such as PSRR, output noise, and transient response, design the board with separate ground planes for V_{IN} and V_{OUT}. Connect each ground plane only at the GND pin of the device.

7.4.1.2 Power Dissipation and Junction Temperature

Specified regulator operation is to a junction temperature of 125°C; restrict the maximum junction temperature to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator handles in any given application. To make sure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D. Make sure both $P_{D(max)}$ and P_D are less than or equal to $P_{D(max)}$.

The maximum power dissipation limit is determined using the following equation.

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}} \quad (5)$$

where:

- $T_J$max = Maximum allowable junction temperature
- $R_{\theta JA}$ = Thermal resistance, junction to ambient, for the package, see the *Thermal Information* table
- T_A = Ambient temperature

The regulator dissipation is calculated with the following equation.

$$P_D = (V_I - V_O) \times I_O \quad (6)$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.

7.4.2 Layout Example

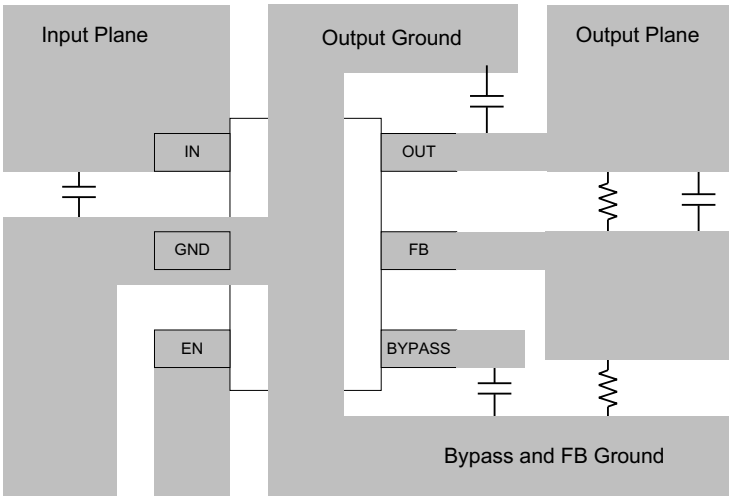


Figure 7-8. Layout Example (DBV 6-Pin Package, Legacy Chip)

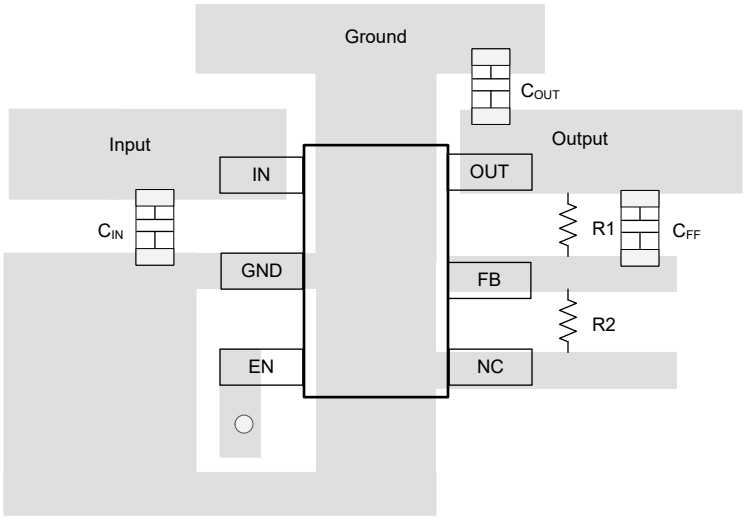


Figure 7-9. Layout Example (DBV 6-Pin Package, New Chip)

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 Evaluation Modules

Multiple evaluation modules (EVMs) are available to assist in the initial circuit performance evaluation using the TPS793-Q1:

- TPS79301EVM
- TPS79328EVM
- DEM-SOT23LDO

Request these EVMs at the Texas Instruments web site through the device product folders or purchase directly from the TI eStore.

8.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS793 is available through the product folders under *Tools & Software*.

8.1.2 Device Nomenclature

Table 8-1. Available Options

PRODUCT(1)	DESCRIPTION
TPS793**xxyyyzM3Q1**	**xx(x)** is the nominal output voltage (for example, 28 = 2.8V; 285 = 2.85V; 01 = Adjustable version). **yyy** is the package designator. **z** is the package quantity. **M3**is a suffix designator for devices that only use the latest manufacturing flow (CSO: RFB). Devices without this suffix ship with the legacy chip (CSO: DLN) or the new chip (CSO: RFB). The reel packaging label provides CSO information to distinguish which chip is being used. The device performance for new and legacy chips is denoted throughout the document. **Q1** indicates that this device is an automotive grade (AEC-Q100) device.

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Using New Thermal Metrics* application note
- Texas Instruments, *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application note
- Texas Instruments, *TPS79301EVM, TPS79328EVM LDO Linear Regulator Evaluation Module* user's guide

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

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All trademarks are the property of their respective owners.

8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (March 2016) to Revision J (June 2025) — **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document ... 1
- Added new silicon (M3) devices to document ... 1
- Added new chip DBV package (fixed and adjustable versions) to document ... 1
- Changed entire document to identify the features and differences of the legacy chip and new chip and the adjustable and fixed versions of the device ... 1
- Changed *Features*, *Applications*, and *Description* sections ... 1
- Changed *Description* section to match new chip information, deleted legacy chip *Output Spectral Noise Density vs Frequency* curve ... 1
- Deleted *Voltage Options* table ... 3
- Added new chip curves to *Typical Characteristics* section to show side-by-side comparison with legacy chip curves ... 9
- Changed *Overview* section ... 15
- Changed *Functional Block Diagram* section ... 15
- Changed *Undervoltage Lockout (UVLO)* section ... 17
- Changed discussion of EN pin in *Shutdown* section ... 17
- Changed *Foldback Current Limit* section ... 17
- Changed *Reverse Current Operation* section ... 18
- Deleted *Regulator Protection* section ... 18
- Changed *Device Functional Mode Comparison* table ... 20
- Deleted *(170 µA typically)* from low quiescent current discussion in *Application Information* section ... 21
- Added *Exiting Dropout* section ... 21
- Added *Typical Application Circuit (New Chip)* figure ... 22
- Deleted *(Lithium Ion battery)* from input voltage row of *Design Parameters* table ... 23
- Deleted last paragraph of *External Capacitor Requirements* section ... 23
- Changed *Adjustable Operation* section and title ... 23
- Changed *Application Curves* section ... 25
- Added new chip information to *Device Nomenclature* table ... 27

Changes from Revision H (January 2013) to Revision I (January 2016) — **Page**

- Changed document part numbers to the generic TPS793-Q1 ... 1
- Removed the 2.85-V version from the data sheet ... 1

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS79301DBVRG4Q1	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGV1
TPS79301DBVRG4Q1.A	Active	Production	null (null) |	3000 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	See TPS79301DBVRG4Q1	PGV1
TPS79301DBVRQ1	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGV1
TPS79301DBVRQ1.A	Active	Production	null (null) |	3000 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	See TPS79301DBVRQ1	PGV1
TPS79318DBVRG4Q1	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 125	PHH1
TPS79318DBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHH1
TPS79318DBVRQ1.A	Active	Production	null (null) |	3000 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	See TPS79318DBVRQ1	PHH1
TPS79325DBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGW1
TPS79325DBVRQ1.A	Active	Production	null (null) |	3000 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	See TPS79325DBVRQ1	PGW1
TPS79328QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGX1
TPS79328QDBVRQ1.A	Active	Production	null (null) |	3000 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	See TPS79328QDBVRQ1	PGX1
TPS79330QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGY1
TPS79330QDBVRQ1.A	Active	Production	null (null) |	3000 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	See TPS79330QDBVRQ1	PGY1
TPS79333DBVRG4Q1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHU1
TPS79333DBVRG4Q1.A	Active	Production	null (null) |	3000 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	See TPS79333DBVRG4Q1	PHU1
TPS79333DBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHU1
TPS79333DBVRQ1.A	Active	Production	null (null) |	3000 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	See TPS79333DBVRQ1	PHU1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TPS793-Q1 :

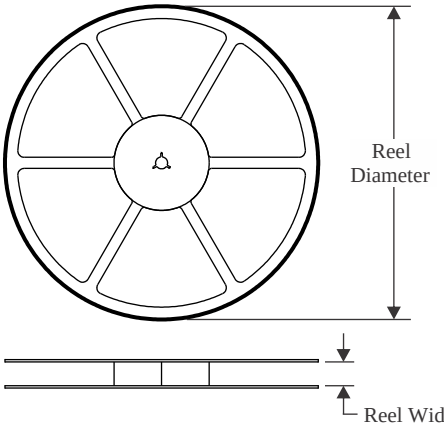
- Catalog : TPS793

NOTE: Qualified Version Definitions:

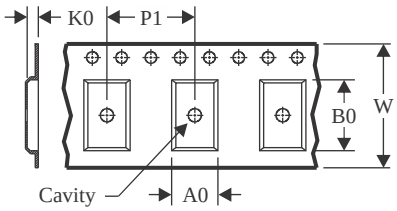
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

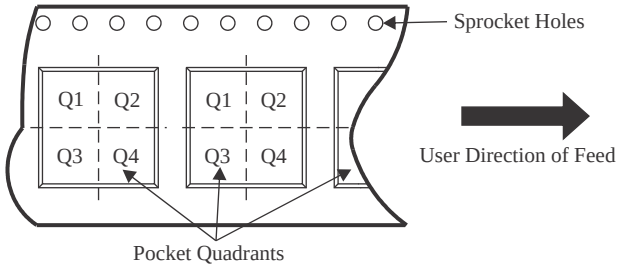


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

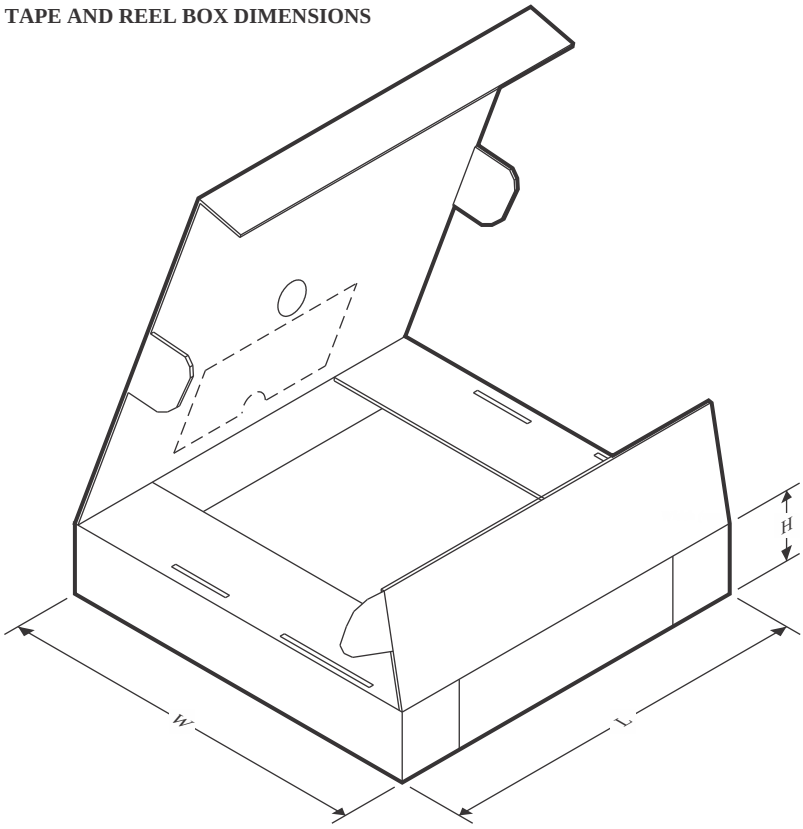
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79301DBVRG4Q1	SOT-23	DBV	6	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS79301DBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS79318DBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS79325DBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS79328QDBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79330QDBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79333DBVRG4Q1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS79333DBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

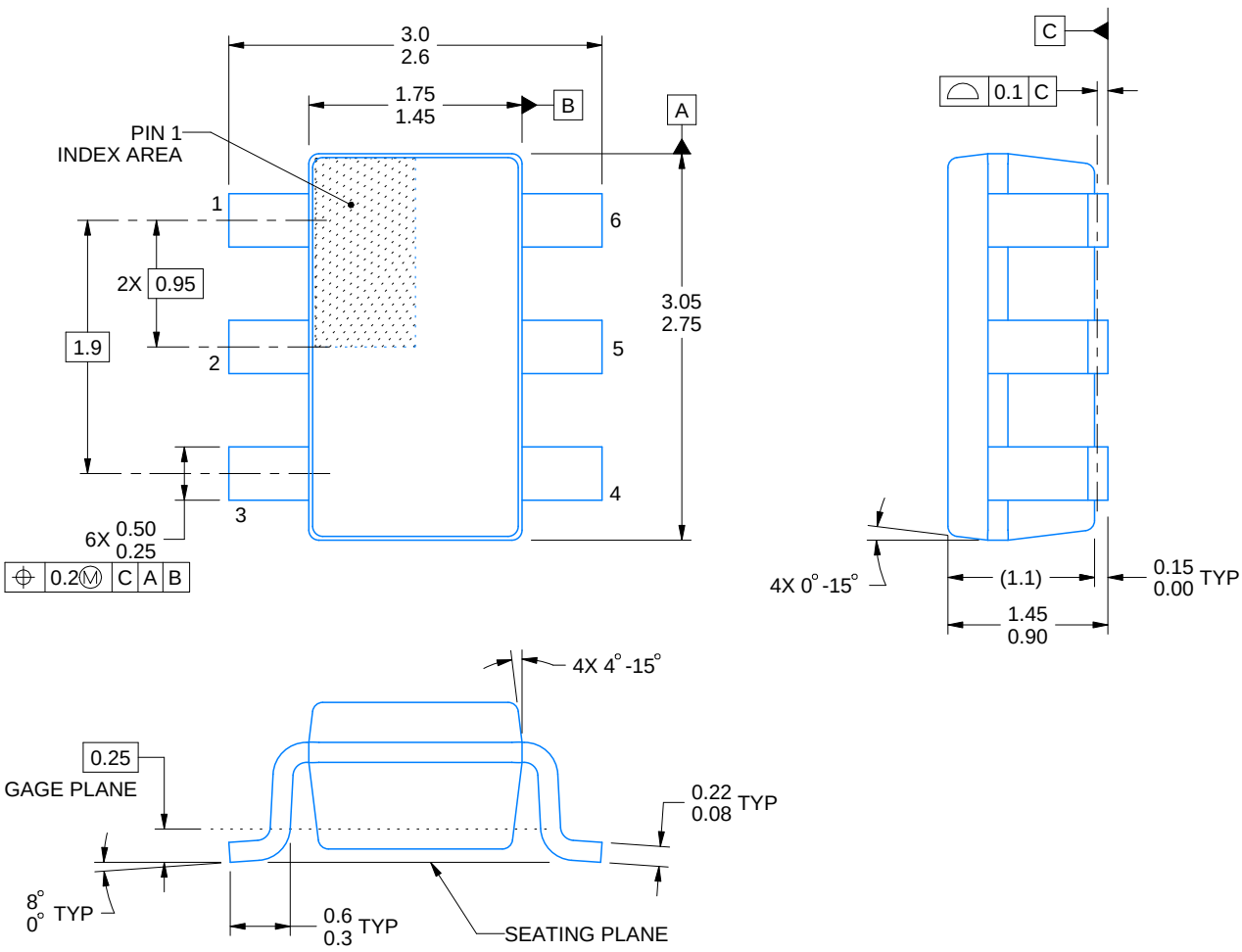
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS79301DBVRG4Q1	SOT-23	DBV	6	3000	445.0	220.0	345.0
TPS79301DBVRQ1	SOT-23	DBV	6	3000	445.0	220.0	345.0
TPS79318DBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS79325DBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS79328QDBVRQ1	SOT-23	DBV	5	3000	200.0	183.0	25.0
TPS79330QDBVRQ1	SOT-23	DBV	5	3000	200.0	183.0	25.0
TPS79333DBVRG4Q1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS79333DBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

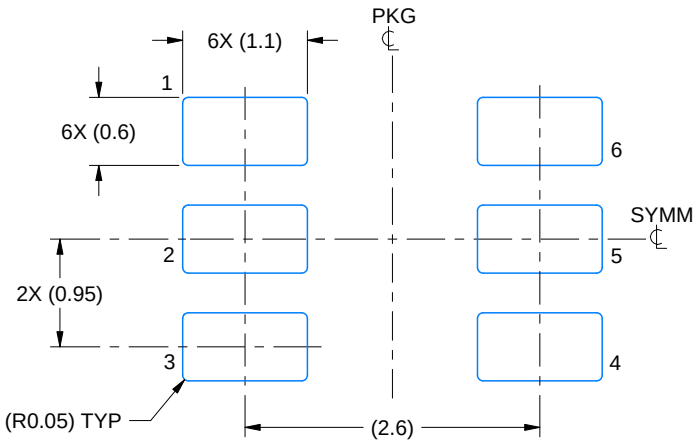
SMALL OUTLINE TRANSISTOR



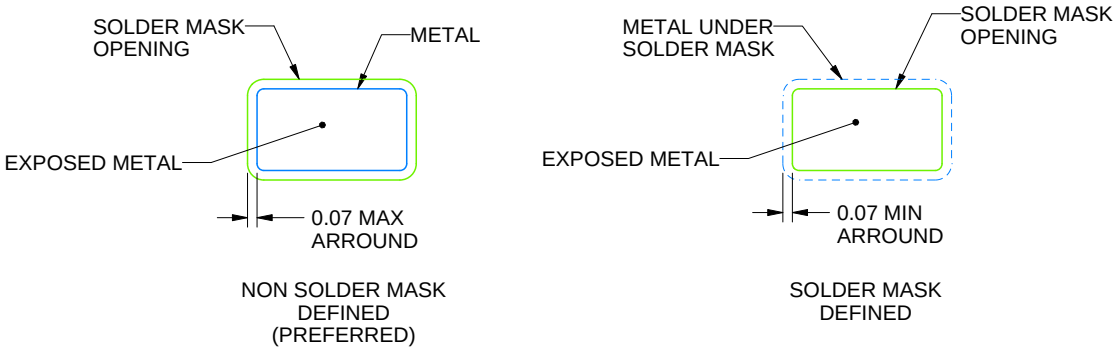
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

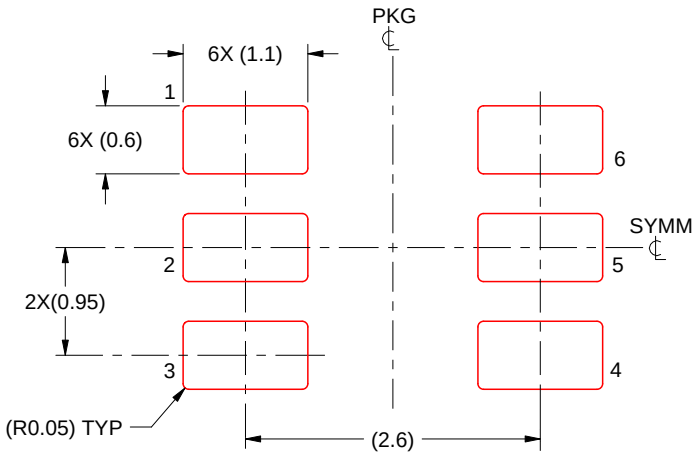


SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

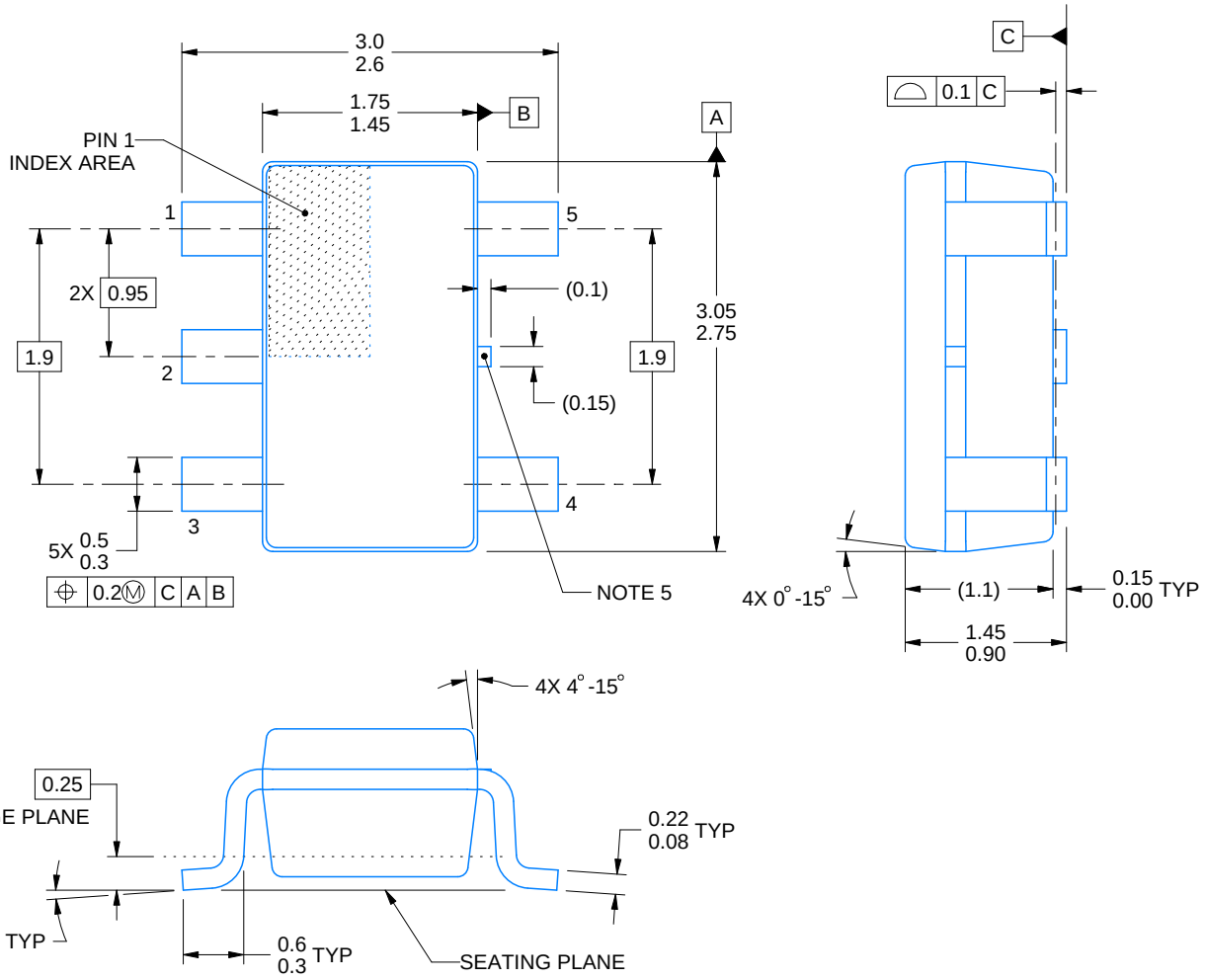
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

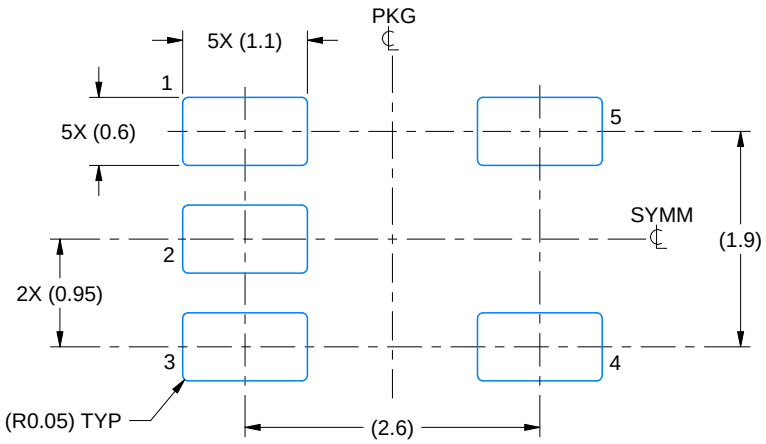
SMALL OUTLINE TRANSISTOR



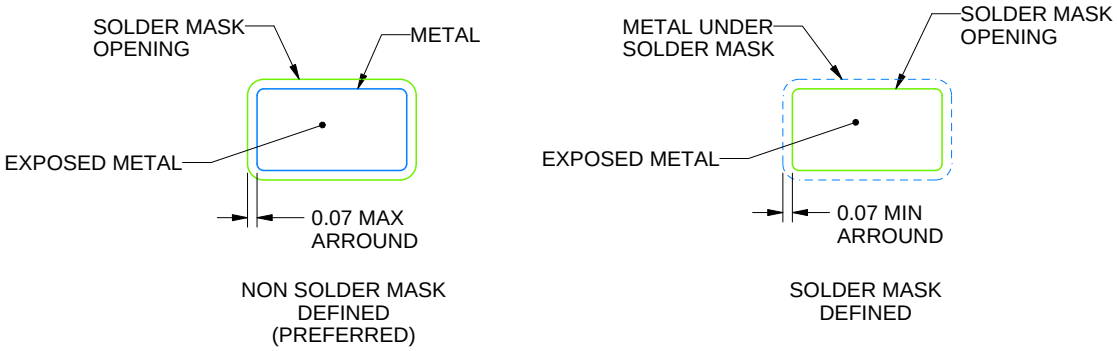
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

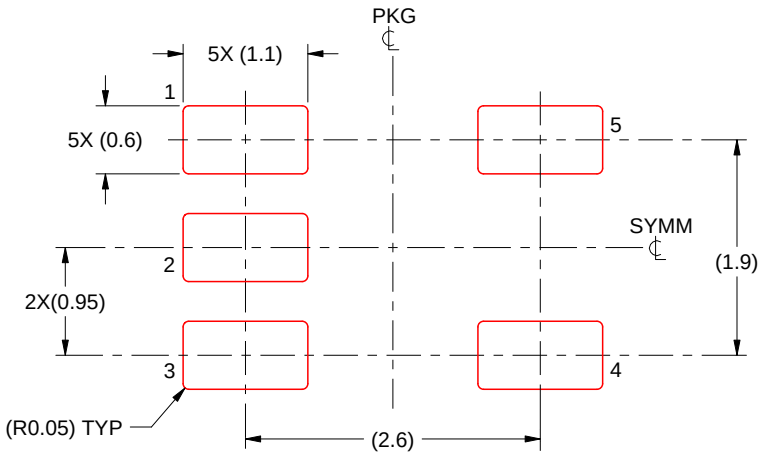


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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